

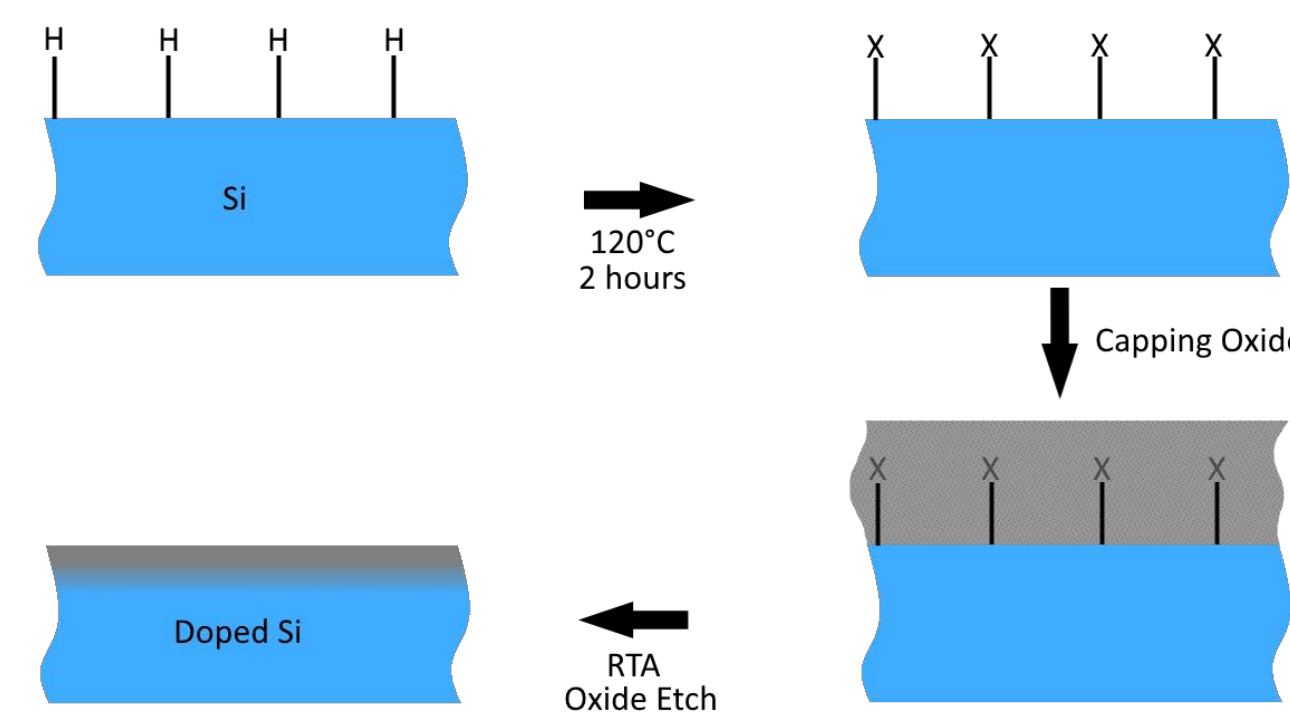
Project Objectives/Motivation

Goal: To create MOSFETs with MLD doped source/drain and characterize the process and electrical characteristics.

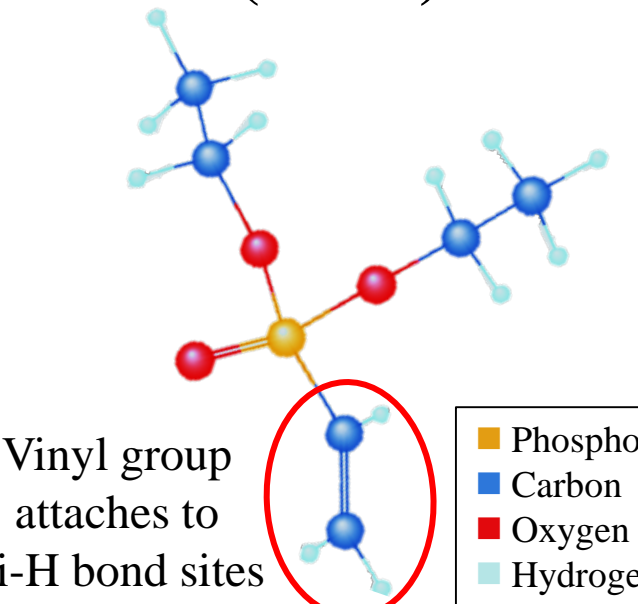
- MLD dopes silicon by creating a self-assembled monolayer of a dopant-containing compound followed by a rapid thermal anneal to form ultra-shallow junctions with high surface concentrations.
- Previously, N+P diodes doped with MLD have been fabricated and characterized, but patterned using mesa etch, not patterned SiO₂.
- Advantages of MLD over conventional doping techniques such as ion implantation or spin-on dopants include: conformal doping of both planar and non-planar substrates, no crystalline damage to the substrate, and use of less hazardous chemicals.
- MLD applications are not limited to IC industry, also attractive to solar industry for use as selective emitter or passivated contact.

MLD Process

- Etch p-Si sample in HF to create hydrogen-terminated surface
- Immerse sample in 1:25 V:V ratio of DVP:mesitylene at 120°C, 2 hrs
- Rinse sample using a sequence of solvents of decreasing polarity
- Deposit 50 nm of PECVD oxide as capping layer
- Anneal sample for 5 min at 1000°C
- Etch capping layer with HF to remove

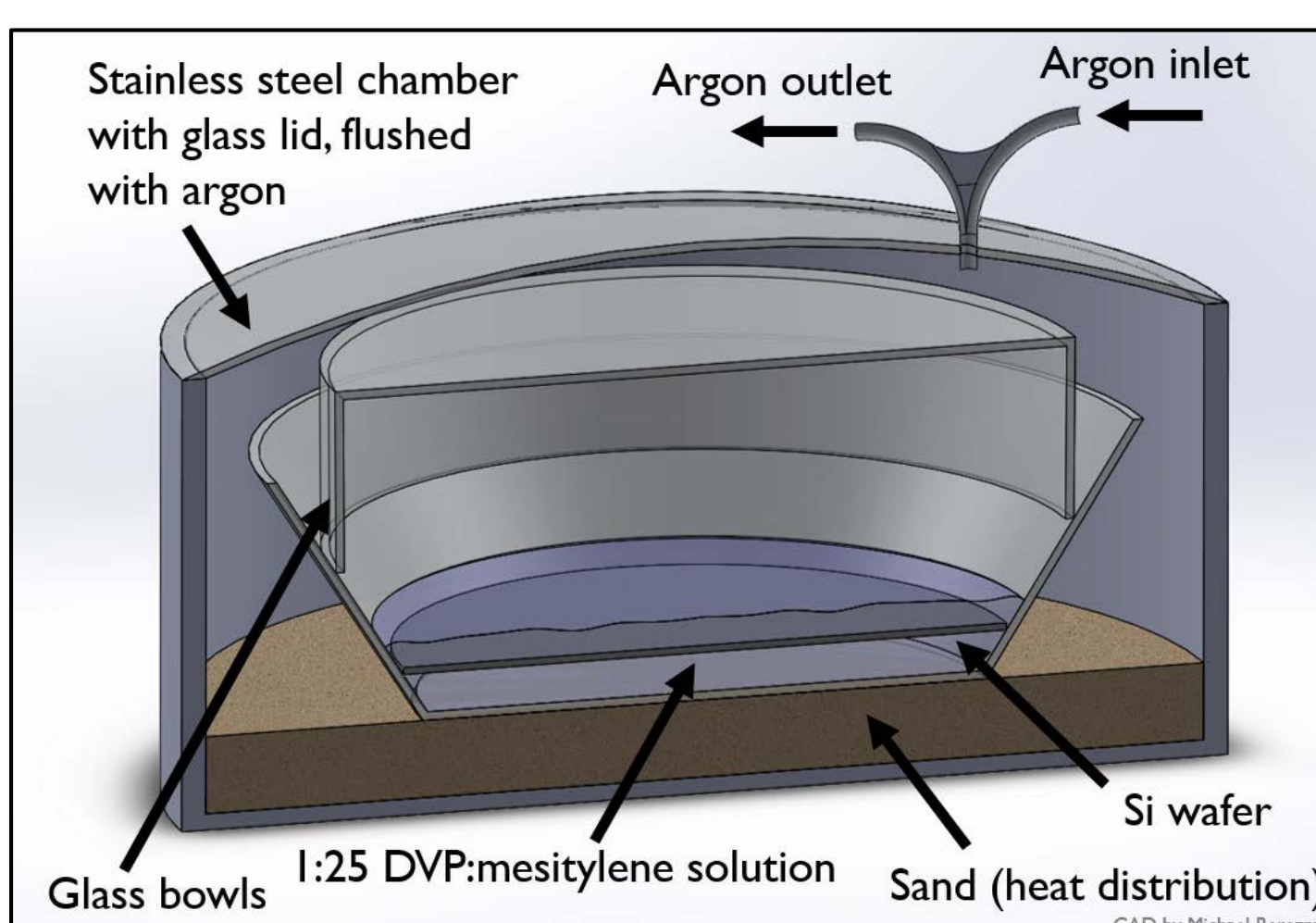


Diethyl vinylphosphonate (DVP)



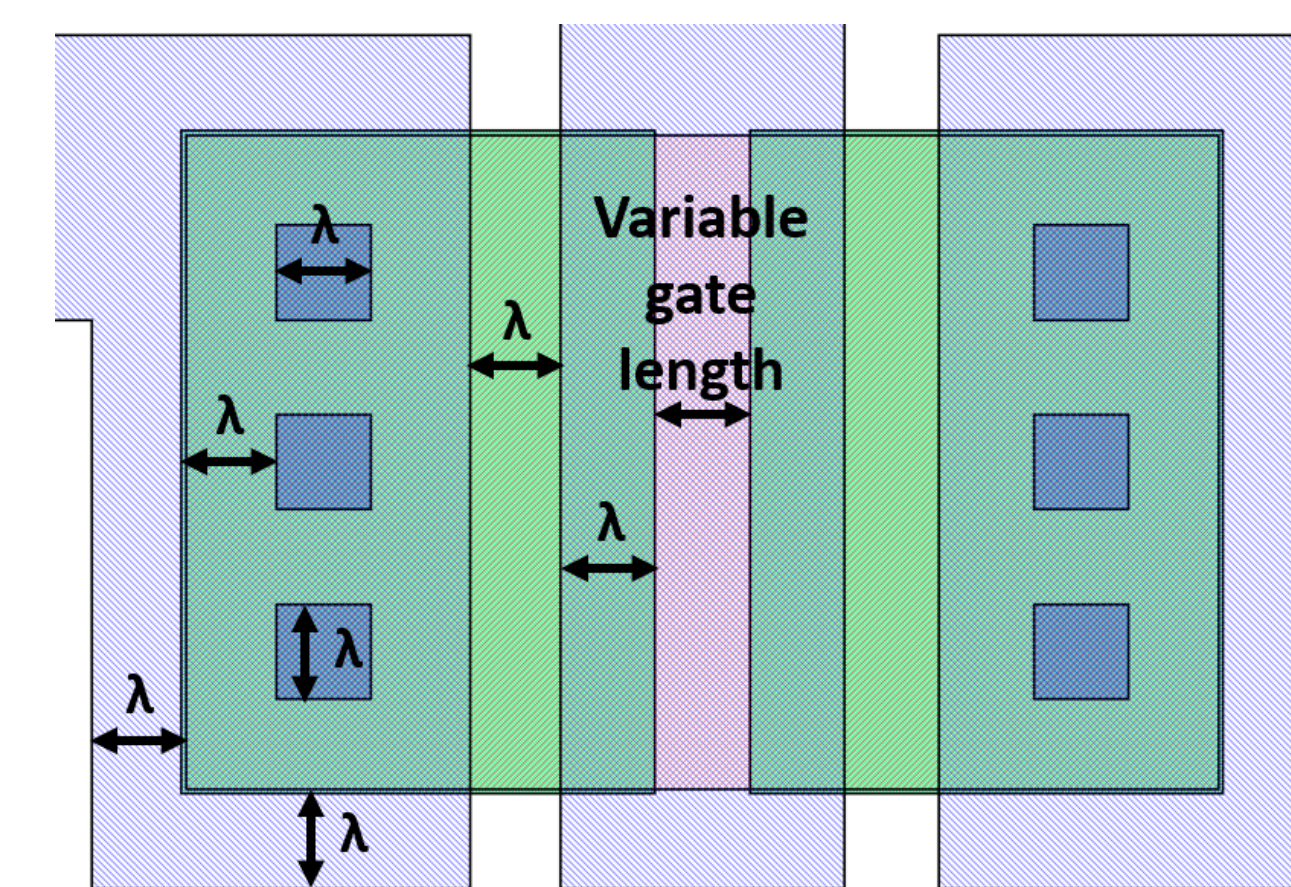
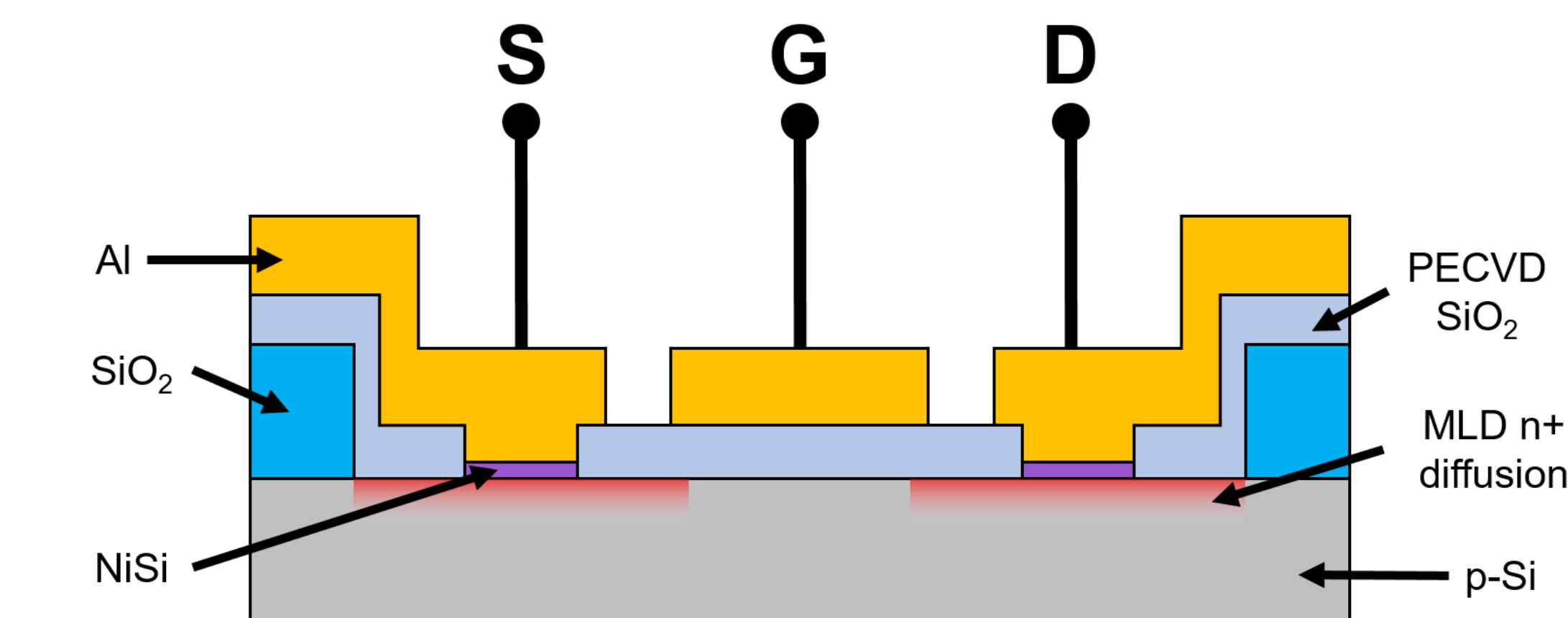
MLD Chamber Design

- Economic chamber designed using items purchased from local home goods stores (cooking pot and glass bowls) and items readily available in chemistry stockrooms.
- Apparatus must:
 - Evenly heat solution
 - Internally condense solution
 - Immerse 6" wafer in solution
 - Allow argon flow in/out



MLD FET Process Design

- Process designed to:
 - Ensure S/D areas are not too far from gate/channel
 - Minimize thermal budget post-MLD (no processing > 700°C)
 - Minimize possibility of junction spiking (nickel silicide)

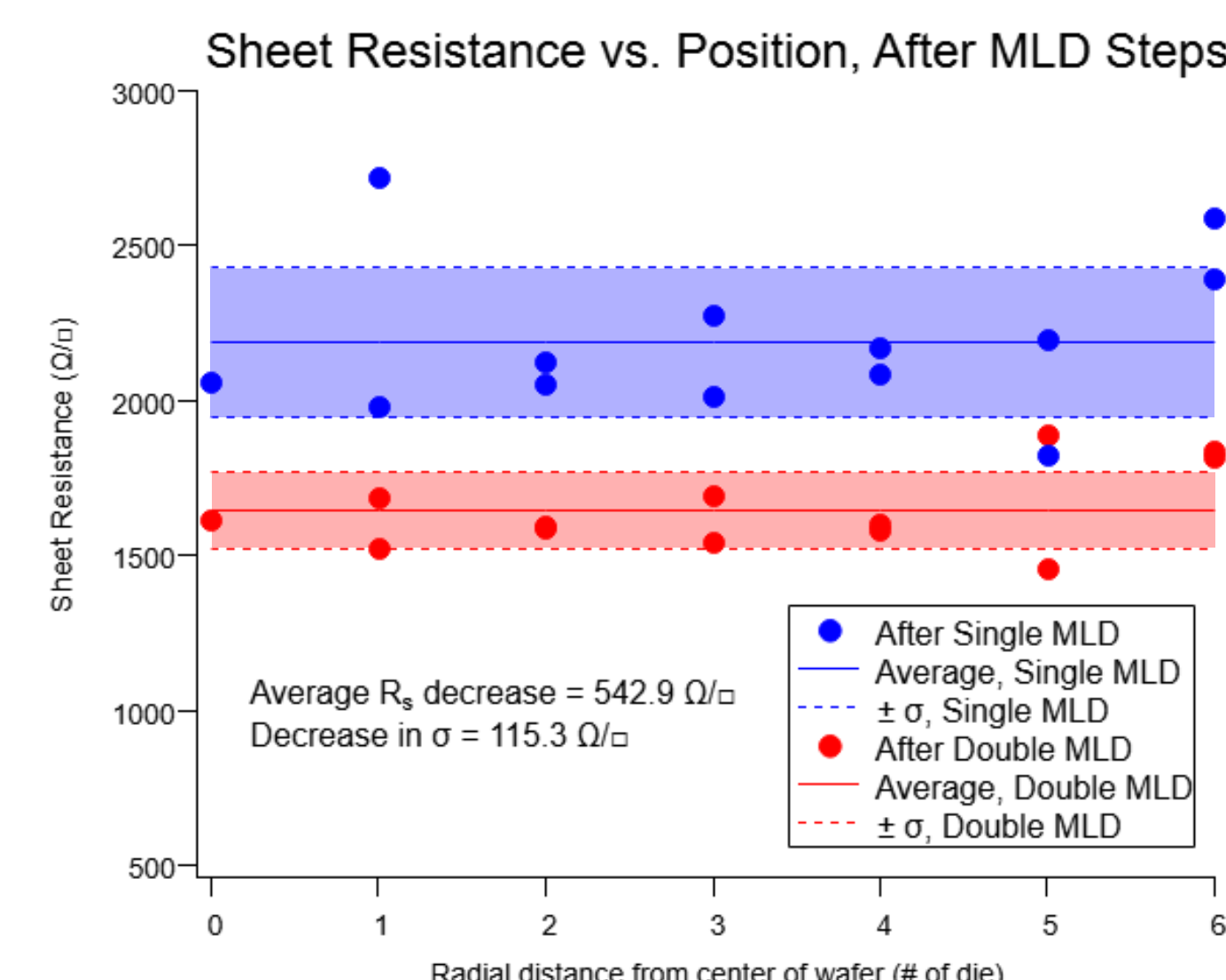
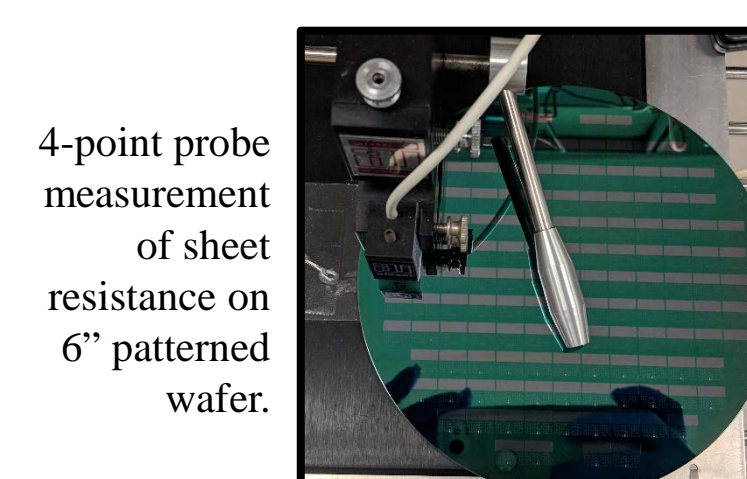


- Mask Design:
 - λ -based design rules
 - $\lambda = 10 \mu\text{m}$
 - Gate lengths set to 0.5, 1, 2, 5, 10 μm
 - Transistors with variable widths, inverter circuits, and resistors included in designs.

Measurement of Doping

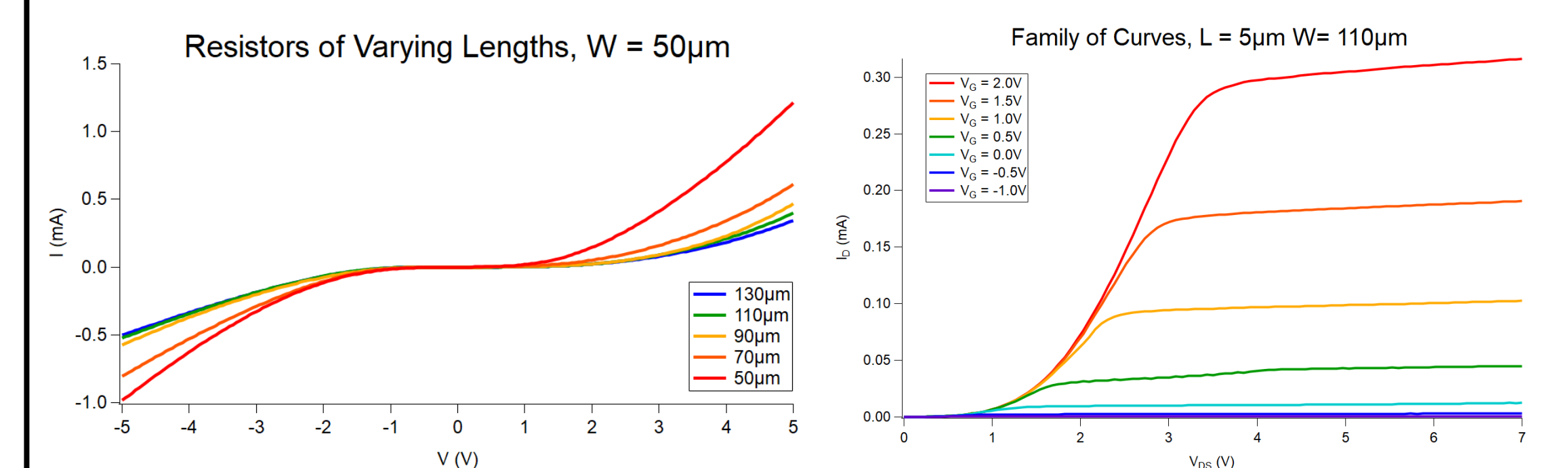
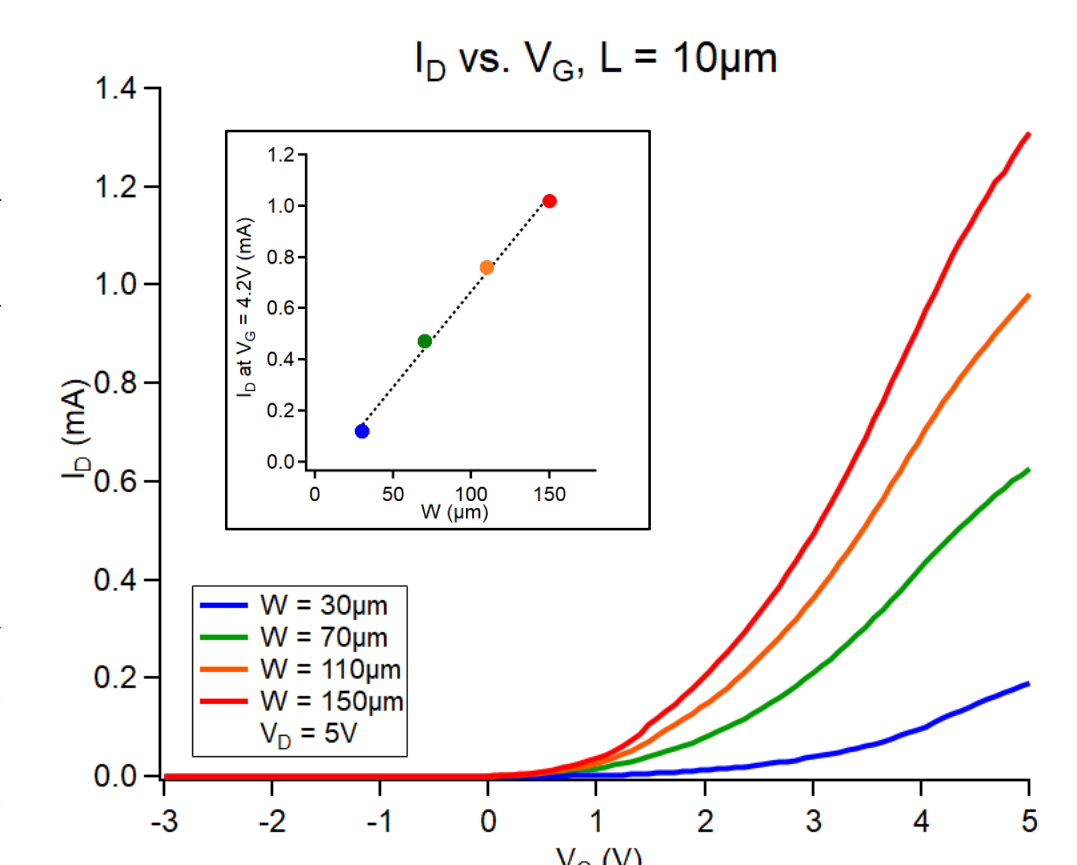
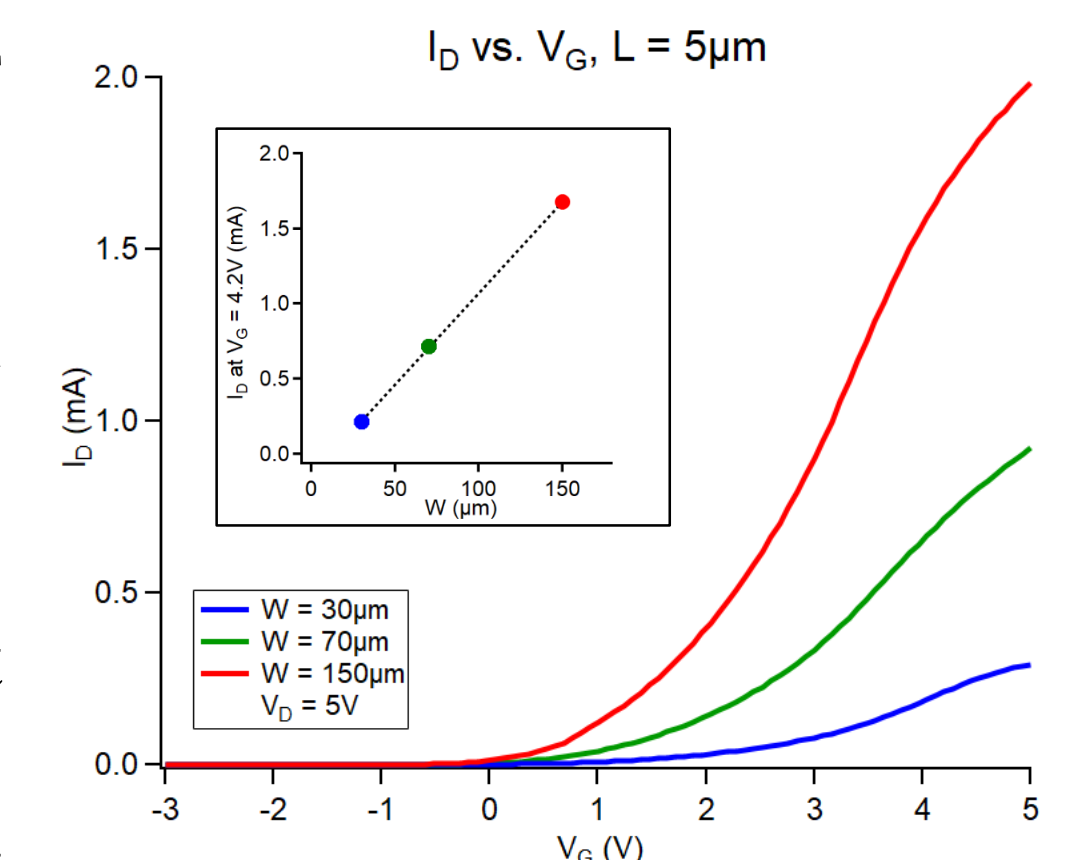
- Doping via MLD is quantified by sheet resistance ($R_s, \Omega/\square$)
- Measurements taken using 4-point probe
- p-Si pieces (~1 cm x 2 cm) doped to determine bulk R_s values
- Single MLD: sample immersed, capped, annealed, etched
- Double MLD: after a single MLD, MLD process is repeated
- S/D areas on patterned wafers doped, R_s values measured in large windows on select die to determine uniformity
 - For patterned wafers, trends and uniformity are considered, not numerical R_s values (4-point probe assumption that substrate is infinite compared to probe spacing is invalid for patterned case)

	Piece, $R_s (\Omega/\square)$	6" wafer, $R_s (\Omega/\square)$
Single MLD	1058.8	2189.0
Double MLD	769.6	1646.1



Device Characterization

- Field effect demonstrated; V_T ranges across devices sizes between -0.5V and -1.5V, indicating depletion mode devices as expected, since no V_T adjustment was made.
- I_D vs. V_G curves shown at right for two different lengths and multiple widths; current scales with width as expected.
- Measurement of resistors and family of curves indicates high series resistance, likely due to issues with contacts.
- Due to an overetch of the SiO₂ patterning the S/D areas, the 0.5, 1, and 2 μm devices were shorted and not functional.



Conclusions/Future Work

MOSFETs with S/D doped via MLD were successfully designed, fabricated, and characterized. The ability of MLD to dope areas patterned with SiO₂ was demonstrated. A new economic chamber design to complete the MLD process was also designed and tested successfully. The devices showed high series resistance, which may have been caused by oxidation of the Ni before the NiSi process or by Al junction spiking. In future work, the robustness of the contact process can be improved, as well as reducing overetch of the S/D patterning to increase device yield.

Acknowledgements & References

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- Senior Design Advisors and Students
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