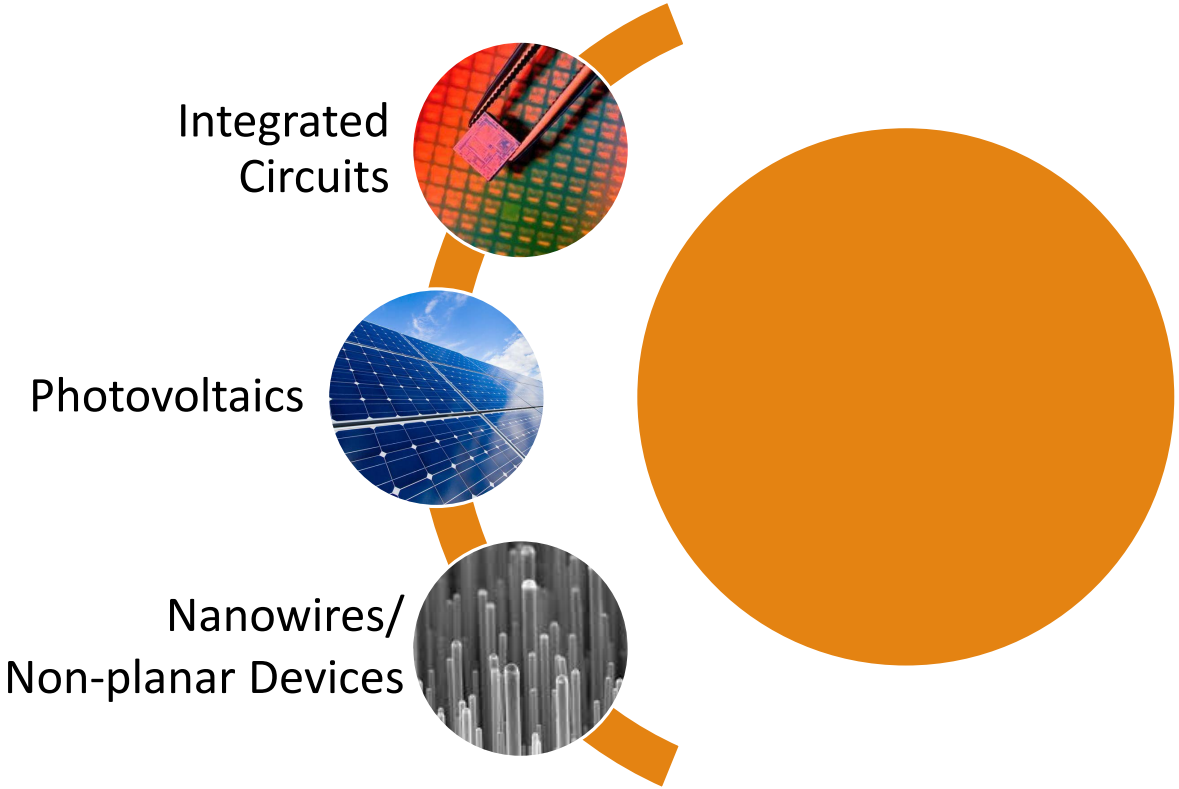
Monolayer doping (MLD) for ultra-shallow junction MOSFET fabrication

JENNA DORAN

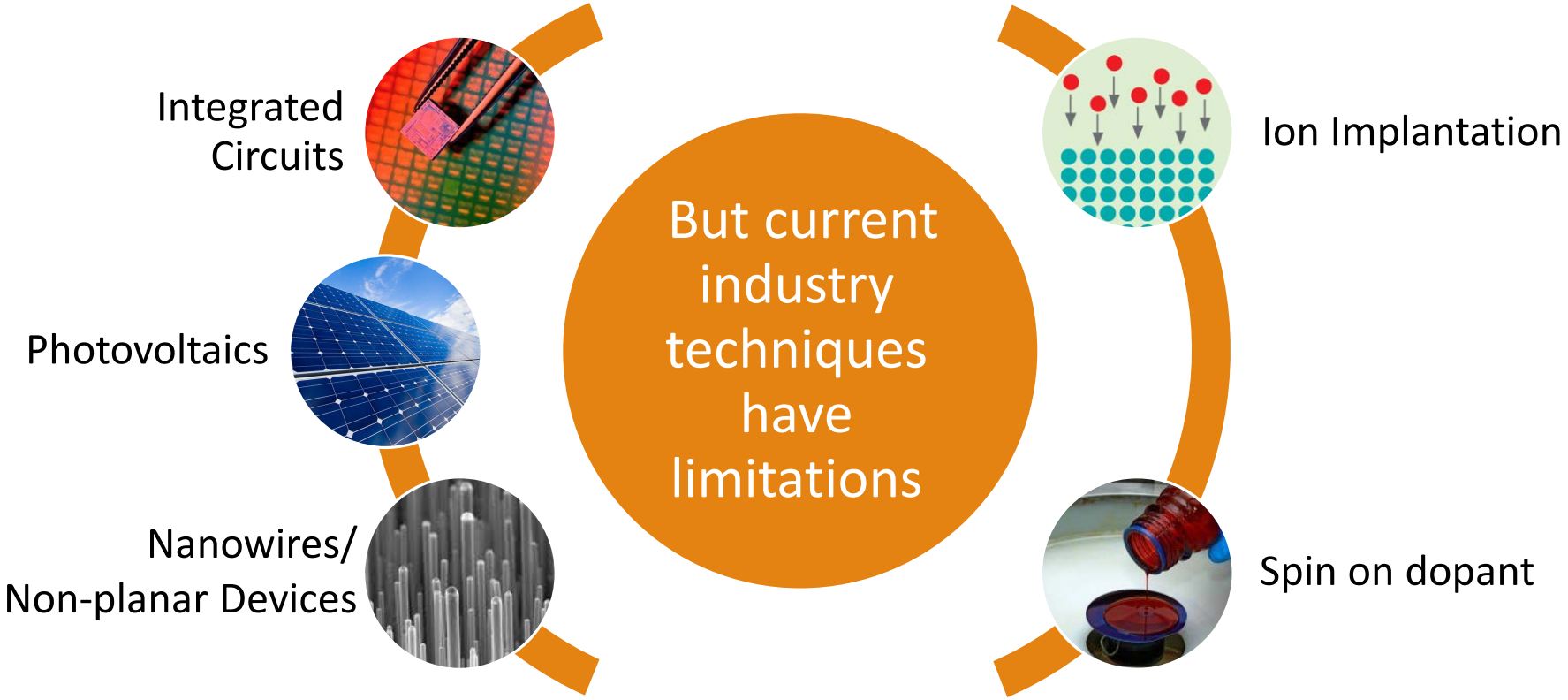
ADVISORS: DR. SANTOSH KURINEC, DR. SCOTT WILLIAMS

ROCHESTER INSTITUTE OF TECHNOLOGY

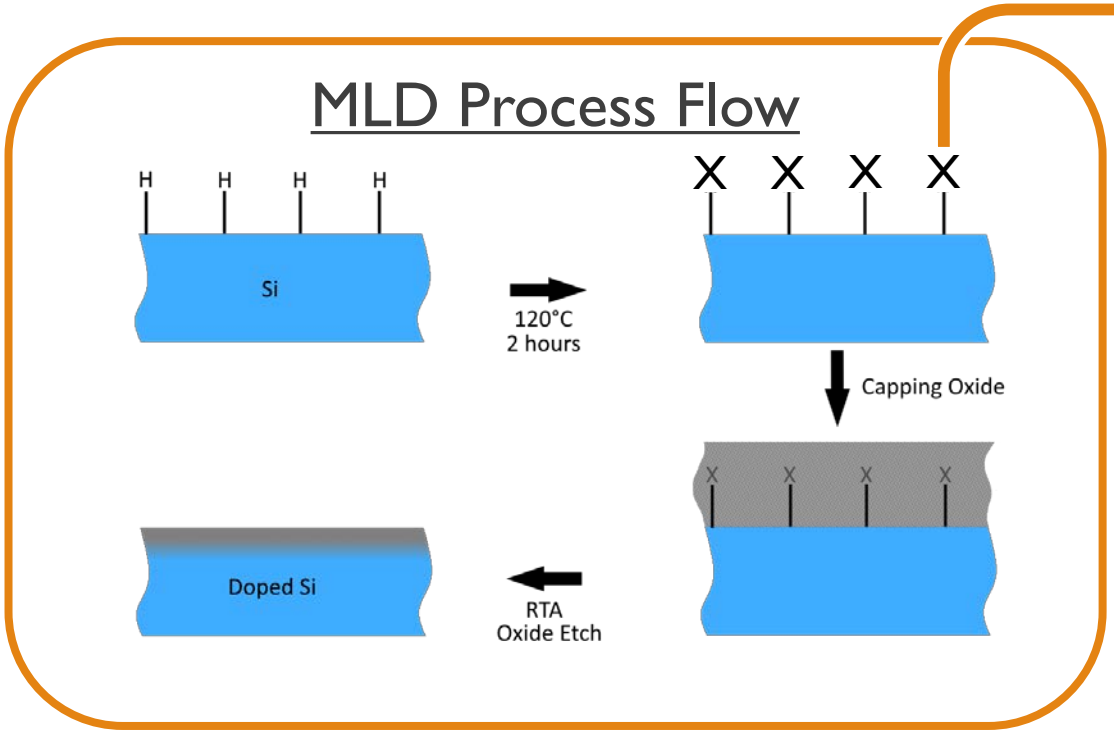
Doping is key for increasingly small semiconductor devices



Doping is key for increasingly small semiconductor devices

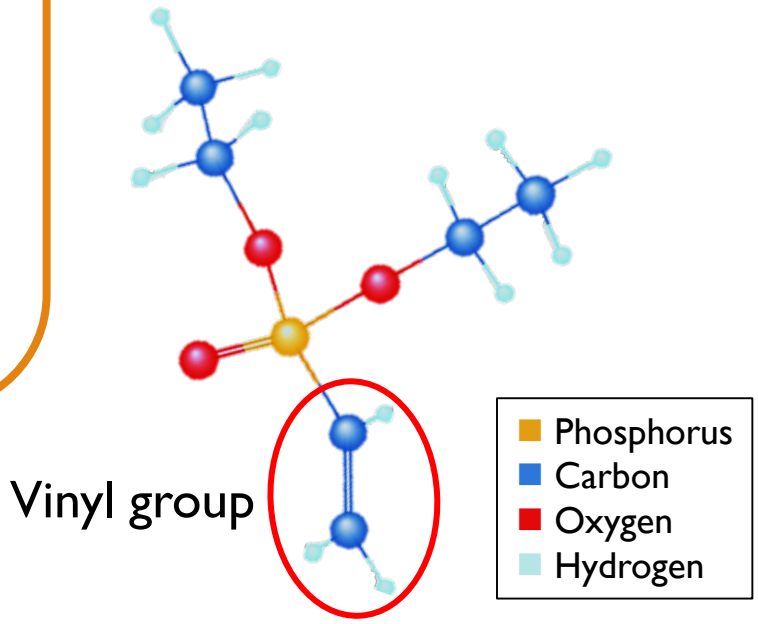


MLD provides ultra-shallow, high concentration doping



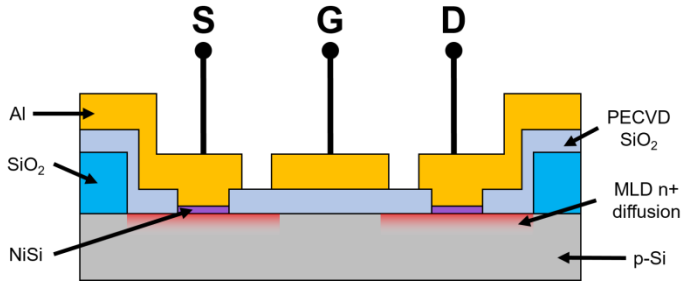
X:

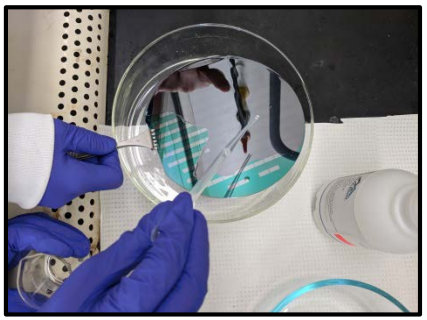
Diethyl vinylphosphonate

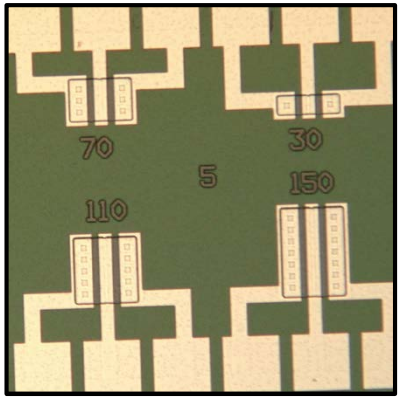


Goal: Create MOSFETs with MLD doped source/drain

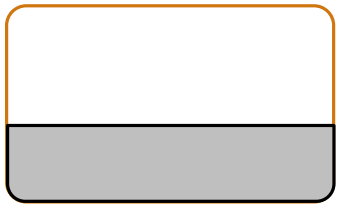
1. Develop a process to fabricate MOSFETs with MLD doped source/drain
2. Design MLD process chamber and characterize results
3. Fabricate and characterize devices







Process flow designed for MOSFETs with MLD doped S/D



Start with p-Si

Pattern field oxide

MLD n+ diffusion

Etch active area

NiSi anneal

Deposit Ni

Contact cuts

Deposit gate oxide

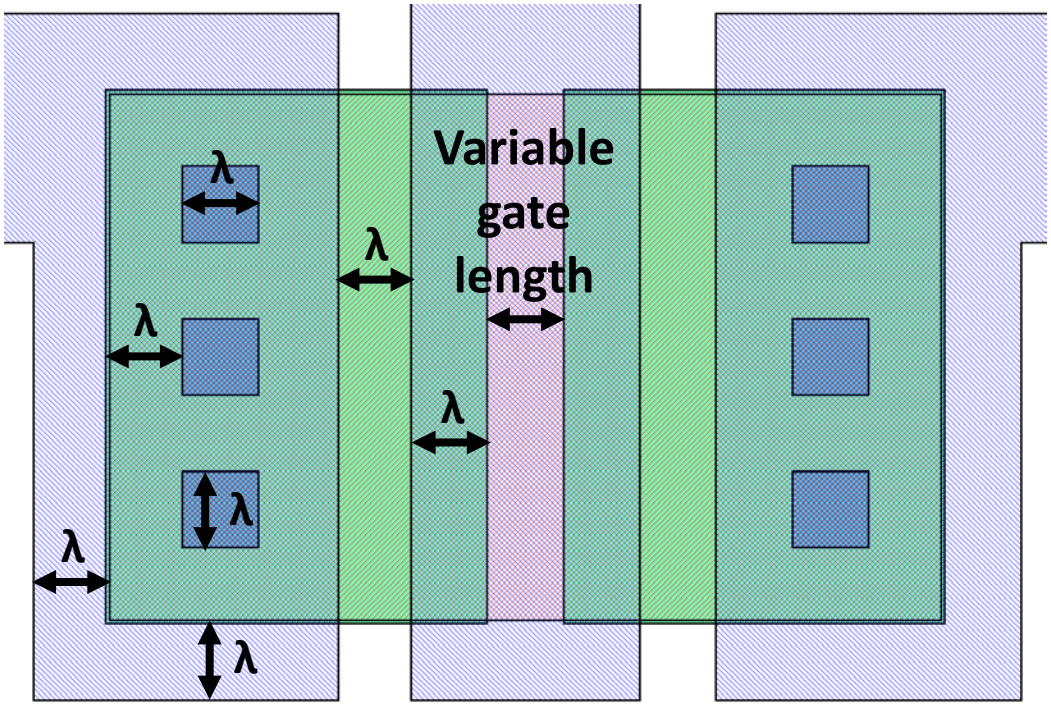
Etch Ni

Deposit Al

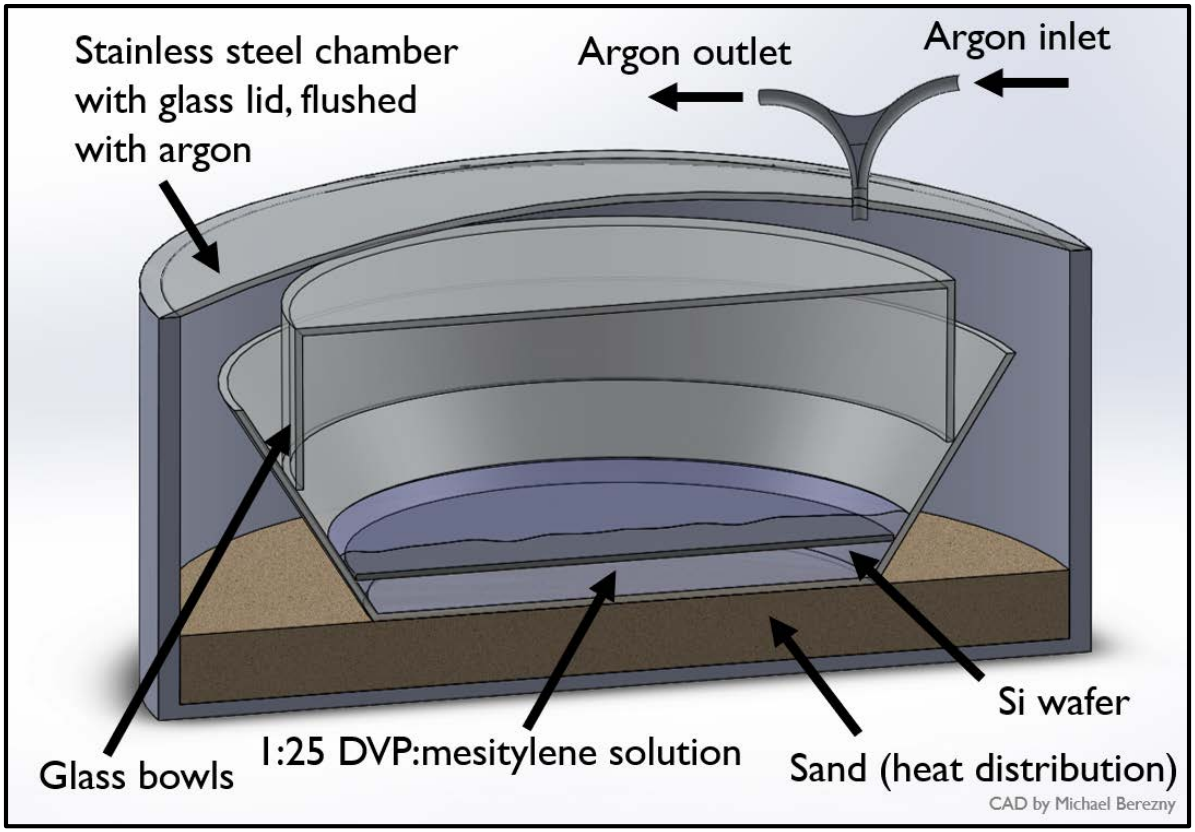
Pattern Al

Mask levels designed to fit processing constraints

- λ-based design rules
  - λ = 10 μm
  - Gate length was not controlled by λ, set to 0.5, 1, 2, 5, 10 μm
- Transistors with variable widths, inverter circuits, and resistors included in designs

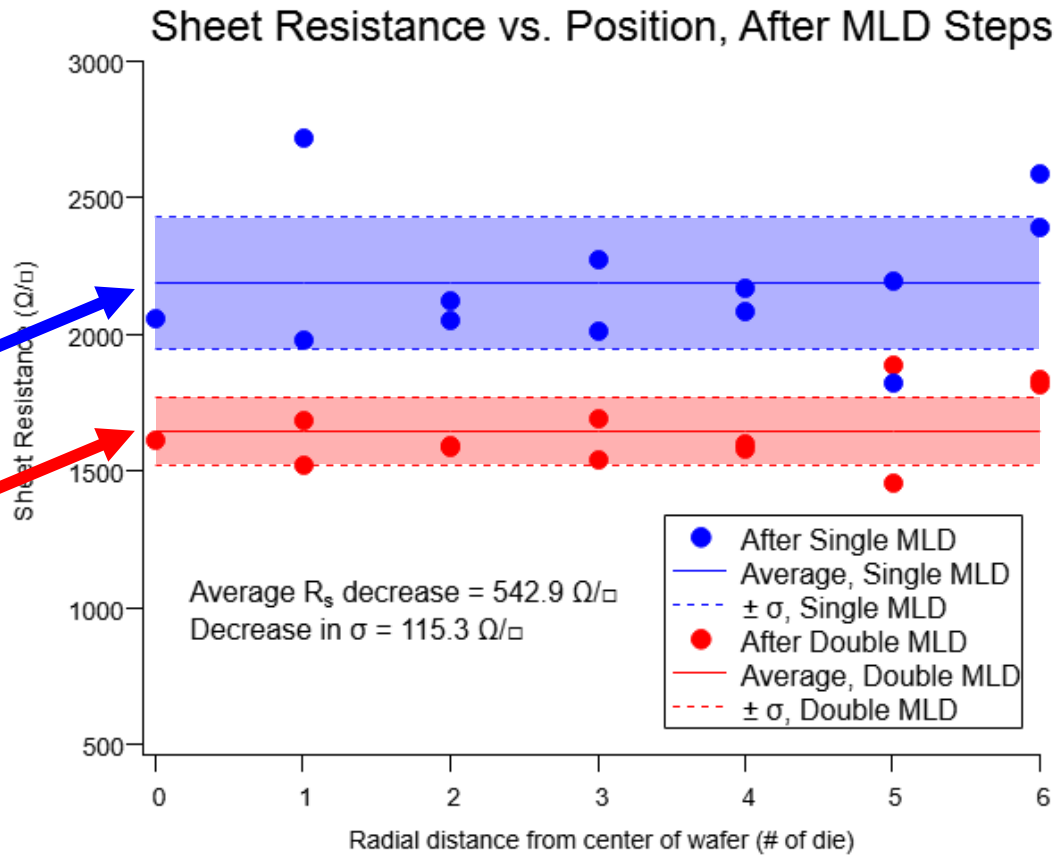


MLD process chamber designed to be low-cost and functional

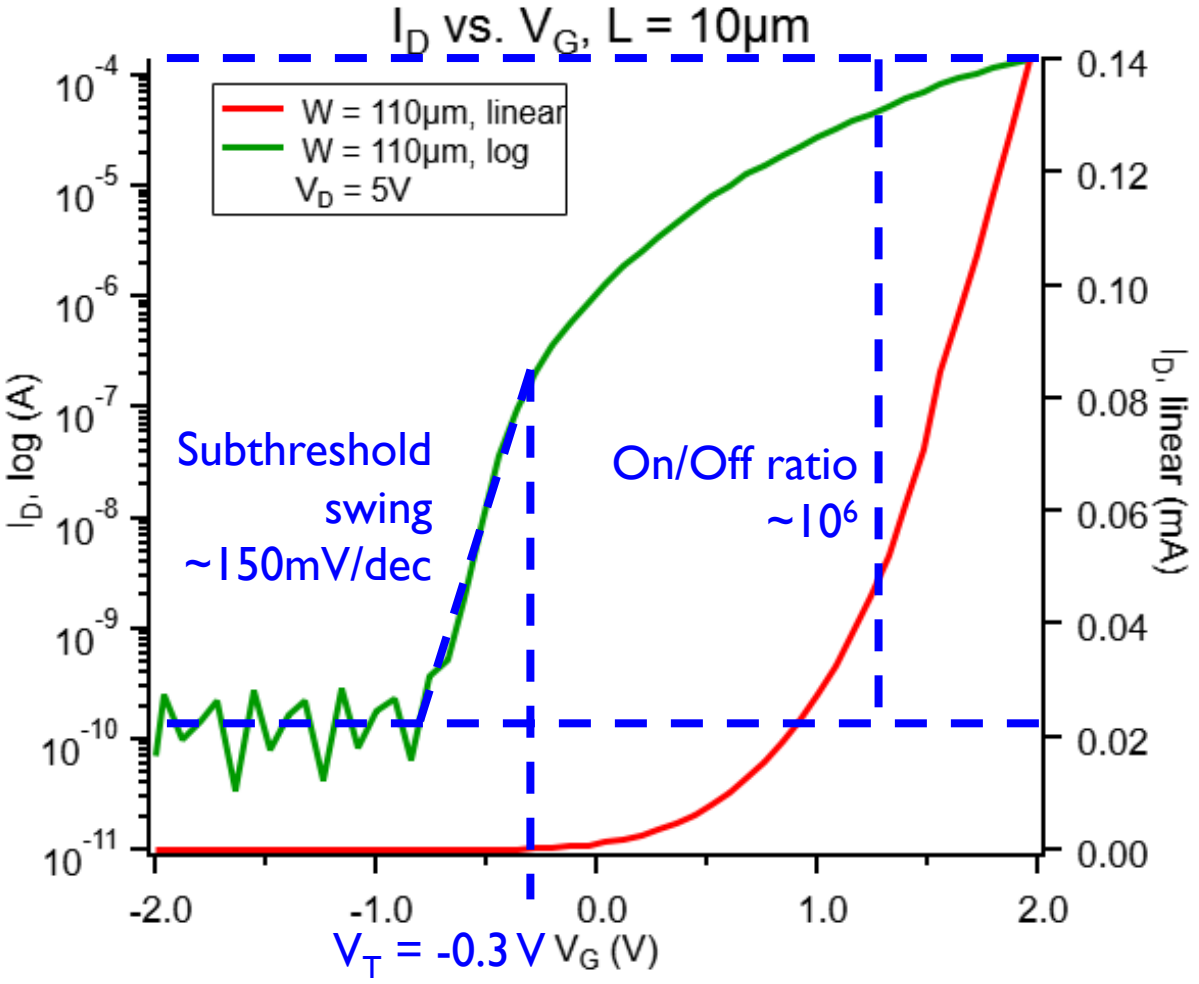


Patterned wafers doped via MLD are uniform and follow bulk trend

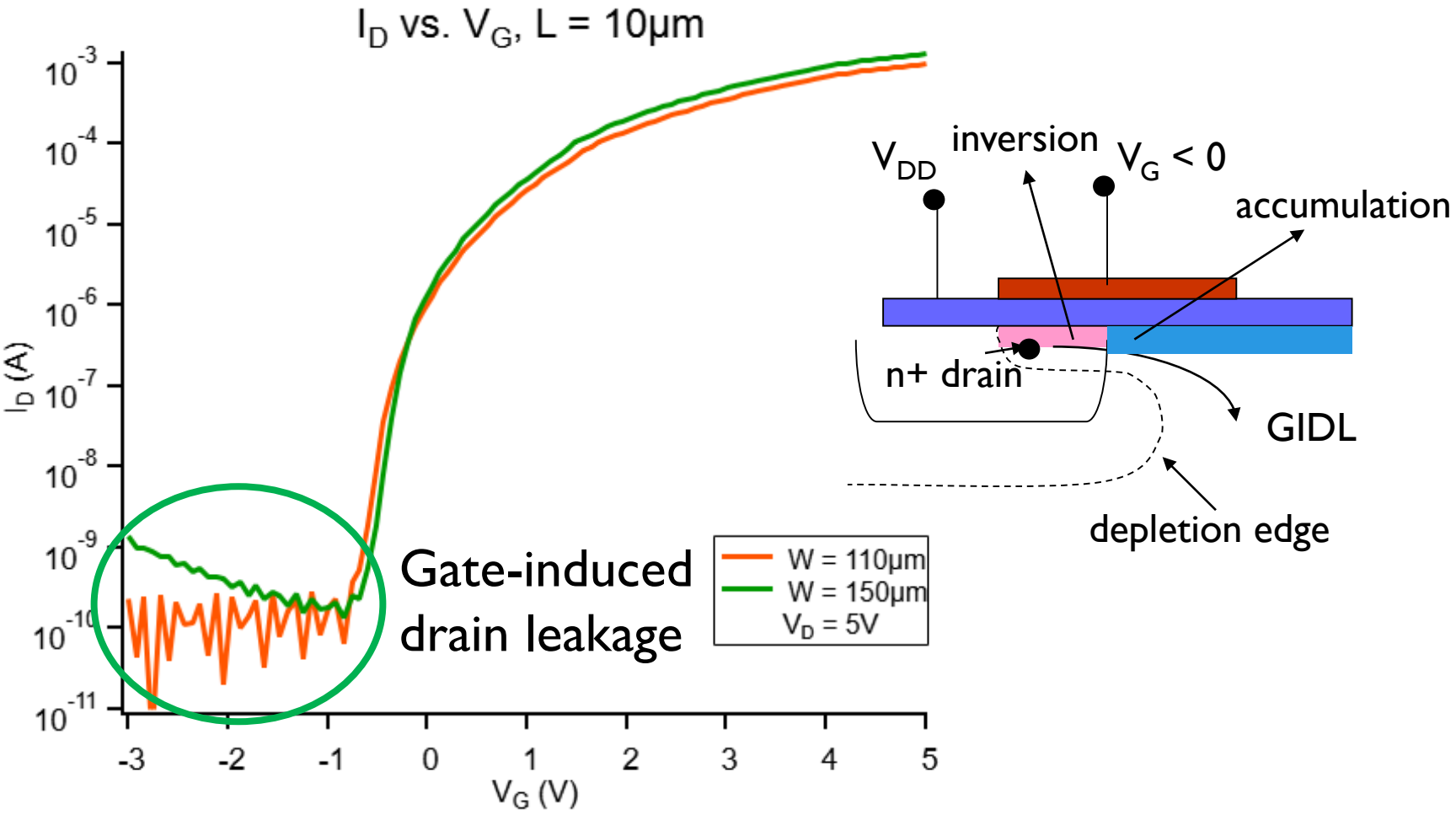
	Piece, R_S (Ω/□)	6" wafer, R_S (Ω/□)
Single MLD	1058.8	2189.0
Double MLD	769.6	1646.1



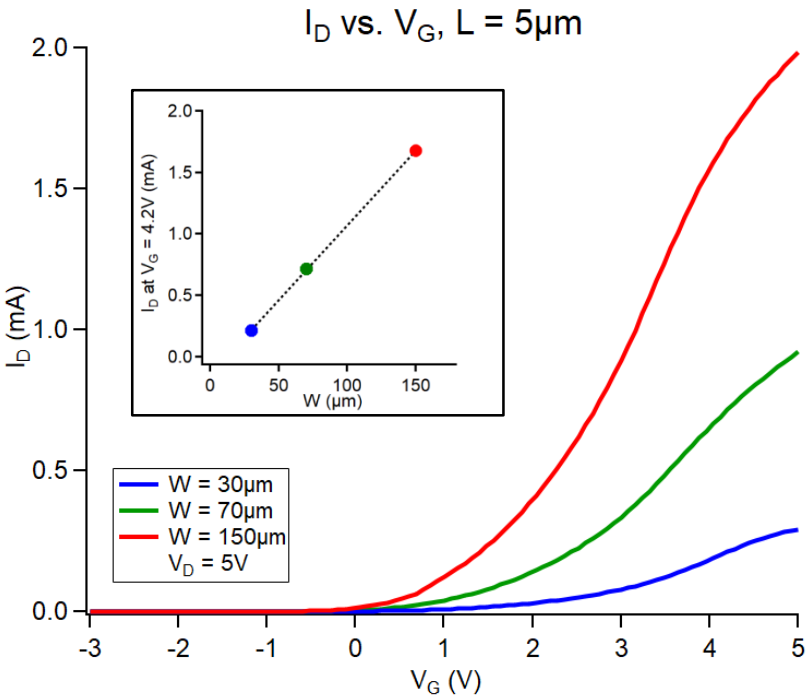
Transfer characteristic shows field effect behavior

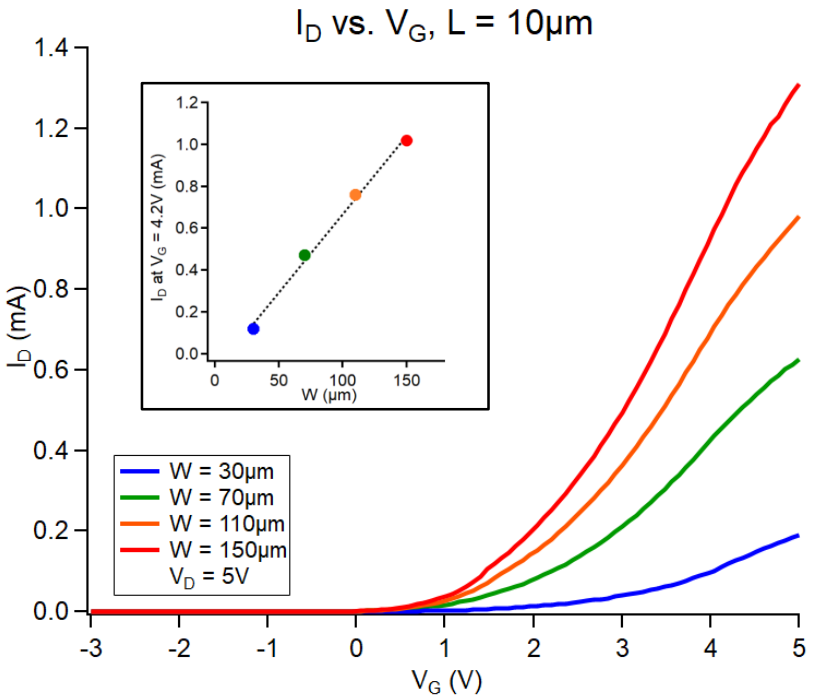


GIDL confirms dopant diffusion to gate edge and beyond

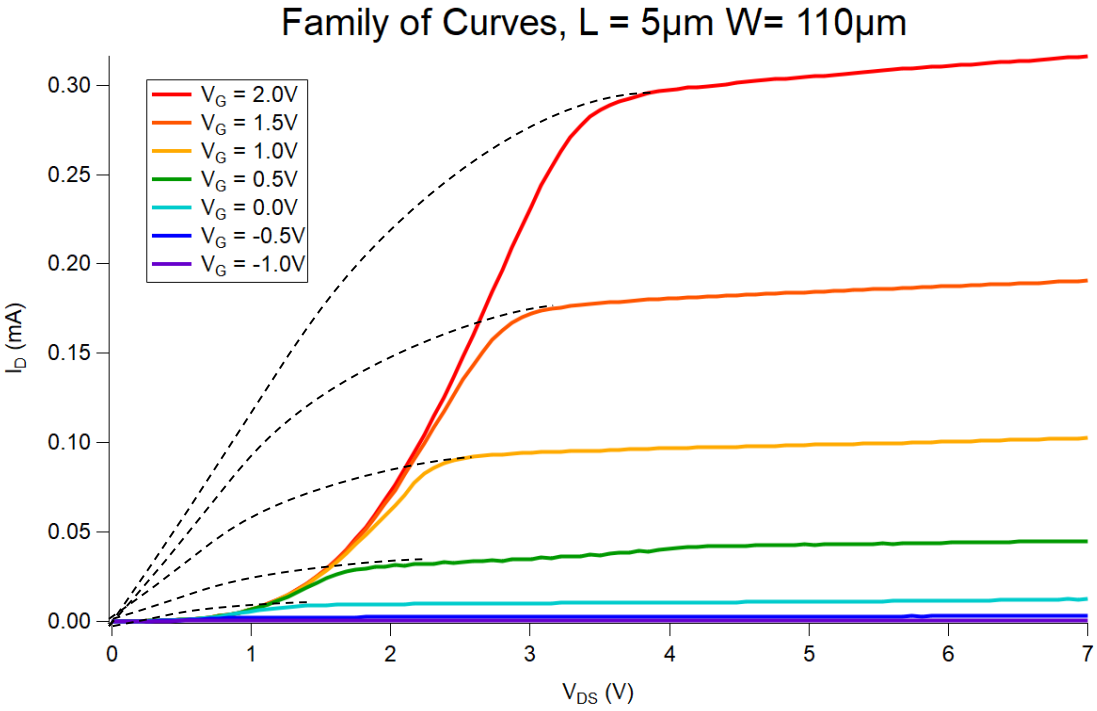


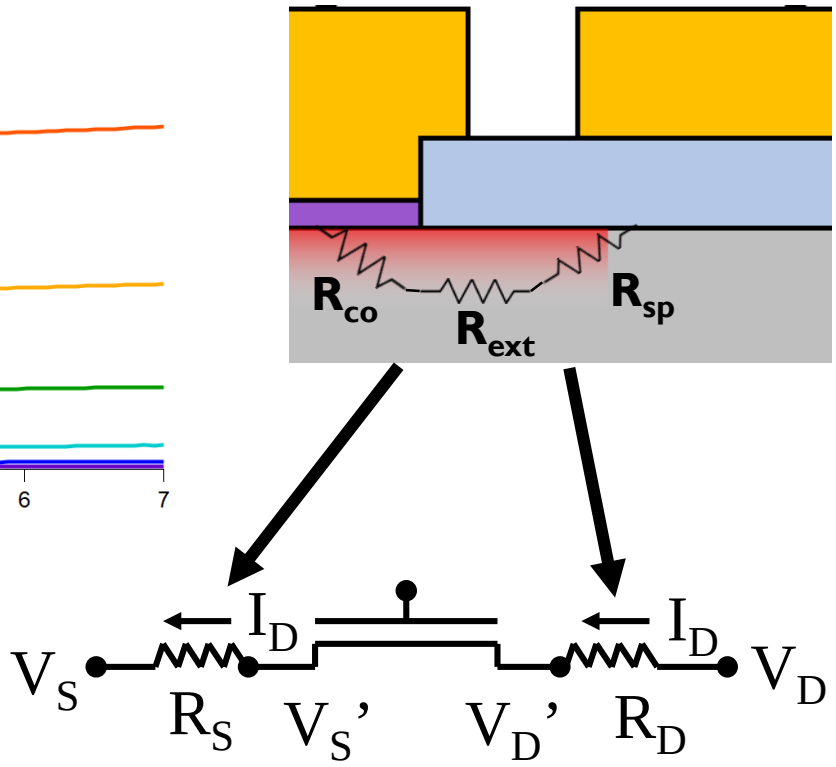
Current scales linearly with increasing W





Output characteristics reveal significant series resistance





Conclusions and future work

- MOSFETs with source/drain doped via MLD successfully fabricated and characterized
  - Devices demonstrated field effect behavior
  - Chamber design for MLD process was successfully tested
  - Proved that MLD can be patterned using SiO_2
- Future work:
  - Determine cause of high series resistance and revise process to minimize issue
  - Use a less isotropic etch for FOX or redesign masks to improve device yield
  - Use a better quality gate oxide – possibly hi-k

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- Former Students on this Project: Astha Tapriya, Brian Novak, Casey Gonta
- Senior Design Advisors and Students
- SMFL Staff

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Images:

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