Monolayer doping (MLD) for ultra-shallow junction MOSFET fabrication

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ABSTRACT

As devices continue to shrink following the trend of Moore's law, and non-planar devices such as FinFETs and 3D nanostructures become more common, ultra-shallow (sub-50 nm) junctions become more desirable. Semiconductor devices are traditionally doped using a combination of ion implantation or spin-on dopant and thermal diffusion techniques; however, these have limitations such as crystalline damage, use of hazardous chemicals, or glassy skin formation. Monolayer doping (MLD) provides a non-destructive and less hazardous method for doping the silicon surface. MLD creates a self-assembled monolayer of a dopant-containing compound followed by a rapid thermal anneal to form ultra-shallow junctions with high surface concentrations. Using the dopant-containing compound diethyl vinylphosphonate (DVP), MLD is used to dope the source and drain of MOSFETs. A fabrication process for these devices is designed to ensure that the source and drain are not too far away from the gate, the thermal budget is limited after the MLD process (no processing >700 °C), and to minimize the possibility of junction spiking. The MLD process chamber is also redesigned to be more economical and ensure process repeatability. Electrical characterization of the devices show field effect behavior, confirming that MOSFETs have been successfully fabricated and demonstrating the ability of MLD to be patterned using SiO_2.

1. INTRODUCTION

Smaller devices and non-planar devices present unique challenges for doping processes.[1] Current industry standards such as ion implantation or spin-on dopant processes have limitations. Smaller devices require shallower junctions, so any surface defects or imperfections have a magnified impact. Ion implantation causes crystalline damage which can negatively affect device performance. Spin-on dopants can leave residues after the glassy skin is etched away, which also results in suboptimal device performance. Non-planar devices also require conformal doping. To achieve conformal doping with ion implantation, a combination of several angled implants must be used, which adds extra process time and cost. Spin-on dopants can conformally coat structures, however the viscosity of the solution can make it difficult to conformally coat small non-planar features, e.g. nanowires.

Monolayer doping is an attractive alternative to these other industry standard doping methods. It creates no crystalline damage to the wafer surface (unlike ion implantation), does not leave residues on the wafer surface (unlike spin-on dopants), and uses much less hazardous chemicals (compared to both ion implantation and spin-on dopants). It also can conformally dope non-planar structures such as nanowires without modifying that basic MLD process.[2]

Previously at RIT, n+p diodes were fabricated using MLD doped n+ diffused regions.[1] The monolayer doping process was characterized using sheet resistance measurements and SIMS, and the devices were characterized electrically. The experimental data agreed with a fitted unified diode model, confirming good electrical performance and successful fabrication of the diodes. One key difference between this previous work and the work explored in this paper is the device isolation. In previous work, a blank wafer underwent the MLD process and the devices were isolated using a mesa etch. In this work, SiO_2 will be used to pattern the wafer prior to the MLD process, since the MLD process is selective to silicon. The diodes also used a back-side contact, whereas the MOSFETs fabricated in this work only have front-side contacts.

2. THEORY

Monolayer doping relies on the formation of a self-assembled monolayer of a dopant-containing compound to act as the source of dopant diffusion. The dopant-containing compound explored in this work is diethyl vinylphosphonate (DVP), which is shown below in Figure 1. Diethyl vinylphosphonate is an organic compound with a central phosphorus atom which acts as the n-type dopant. The vinyl group substitutes with

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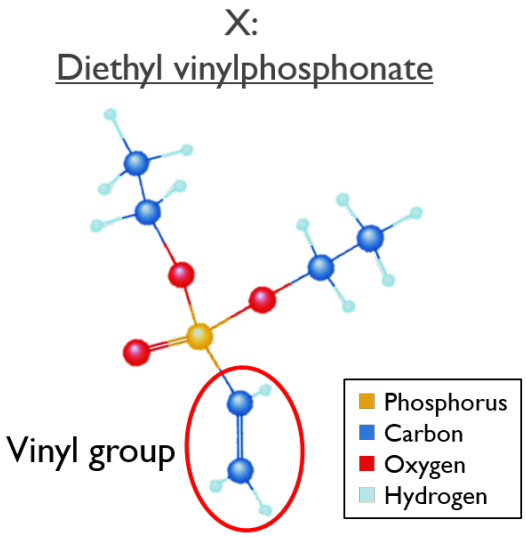

Figure 1. Diethyl vinylphosphonate molecule, showing vinyl group which attaches to the silicon surface.

hydrogen atoms on the surface of the silicon sample, and the reaction continues until the bond sites are saturated. Due to the footprint of DVP, saturation of bond sites does not imply that all Si:H bond sites will be occupied by a DVP molecule, rather that there are no more accessible bond sites and the self-assembled monolayer has been formed.

DVP is extremely sensitive to and will react with ambient air and water vapors, which prevents the molecule from forming the self-assembled monolayer. The MLD process include a solution preparation procedure which attempts to minimize any adverse reactions. First, any glassware that contacts the DVP is flamed prior to use in order to remove water residues. The monolayer formation occurs with the sample submerged in a solution, where DVP is mixed with a solvent (mesitylene). The solution is mixed in a glove bag filled with argon in a 1:25 volume to volume ratio of DVP:mesitylene. After the solution is mixed, it is removed from the glove bag: it is protected by a layer of heavy argon gas essentially capping the solution, which does not allow the lighter ambient air molecules to interact with the solution. The solution is then sparged with argon gas to ensure that the solution is fully saturated with argon, which will also protect it from reaction with the ambient air and water vapors.

The monolayer doping process used in this work is adapted from work by Ho et al.[3] The process is illustrated above in Figure 2. It begins with a hydrogen-terminated silicon surface; the sample is etched in 10:1

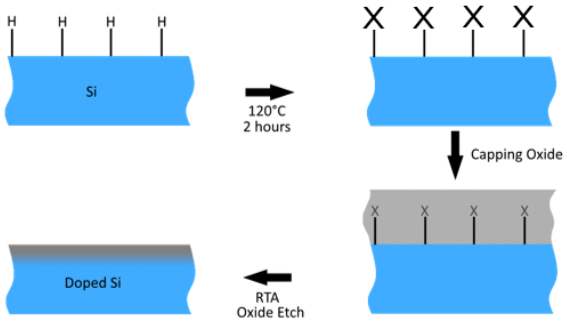

Figure 2. MLD process flow.

buffered oxide etch (BOE) for 15 seconds to remove any surface oxide and create the hydrogen-terminated surface. The sample is then placed in a custom-designed chamber flushed with argon, submerged in the prepared solution of DVP and mesitylene for 2 hours at 120°C. The self-assembled monolayer formation reaction occurs in the solution, and when the sample is removed, any further reaction is halted. The sample is rinsed with a sequence of solvents of decreasing polarity (toluene, acetone, methanol, then DI water), dried between each step with nitrogen gas. This rinse process removes any residual solution.

After the sample is sufficiently rinsed, a 50 nm capping layer of SiO_2 is deposited via plasma-enhanced chemical vapor deposition (PECVD). Next, the sample is annealed with a rapid thermal process under nitrogen for 5 minutes at 1000°C. This process diffuses the phosphorus from the DVP into the silicon, forming the ultra-shallow junction. Finally, the capping layer is etched away using 10:1 BOE.

3. EXPERIMENTAL DESIGN

3.1 MLD Chamber Design

The chamber for the MLD process needed to meet several requirements. First, it needed to accommodate up to a 6" wafer. Second, it needed to evenly distribute heat from a hot plate to the solution. Third, it needed to internally condense the solution. Fourth, it needed to allow argon flow in and out of the chamber. A silicone-sealed chamber was designed previously,[4] the silicone began to degrade and it was determined that the seal was not necessary.

The new chamber was designed to meet the above specifications using economical and readily available materials from local home goods stores and chemistry stockrooms. The design is shown below in Figure 3. The stainless steel chamber is a large cooking pot, and large glass bowls are nested inside the pot to contain and condense the solution. The steam outlet in the pot lid

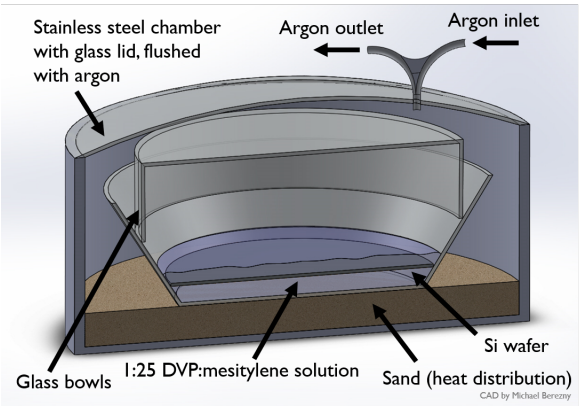

Figure 3. MLD chamber design, labelling key components.

was modified to allow a y-tube joint to be inserted and flow argon in and out of the chamber.

3.2 MOSFET Fabrication Process Flow Design

The fabrication process for MOSFETs with MLD doped source and drain was developed to meet three main criteria. First, the gate needed to be patterned such that it overlapped the patterned source and drain areas. A concern with the MLD process is that feature edges may not doped as well as feature centers due to the footprint size of DVP or the solution not completely filling the feature, leaving the corners/edges undoped. By designing the process such that the source and drain could underlap the gate region, that ensures that current will be able to flow across the channel under forward bias conditions.

Second, the thermal budget needed to be limited after the MLD diffusion steps. Any processing >700°C would cause additional dopant diffusion, which is undesirable. This resulted in the choice of PECVD oxide as the gate oxide, and densification of that oxide at 600°C instead of a higher temperature.

Third, the possibility of junction spiking needed to be minimized. Metals used for contacts, especially aluminum, can often form unwanted silicides at the interface of the metal and silicon. With an ultra-shallow junction, this silicide could potentially consume all of the doped silicon in the contact region, causing a short. By creating an intentional silicide in the contact regions with a thin layer of nickel, which has one of the lowest silicon consumption rates (1.81 nm of NiSi formed per nm of Ni deposited[5]), this ensures that the diffused layer will not be completed consumed.

Fourth, to improve contact resistance and electrical characteristics, the sheet resistance of the source and drain needed to be low. To lower the sheet resistance,

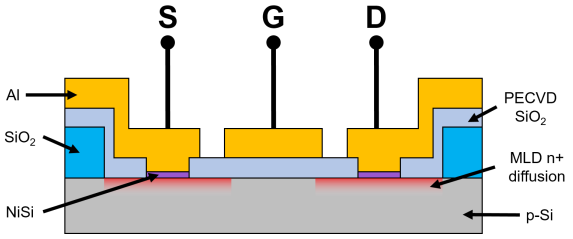

Figure 4. Final cross-section of MOSFET with MLD doped source and drain showing materials used and approximate geometry.

the anneal time can be increased or the dose can be increased. Increasing the anneal time also increases the junction depth, which was not desirable for this fabrication process. Increasing the dose is possible by repeating the MLD process after it has already been capped, annealed, and etched. The first MLD process is referred to as a single MLD, and the repeated process is referred to as a double MLD process. This decreases the sheet resistance without significantly increasing the junction depth as increasing the anneal time would.

The final device cross-section with materials and approximate geometry is shown in Figure 4, and the process flow used to fabricate these dievices is illustrated below in Figure 5.

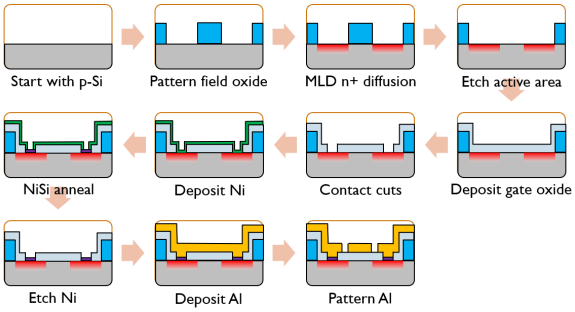

Figure 5. MOSFET fabrication process flow

3.3 MOSFET Mask Design

A four level mask design was created to be compatible with the previously developed process flow. An example transistor layout is shown below in Figure 6. Each device was designed using λ-based design rules, where λ is 10 μm. Each feature size was set by the design rules except the gate length, which was varied between 0.5, 1, 2, 5, and 10 μm.

The first level is the field oxide pattern, creating the source and drain regions. The second level is the active area clear, which removes the spacer between the source and drain and also the capping oxide from the MLD process. The third level is the contact cuts, and the fourth level is the metal lines. The design included

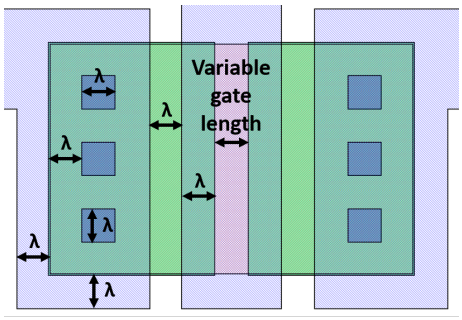

Figure 6. Mask design for a transistor with length of 10 μm and width of 70 μm showing design rules.

transistors of varying gate lengths and widths and resistors of various shapes and sizes.

4. RESULTS AND ANALYSIS

4.1 Characterization of Monolayer Doping

The MLD process can be characterized using sheet resistance measurements. The sheet resistance measurements were taken with a four point probe. A four point probe has four probes equally spaced in a line, passing a current through the central two probes and measuring the resulting voltage with the outer two probes. The current and voltage readings can be converted to sheet resistance using Equation 1. This equation gives accurate results assuming that the substrate being measured is infinitely large compared to the probe spacing.

$$R_S = \frac{\pi}{ln(2)} * \frac{V}{I} \quad (1)$$

Sheet resistance was measured for samples that underwent single and double MLD processes. The first sample was a piece of silicon, approximately 1 by 2 cm. This sample was used to extract the bulk sheet resistance values. The second sample was a patterned device wafer. The numerical values measured on the patterned wafers are not valid due to the measured area dimensions being on the same order of magnitude as the probe spacings. Instead, the trends and uniformity of measurements across the wafer are considered. Average sheet resistance values for all samples and conditions are listed in Table 1 below. For both the piece and patterned wafer, the sheet resistance decreases after the double MLD step, as expected.

Table 1. Average sheet resistance for MLD doped samples.

	Piece, R_S (Ω/□)	**6" wafer, R_S (Ω/□)**
Single MLD	1058.8	2189.0
Double MLD	769.6	1646.1

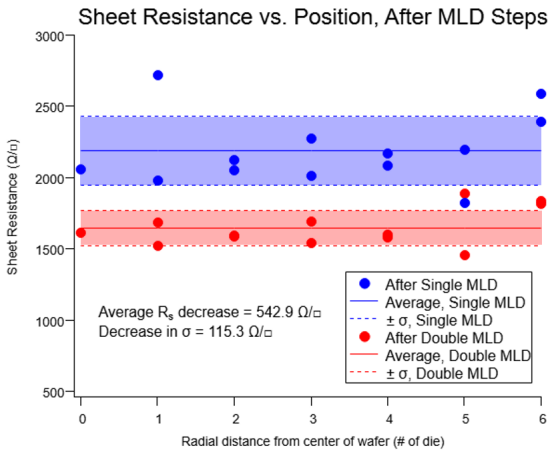

Figure 7. Sheet resistance measurements for single and double MLD steps on a patterned 6" wafer, plotted vs. position relative to the center of the wafer.

The individual data points for the patterned wafer are plotted above in Figure 7. The data points generally fall within one standard deviation of the average value for both single and double MLD, and there does not appear to be any positional dependence of the sheet resistance values. The standard deviation for the double MLD measurements is also smaller, indicating that the second process increased the uniformity.

4.2 Electrical Device Characterization

Once the fabrication process was finished, the devices were characterized electrically. Due to an over-etch of the source and drain areas created by the first lithography level, the 0.5, 1, and 2 μm gate length devices were not functional. The 5 and 10 μm gate length devices were measured.

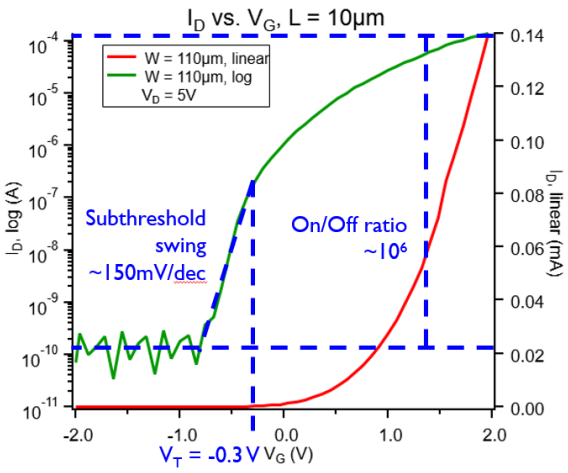

Figure 8. Transfer characteristics of a transistor with gate length of 5 μm, width of 110 μm.

Figure 8 shows the transfer characteristics of a transistor with gate length of 5 μm and a width of 110 μm. The transistor shows field effect behavior, with a threshold voltage of -0.3 V, a subthreshold swing of roughly 150 mV/dec, and an on/off ratio of 6 orders of magnitude.

Other transistors measured showed similar characteristics, with threshold voltages generally between -1.5 and -0.5 V. An NMOSFET would typically have a positive threshold voltage, but by using aluminum and the gate electrode and not doing any threshold voltage adjustment doping, a negative threshold voltage in that range is reasonable.

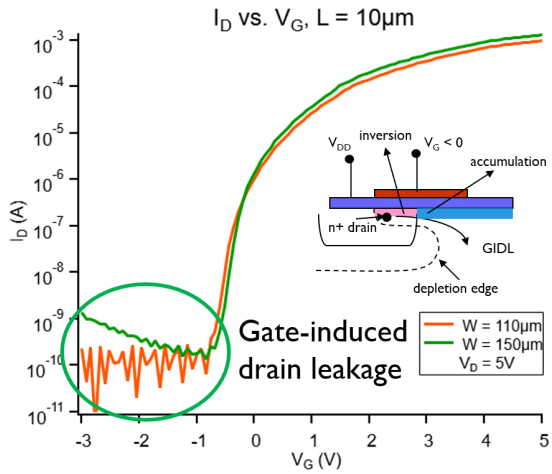

Figure 9. Transfer characteristics showing a device affected by GIDL (W = 110 μm) and a device unaffected by GIDL (W = 150 μm).

Some of the devices exhibited gate induced drain leakage (GIDL), as shown in Figure 9. GIDL occurs when the source or drain region underlaps the gate, and becomes inverted at voltages below the threshold voltage, causing current leakage. This is typically an undesirable effect, but in this case it demonstrates that the MLD source/drain doping did extend towards the edge of the features more than we compensated for, which is an important finding.

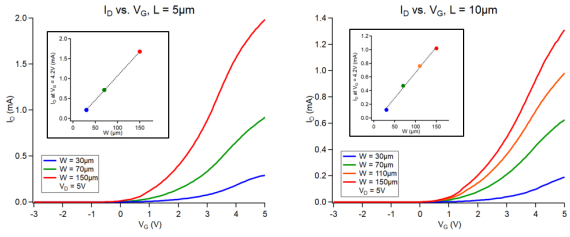

Figure 10. Transfer characteristics for 5 μm and 10 μm devices showing linear scaling of current with increasing width.

The devices also exhibited linear scaling of current as device width increased. This is shown in Figure 10 below for 5 μm and 10 μm devices.

Output characteristics reveal significant series resistance is present in the devices. Figure 11 below shows this effect. The pinching of the output curve at low drain biases for all gate voltages represents a series resistance barrier that the carriers must overcome for current to flow. The typical shape of output characteristics is shown with dotted lines for each curve.

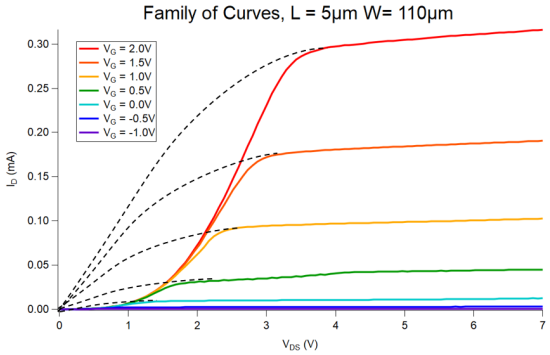

Figure 11. Output characteristics for 5 μm length and 110 μm width device showing. Measured characteristics are shown with solid curves, and the expected characteristics are shown with dotted lines.

The series resistance could be present due to a few potential issues. Resistance was expected to be higher than a typical deep junction device due to the high surface concentrations and shallow junction increasing the sheet resistance. However, the significant increase in resistance most likely originates from the contacts. This is further suggested by measurement of resistors on the wafer, showing pinching of current at low biases instead of a linear increase of current. There are several explanations for increased contact resistance. First, if there is oxide in the contact cuts, implying that the contact cuts did not completely clear. Second, if the nickel oxidized before it was annealed and did not form a silicide. Third, if the nickel was not deposited or completely removed by the piranha, and the aluminum deposited formed a silicide during the sintering process and spiked the junction. In future work, the exact cause could be determined.

5. CONCLUSIONS AND FUTURE WORK

MOSFETs with source and drain doped via MLD were successfully designed, fabricated, and characterized. The ability of MLD to dope areas patterned with SiO_2 was demonstrated. A new economic chamber design to complete the MLD process was also designed and tested

successfully. The devices showed high series resistance. In future work, the robustness of the contact process can be improved, as well as reducing overetch of the source and drain patterning to increase device yield. A higher quality gate oxide (potentially ALD deposited hi-k dielectric material) could also be used to improve device characteristics.

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