Fabrication of MOSFETs on InGaAs with Al_2O_3 Gate Dielectric

36th Microelectronic Engineering Conference

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Overview

- Motivation
- Goal
- Mobility of III-V Materials
- Process Flow
- Mask Design
- Process Characterization
- Device Fabrication
- Electrical Results
- Conclusions

Motivation

- InGaAs high electron mobility compared to Silicon (10,000 cm^2/V*s vs 1,400 cm^2/V*s) this can lead to a boost in drive current at .5V power supply.
- Past fabrication of III-V MOSFETs used the University of Rochester's ALD tool for the deposition of Al_2O_3 - Full fabrication process done at RIT.

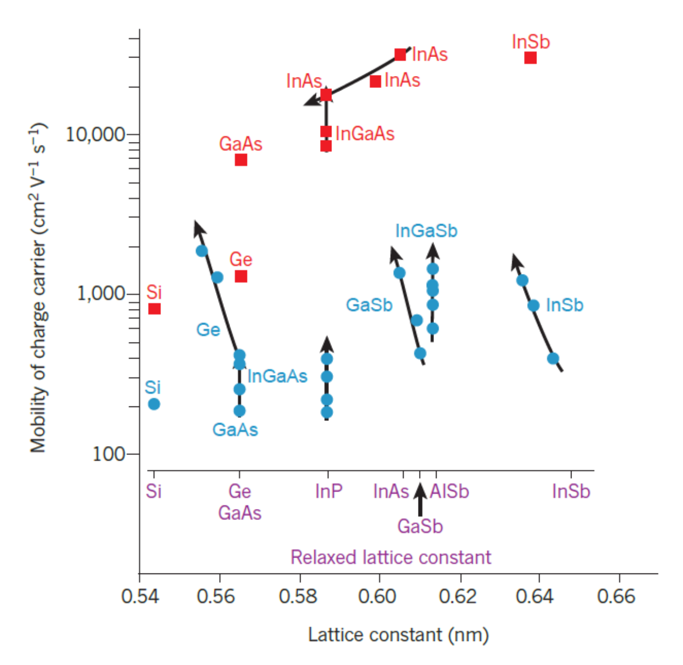
Goal

- **Fabrication of MOSFETs on InGaAs**

  - Fabricate Capacitors on Si with Al_2O_3 dielectric using RIT's ALD Tool and analyze CV.

  - Develop and characterize process for device fabrication.

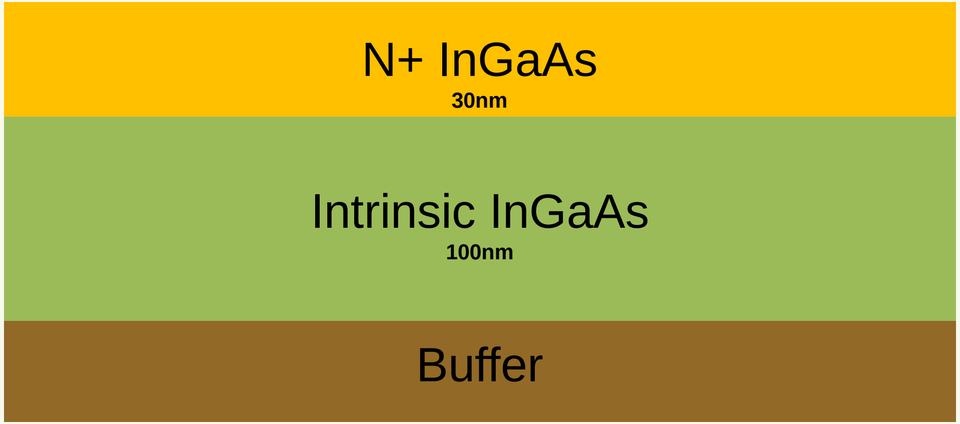
Mobility of III-V Materials



- III-V Materials have higher electron mobilities than Si.
- Drive current is directly affected by mobility.
- Manufacturing costs of these materials much greater than that of Si, more defects, and higher stress and strain.

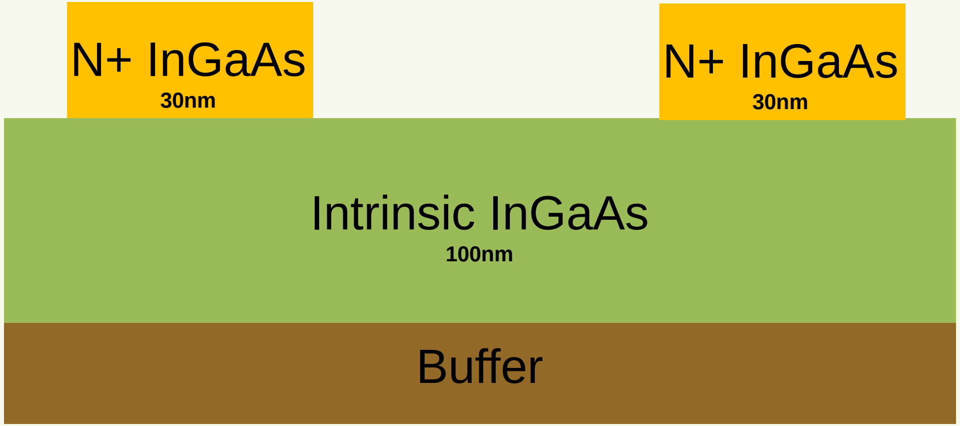
J. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors", *Nature*, vol. 479, no. 7373, pp. 317-323, 2011.

Process Flow
Starting Material Stack



Process Flow

Mesa Etch 20:20:1 Citric Acid:DI Water:H_2O_2



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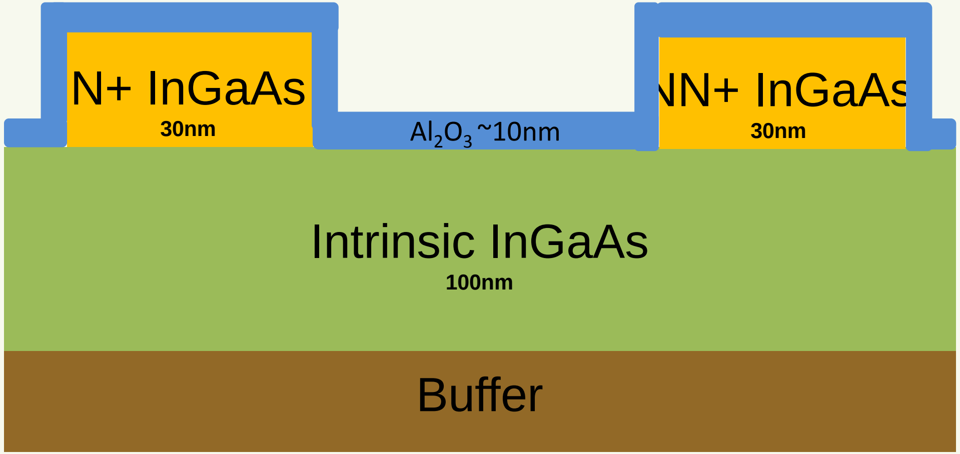
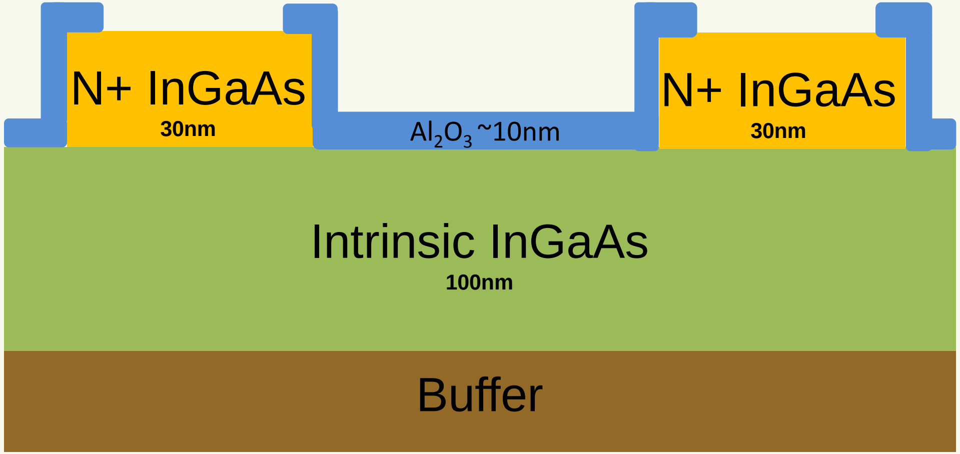
Process Flow

Al_2O_3 Deposition by ALD – 100 Cycles

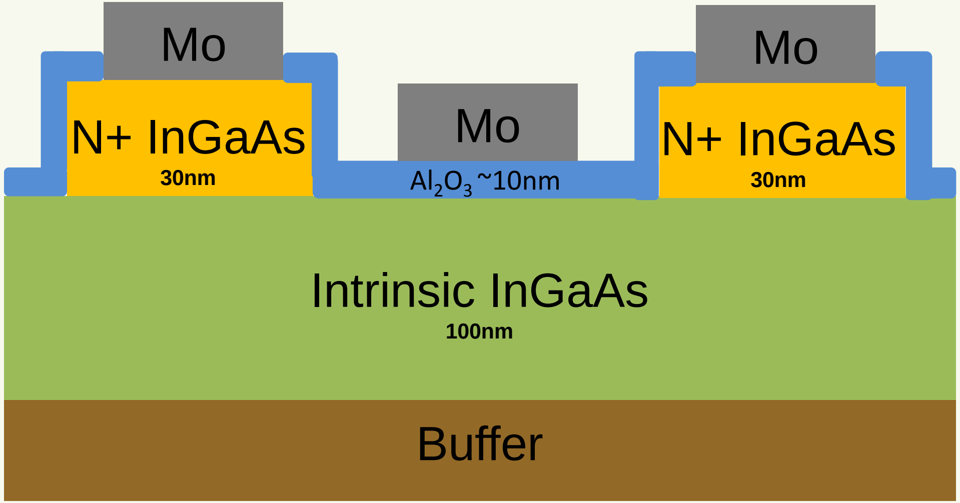


Process Flow
Al_2O_3 Etch 100:1 HF:DI Water

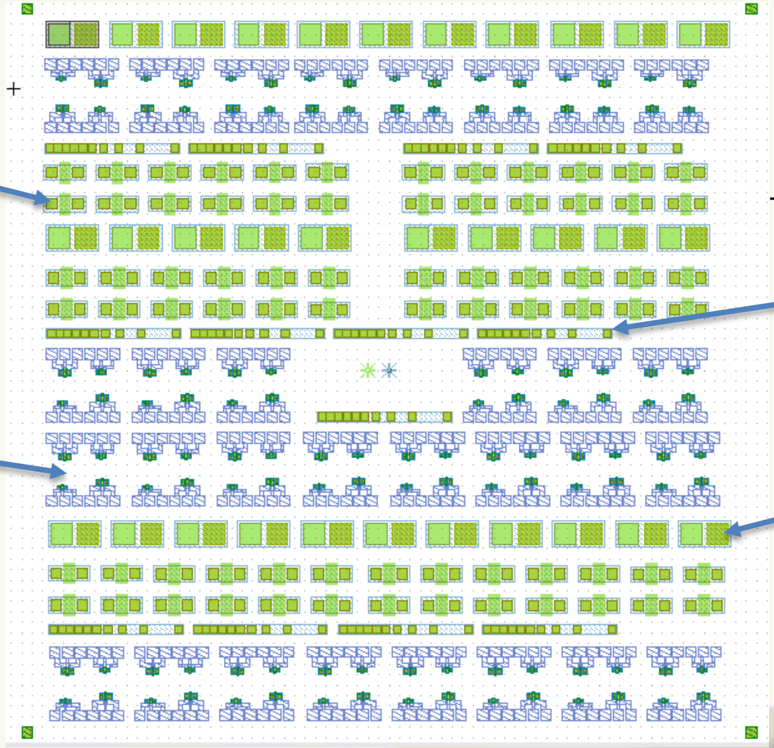


Process Flow

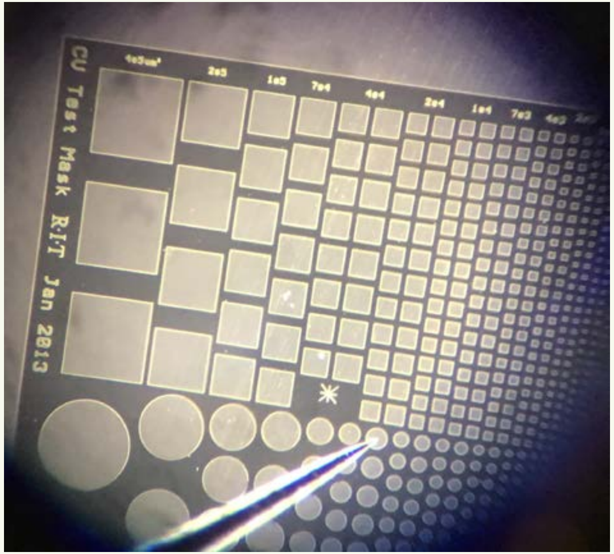
Deposition of Mo and Patterning with Lift Off

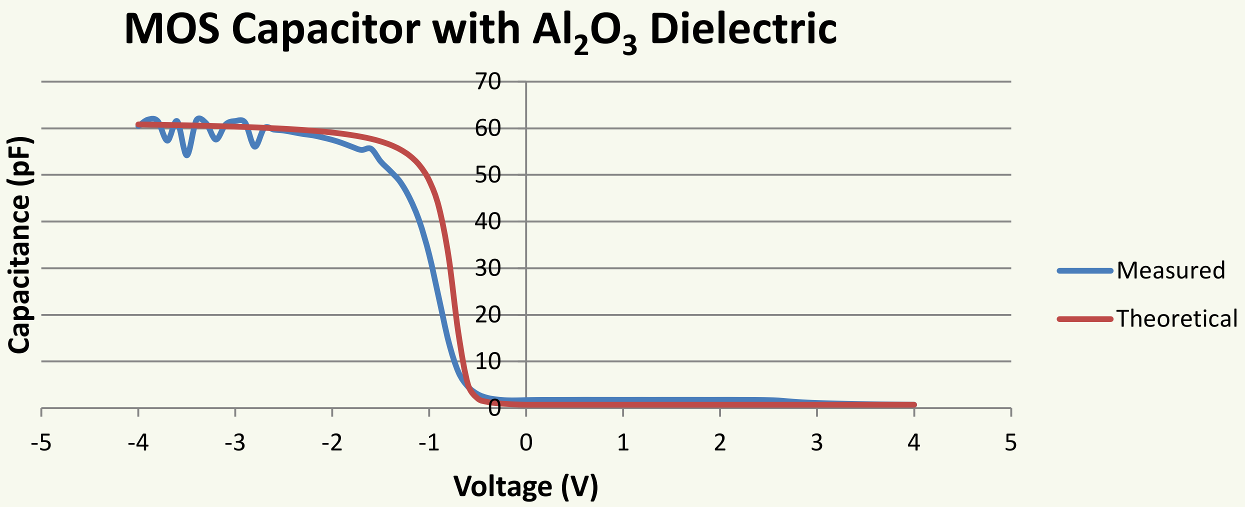


Mask Design Layout



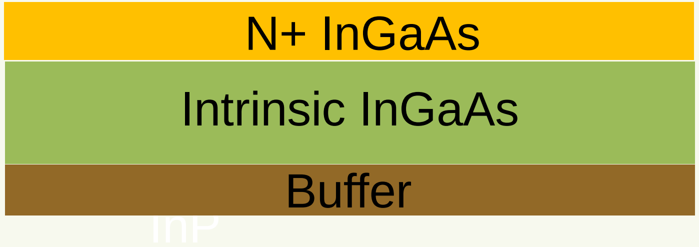
Characterization of Al_2O_3 with MOS Capacitors on Si

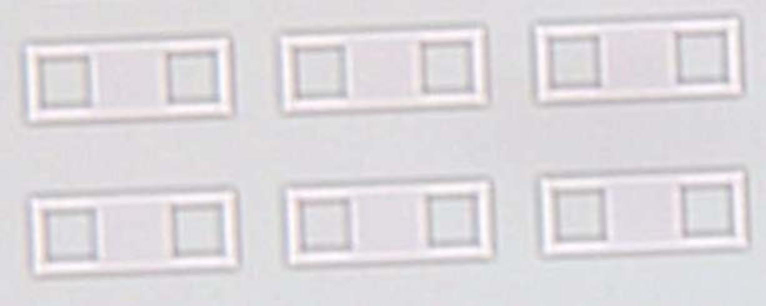




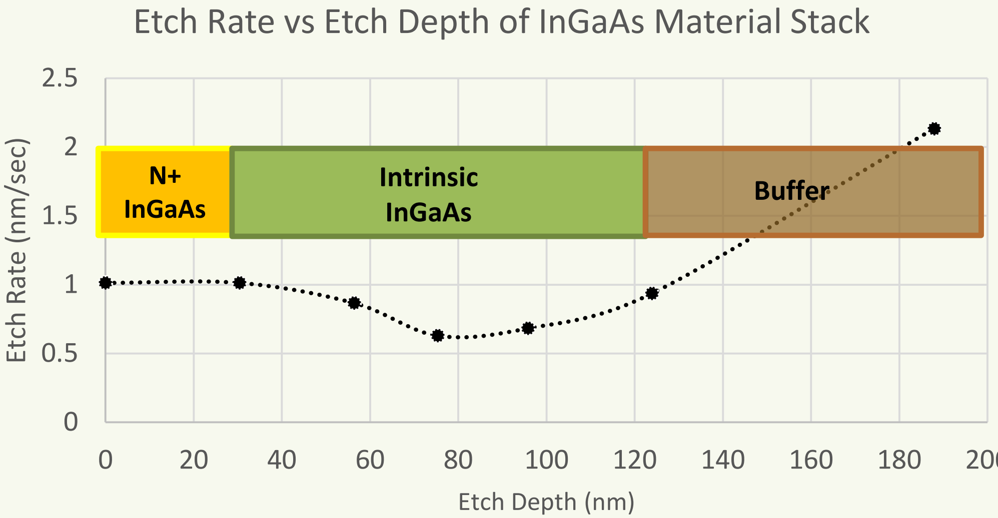
T_{ox} : 12.8nm
Relative Dielectric Constant ε_r: 9.01

20:20:1 Citric Acid:DI Water:H_2O_2 Etch Rate as a Function of Doping





Etched Mesa down to Intrinsic InGaAs

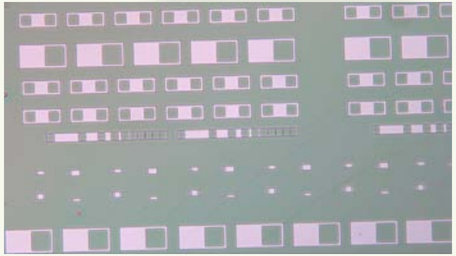


N+ InGaAs Etch Rate: ~1nm/sec

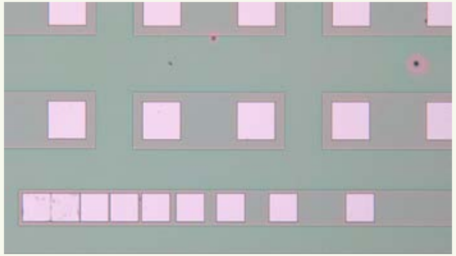
Lithography Challenges

- GCA Stepper was used for photolithography.
- Pieces were used for fabrication.
- Substrate is thicker than Silicon wafers. Requires different focus.
- Manual Alignment must be done for each lithography level.

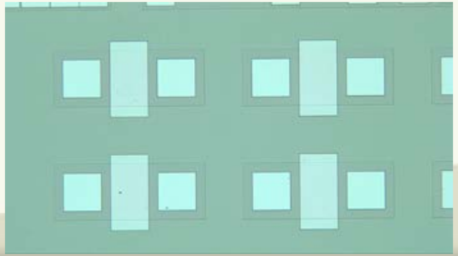
Level 1



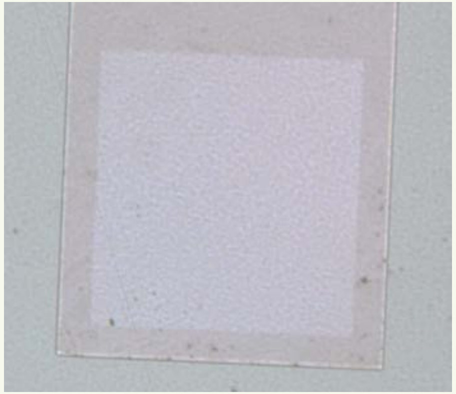
Level 2



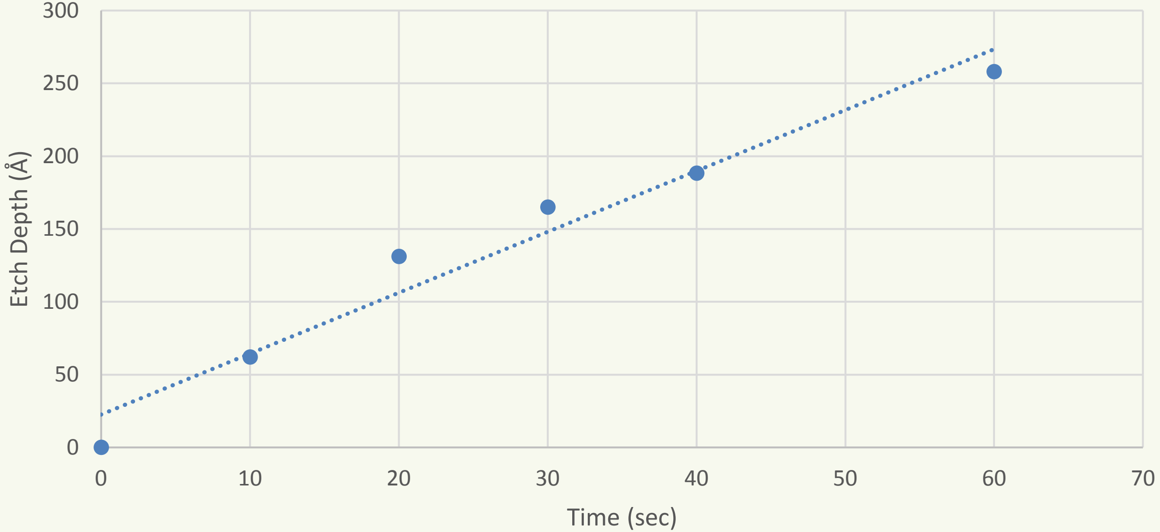
Level 3



Al_2O_3 Etch Characterization

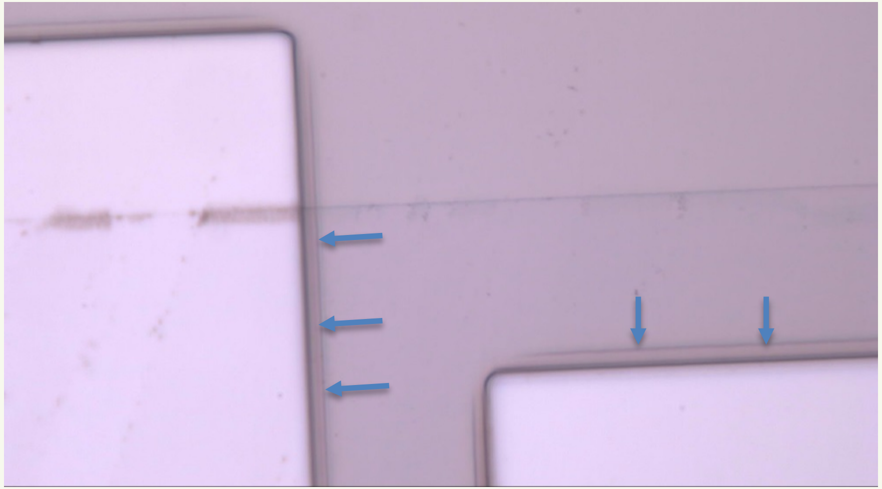


Etch of Al_2O_3 can be seen down to InGaAs layer

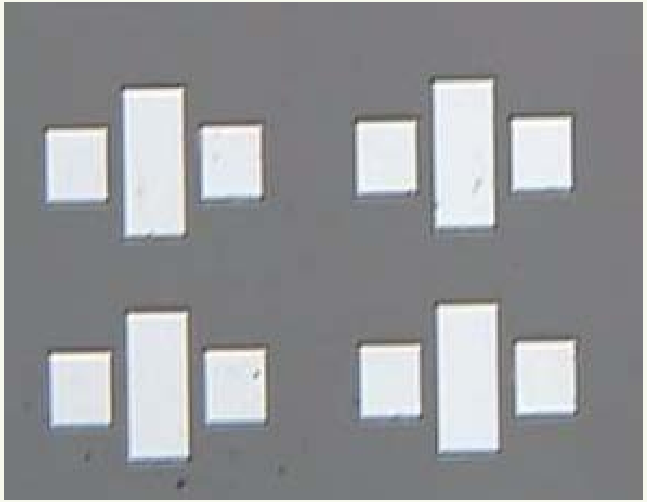


Etch Rate: ~4Å/sec

Characterization of Lift Off Process

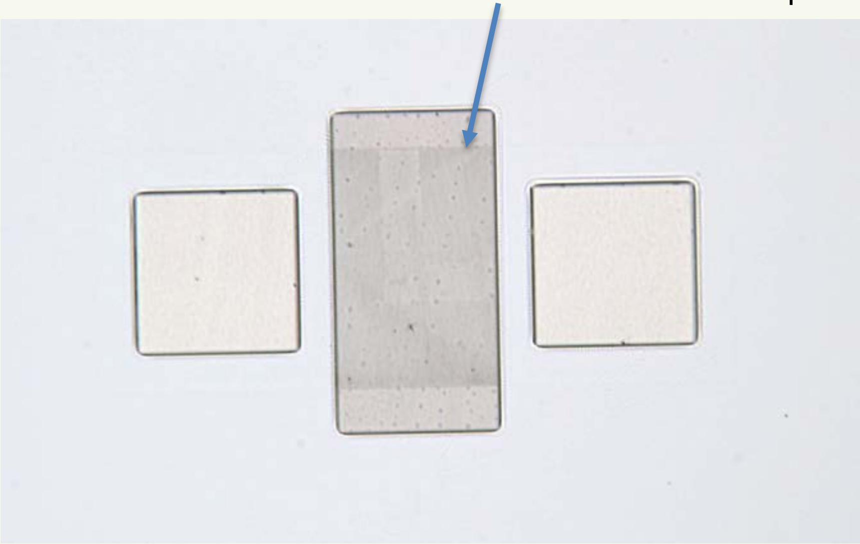


Undercutting of LOR 5A can be seen underneath HPR504 Photoresist

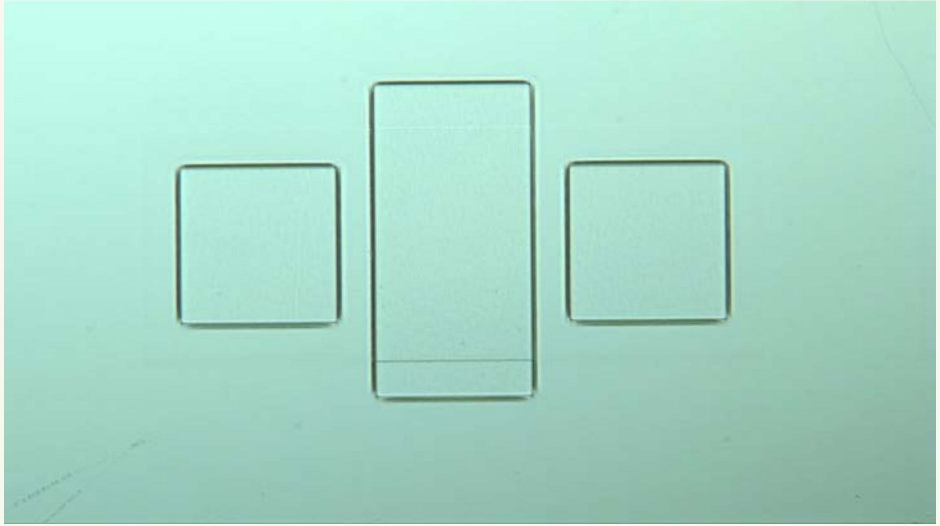


Desired pattern achieved after Lift Off

Molybdenum Deposition

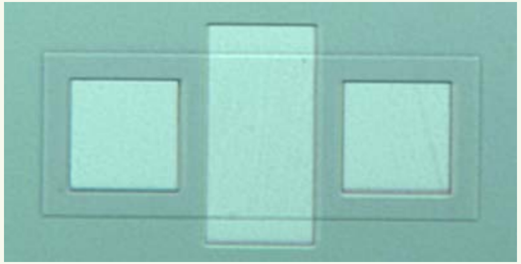


Molybdenum Deposited with E-Beam Evaporation

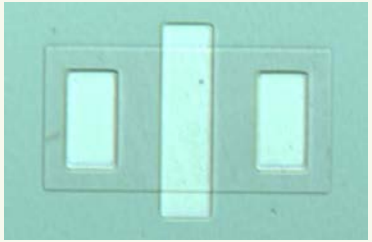


Molybdenum Deposited with Sputtering

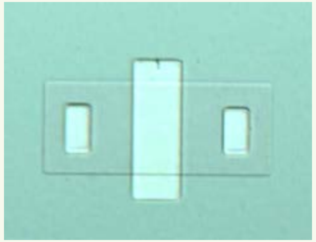
Finished Devices



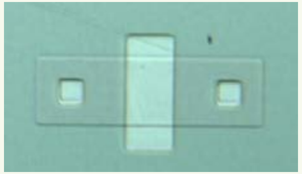
W: 150µm
L: 100µm



W: 60µm
L: 20µm



W: 40µm
L: 20µm



W: 30µm
L: 20µm

Electrical Results

- Testing of MOSFETs showed devices act like resistors.
- Fencing from lift off process paired with tight design rules lead to contact metal reaching down to the channel.
- Gate was found to be isolated from the Source/Drain.

Metal can be seen coming over the edge of the N+ InGaAs region

Conclusions

- Smaller features for the Source/Drain contacts should be used in the future to help prevent shorting.
- Depositing Mo using E-Beam Deposition requires further characterization. Decreasing the total mass of material inside the boat could provide better results.
- Sputtering Mo is viable for a lift-off process. Thick LOR is needed due to how conformal the film is from sputtering.
- Fabrication of an InGaAs MOSFET is achievable through the use of RIT's SMFL tools alone.

Acknowledgements

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