Fabrication of MOSFETs on InGaAs with Al_2O_3 Gate Dielectric

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I. Project Objectives

Goal: To characterize MOSFETs on InGaAs

- Analyze CV of capacitors on Si with Al_2O_3 dielectric
- Develop and characterize process for fabrication of MOSFETs on InGaAs
- Demonstrate gate control of MOSFETs

II. Motivation

- Past fabrication of III-V MOSFETs used UR's ALD tool for the gate dielectric deposition.
  - Full fabrication process done at RIT SMFL
- InGaAs high electron mobility compared to Silicon (10,000 $cm^2/V*s$ vs 1,400 $cm^2/V*s$) can lead to a boost in drive current.
- Need to show gate control for InGaAs MOSFET
  - Gives confidence in designed structure for future development and optimization of fabrication process.
  - Verification of correct materials chosen for device

III. MOSFET Operation

- For enhancement mode N-Channel devices, when there is no voltage applied to the gate, the channel region does not conduct.

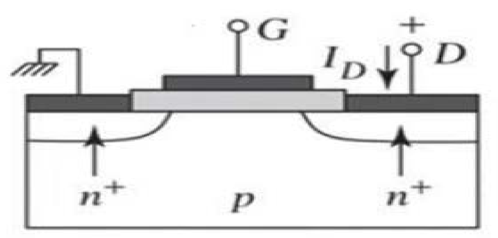

Figure 1. N-Channel MOSFET [1]

- When a positive voltage is placed on the gate, the channel region is inverted, and the device will conduct current.

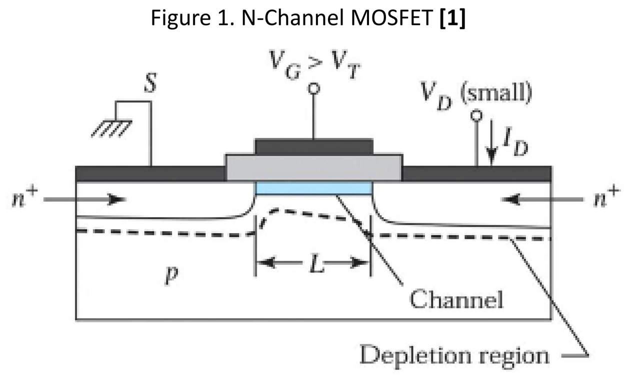

Figure 2. Inverted channel region of N-Channel MOSFET due to applied gate voltage [1]

- Higher electron mobility (μ) leads to increased drive current for a given gate voltage (V_{GS}).

$$I_D = \mu C_{ox}\frac{W}{L}(V_{GS}-V_T)V_{DS}, \text{ for } |V_{DS}| << (V_{GS}-V_T)$$

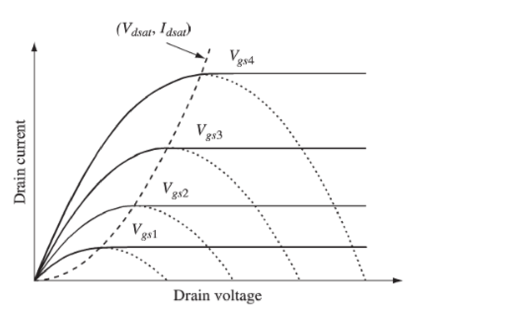

Figure 3. ID-VGS Curve for Enhancement Mode N-Channel MOSFET [2]

IV. Experimental Results

Device Structure

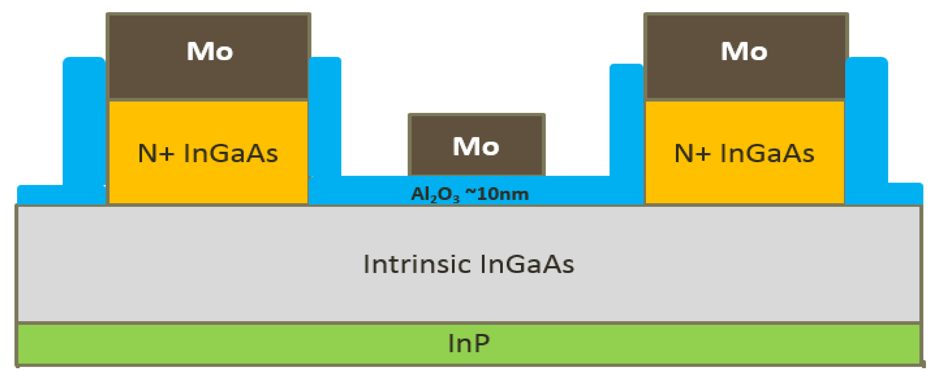

Figure 1. Cross Section of Desired InGaAs MOSFET

Fabrication Process

- 30nm InGaAs Etch with 20:1 Citric Acid:H_2O_2
- Deposition of 10nm Al_2O_3 by ALD
- Al_2O_3 etch with 100:1 HF:DI Water
- Deposition of Molybdenum using Electron Beam Deposition
- Patterning of Molybdenum via Lift off Process

Process Design

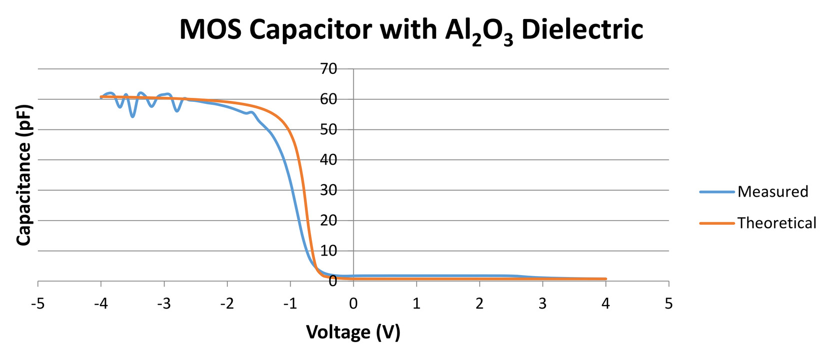

Figure 5. CV Curve of MOS Capacitor with Al_2O_3 Dielectric

Cox (pF)	61.9
Tox (Å)	128.8
Area (um^2)	1.00E-04
Cinv (pF)	.734
Winv (μ)	1.4
Nsub ($/cm^3$)	3.53E+14
Cfb/Co	.0715
Vfb (V)	-0.589
Vt (V)	-.0444
Φms (V)	-0.878
Nss ($/cm^2$)	-1.12E+12

Figure 6. Measured Parameters for MOS Capacitor with Al_2O_3 Dielectric

- MOS Capacitors were fabricated with a Al_2O_3 dielectric using ALD
- Capacitors were electrically tested to ensure proper operation of device

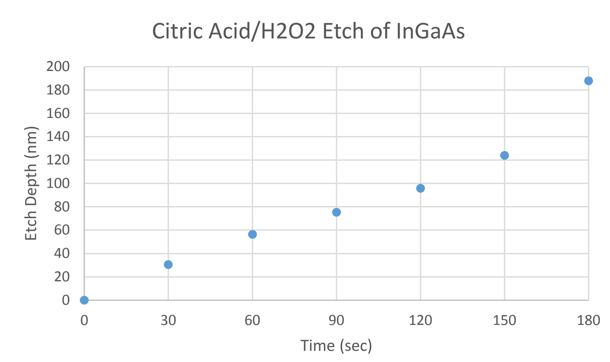

Figure 7. Etch Rate of InGaAs

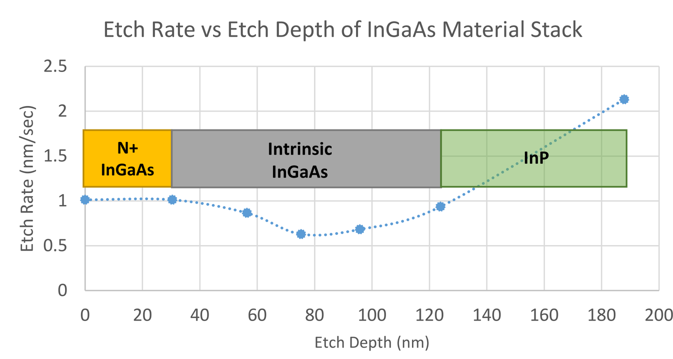

Figure 8. Change In Etch Rate with Differently Doped Materials

- Change in etch rate verifies structure composition

- InGaAs etch rate verified for Mesa etch
- N+ InGaAs Etch Rate ~ 10Å/sec
- Intrinsic InGaAs Etch Rate ~6.3Å/sec

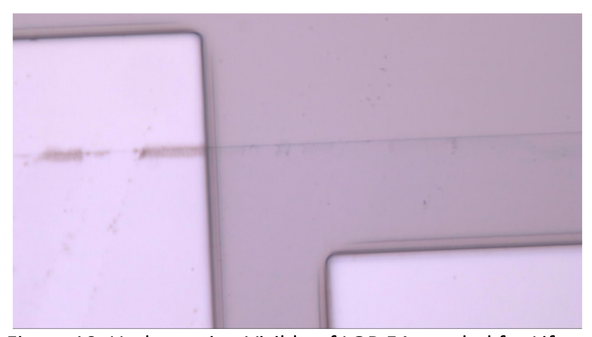

Figure 10. Undercutting Visible of LOR 5A needed for Lift Off Process

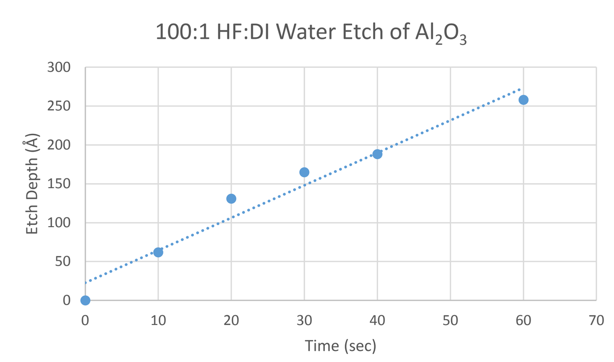

Figure 9. Etch Rate of Al_2O_3

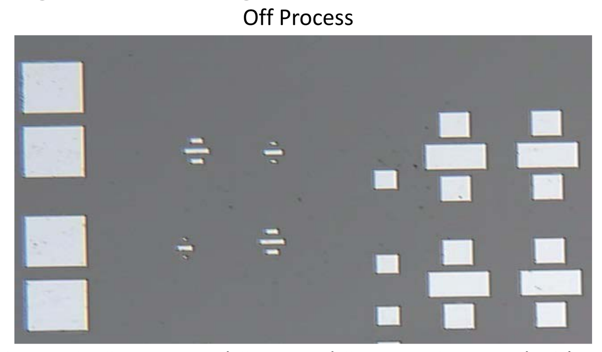

Figure 11. Contacts and Gates and Contacts Patterned with Lift Off with Al

- Al_2O_3 Etch test to ensure proper contact between Mo/N+ InGaAs at Source/Drain
- Al_2O_3 Etch Rate ~4Å/sec

- Application of LOR 5A and HPR 504 characterized to ensure proper lift off

Results (con't)

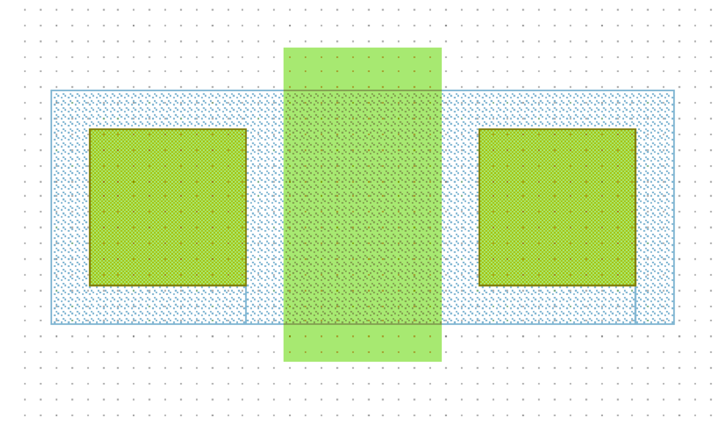

Figure 12. Layout of MOSFET for Mask Design

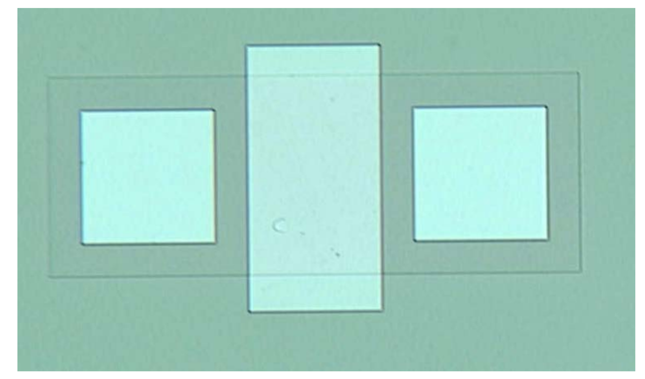

Figure 13. Third Level Lithography for MOSFET for Lift Off using manual alignment

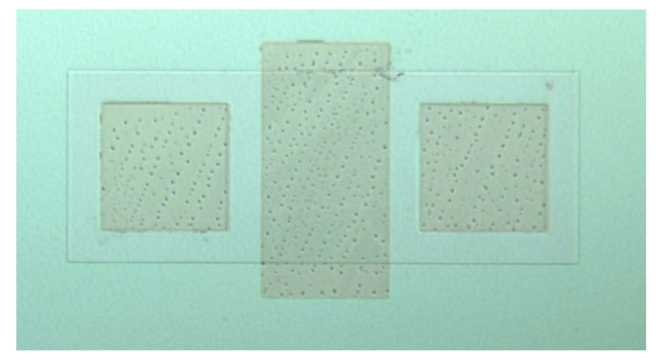

Figure 14. MOSFET After Lift Off including Etched Mesa, Al_2O_3 Deposition and Contact Cut

- Mo deposition using E-Beam Evaporation had problems
- Highest deposition rate achieved .08Å/sec
- Only ~290Å deposited before no more deposition could be achieved

V. Conclusions

Challenges in the deposition of the gate metal and contacts stopped the project short of being able to electrically test. Sputtering the Mo in order to form the gate and contacts seem preferable to E-Beam Evaporation.

Future Work

- Use Sputtering to apply gate metal/contacts
- Test Electrically
- Fabrication Process Optimization
  - Optimization of Gate Oxide Thickness
  - Investigate use of other Gate Metals

References

[1] S. M. Sze and M. K. Lee, Semiconductor Devices, Phys. and Tech., 3rd Ed., Fig. 5.26, pp 188, 2012

[2]Taur and Ning, Fundamentals of Modern VLSI Devices, 3nd Ed., Fig. 3.6, pp 159, 2009

Acknowledgements

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