Fabrication of MOSFETs on InGaAs with Al_2O_3

John Colern, Dr. Sean Rommel

ABSTRACT

The goal of this project was to fabricate MOSFETs on InGaAs with an Al_2O_3 gate dielectric deposited with ALD. The initial structure of the device was planned out, the process was designed, and then each step of the process was characterized prior to the fabrication of the devices. The devices were fabricated, and then electrically tested. Each of the separate processes were shown to be repeatable and accurate. Errors with design rules in the mask layout led to shorting of the devices from source to drain, however the gate was found to be electrically isolated.

1. INTRODUCTION

Silicon has dominated the world of the semiconductor industry since the beginning of the technology. Silicon wafers are cheap to mass produce in comparison to other semiconductor materials. However, as the technologies push forward and higher performance is necessary for devices, researchers are beginning to look more and more at the usefulness of other semiconductor materials. One of these materials in InGaAs. It is a III-V semiconductor grown epitaxially to form single crystal structure wafers. One of the stand out advantages of a material like InGaAs is it's very high electron mobility and unusually large ratio of electron to hole mobility. The room temperature electron mobility for InGaAs approaches 10x10^3 cm^2/V*s, while that of Silicon is only 1400 cm^2/V*s. This higher mobility means that the current carrying capacity of transistors made with InGaAs is higher, the response time of photodetectors is faster, and the series resistance is lower. This can all lead to an improvement in device efficiency as well as reduces noise and power consumption.

2. THEORY

As the scaling of transistors continue under Moore's law, modern logic circuits have reached a limit in power density. The power density on these chips cannot increase much further without increasing packaging as well as cooling costs to make the chips practical. This means that the operating voltage will need to decrease for transistors as they become smaller and chips become more dense. One school of thought to how to fix this problem is the use of group III-V semiconductors. Figure 1 shows the electron and hole mobility of different semiconductor materials as well as Silicon for comparison.[1]

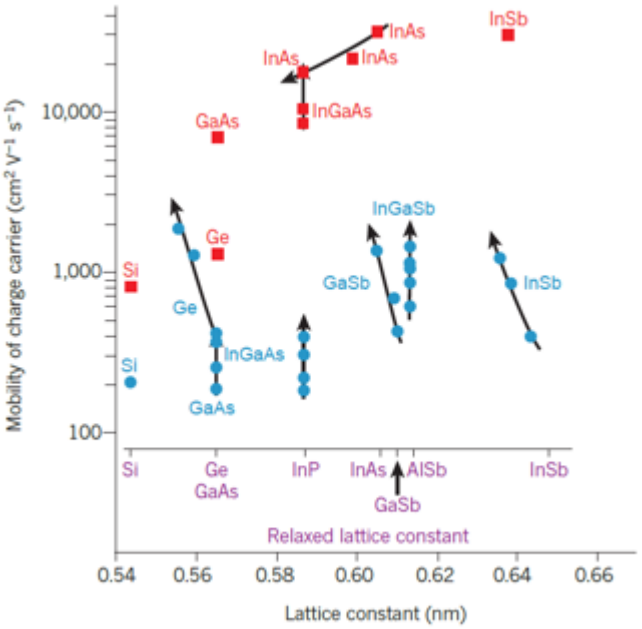

Figure 1. Electron and Hole Mobility of III-V Semiconductors [1]

As seen in Figure 1, the electron mobility of InGaAs is 10 times higher than that of Si. Drive current in a transistor is directly affected by electron mobility. As mobility increases, the drive current also increases at a given voltage, requiring an overall lower drive voltage to reach the same current levels, lowering power consumption. However, there are some challenges to using group III-V semiconductor materials in production. In Figure 1 it can be seen that mobility increases in a material as the lattice constant increases. A higher lattice constant will introduce greater stress and strain into the material, as well as an increase in defect density. The cost of manufacturing III-V semiconductors can also be limiting. Instead of growing large single crystal ingots

John Colern is a student at Rochester Institute of Technology in the Department of Electrical and Microelectronic Engineering.

Dr. Sean Rommel is a professor at Rochester Institute of Technology in the department of Microelectronic Engineering.

like those done with Si, III-V semiconductors like InGaAs, must be grown using epitaxy. This also means the throughput in a manufacturing environment would be significantly lower.

3. PROCEDURE

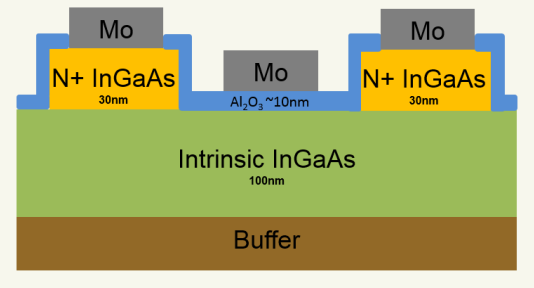

Figure 2. Cross Section of InGaAs MOSFET

A general process flow for the fabrication of the MOSFETs, shown as a crossection in Figure 2, were laid out. First, an etch of the InGaAs would be done in order to form the mesa as well as the raised source and drain regions. Then, the entire device would be coated with Al_2O_3 via ALD. The Al_2O_3 would then be etched away completely over the source and drain. Finally, Molybdenum would be deposited onto the device and patterned using a lift off process. Each of these steps need to be fully characterized before used to fabricate a device. A series of experiments were conducted in order to characterize each process.

First, a series of MOS capacitors were fabricated on Si using ALD for the deposition of Al_2O_3 as the dielectric, with a target thickness of 10nm, the same as in the MOSFET. The film thickness was measured post deposition to ensure the thickness was on target, and then the capacitors were electrically tested in order to extract the relative dielectric constant. Next, pieces of the InGaAs used for fabrication were used and etched with a 20:20:1 mix of Citric Acid:DI Water:H_2O_2 at varying times. The thickness loss was then measured and plotted in order to find the etch rate. The etch rates were also plotted versus the depth into the substrate to verify the change in dopant concentration through the structure. A thicker film of Al_2O_3 was deposited and etched for varying times with 100:1 HF:DI water. The thickness loss was plotted against time and the etch rate of the dielectric was extracted. Recipes were tested for creating the stack needed for the lift off process, the stacks were exposed, developed and analyzed under a microscope in order to verify proper undercutting of the lift off resist that was required. A lift off process was completed using the stack as well to achieve the desired metal pattern. Following characterization of each process, the devices were then fabricated and electrically tested.

4. RESULTS AND DISCUSSION

The first step prior to fabrication of the devices, was the design and characterization of each of the fabrication processes. The first process to be characterized was the deposition of Al_2O_3 using ALD. A target thickness of 10nm was chosen, and the ALD was run using 100 cycles. MOS Capacitors on Si were then fabricated using Al_2O_3 as the dielectric. The thickness of the dielectric was measured using ellipsometry and found to be 12.8nm with 100 cycles. An image of the capacitors made is shown in Figure 3 below.

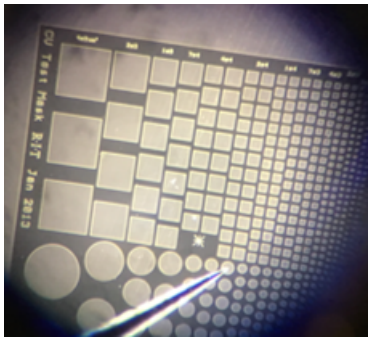

Figure 3. MOS Capacitors on Si under a microscope at 20x

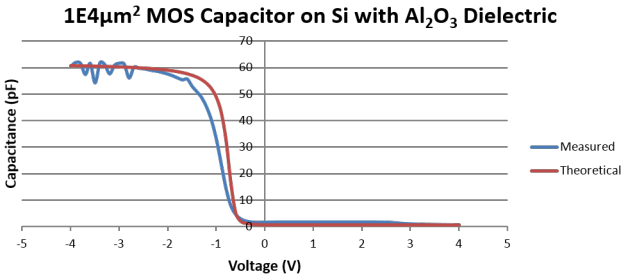

Figure 4. CV Curve of Fabricated MOS Capacitor

After fabrication the devices were electrically tested and CV curves were generated in order to extract oxide thickness, t_{ox}, for confirmation in the measured thickness, as well as the relative dielectric constant, ϵ_r. From the generated curve, t_{ox} was found to be 12.8nm again, confirming our findings, and ϵ_r was found to be 9.01. This value of ϵ_r matched findings in literature and was satisfactory for the needs of the process.

Following characterization of the dielectric deposition, the etch process of InGaAs for the mesa etch

was characterized. A 20:20:1 mix of Citric Acid:DI Water:H_2O_2 was put together and used for the etch. This chemistry's etch rate is known to be dependent on the dopant concentration of the InGaAs. This means that during the test to find the etch rate, the etch rate can be monitored as it etches through the material, to verify the thickness of the different regions of the starting structure, which can be seen in Figure 5.

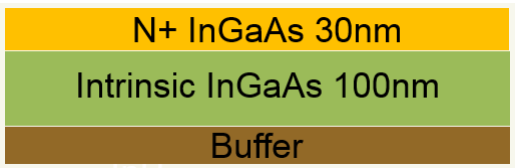

Figure 5. Beginning Structure of InGaAs Substrate

A group of samples of the InGaAs were etched for varying lengths of time. The etch rate was then calculated in between each point, and then those etch rates were plotted against the current etch depth. The reported thicknesses of the different layers were then laid over the plot to visualize the change in etch rate through the structure, and can be seen in Figure 6. The area interested in being etched is the N+ InGaAs, and the etch rate in that region was found to be 1nm/sec.

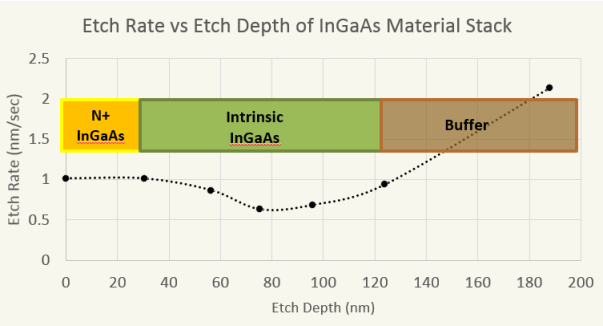

Figure 6. Change in Etch Rate Dependent on Dopant Concentration

One of the biggest challenges in the fabrication process was during the lithography steps. Due to the high cost of InGaAs, smaller pieces of the materials were used instead of full wafers. Because of this, a GCA Stepper was used as it is the only stepper in the SMFL capable of exposing pieces. The first challenge for the lithography step was that the substrates being used in this process are thicker than normal Si wafers. This means that the focal plane needed adjustment in order to properly image. However due to using small pieces, a focus exposure matrix was out of the question. This meant that many exposures had to be done, adjusting the focus manually each time, then the resulting image was evaluated after development under a microscope. An additonal challenge with using the GCA stepper came down to the alignment, which is done manually. A pair of joysticks are used, paired with a camera with a crosshair on it, to match to the alignment marks on the piece. Many hours of trial and error finally led to sufficient ability for good alignment. Figure 7 shows images taken with a microscope of the different lithography levels showing good alignment.

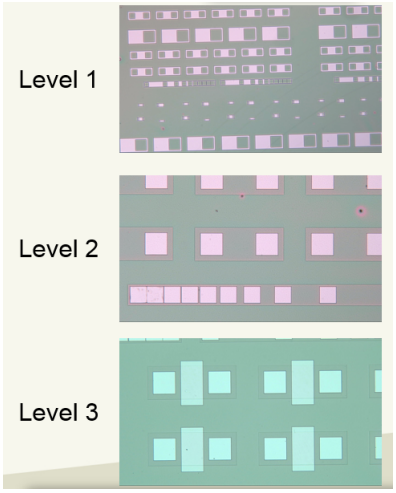

Figure 7. Alignment Shown of Different Lithography Levels

With alignment of the different mask layers under control, the etch rate of the Al_2O_3 was characterized. A 100:1 mixture of HF:DI Water was used for the etch. 30nm of Al_2O_3 was deposited using ALD, then etched with the diluted HF for varying times and the thickness loss was measured. These results were then plotted, Figure 8, and an etch rate of 4Å/sec. Figure 9 shows an image taken of the Al_2O_3 etched away from the source and drain region of the MOSFET.

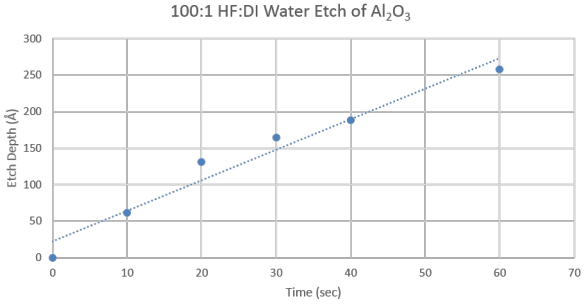

Figure 8. Etch Test Results of Al_2O_3 with 100:1 HF:DI Water

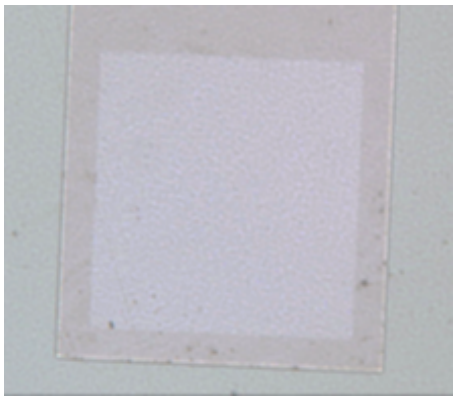

Figure 9. Al_2O_3 Etched Away from Source and Drain Region

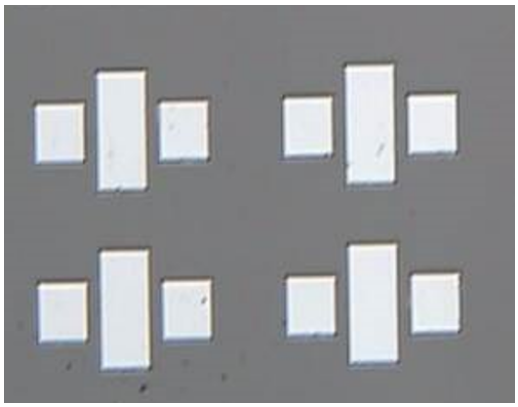

Figure 11. Metal Patterned with Lift Off Process

The next process to be characterized was the lift off process. LOR5A was used as the lift off resist underneath HPR504, the photoresist. In order to ensure proper patterning of the metal, undercutting of the LOR5A must occur at the edges of the pattern, and the metal layer deposited must be no more than 40% of the LOR5A layer. Spin speeds and times were adjusted for the correct thickness, with reference to the LOR5A data sheet, the stack was exposed, and then developed. Following development the patterns were analyzed under a microscope in order to look for undercutting. After a few trials good undercutting was observed and a recipe was chosen. An image showing the undercutting is seen in Figure 10. Metal was then deposited over the resist stack, and the resist was lifted off leaving the desired pattern, shown in Figure 11.

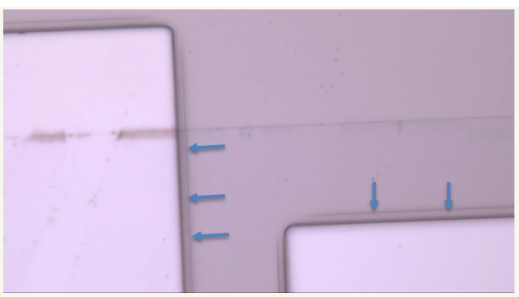

Figure 10. Undercutting of LOR5A

For the deposition of Molybdenum (Mo), E-Beam evaporation was chosen. Mo's boiling point is too high for resistive thermal evaporation, and films deposited via sputtering are very conformal, which can cause issues for lift-off processes. However attempts to deposit Mo using E-Beam evaporation fell short. Mo's boiling point increases quickly as pressure increases. The Mo used in the deposition outgassed heavily. This made it, paired with the large mass of the material, too difficult to get hot enough to evaporate. The film deposited was so thin it was still transparent, and filled with pinholes, and can be seen in Figure 12.

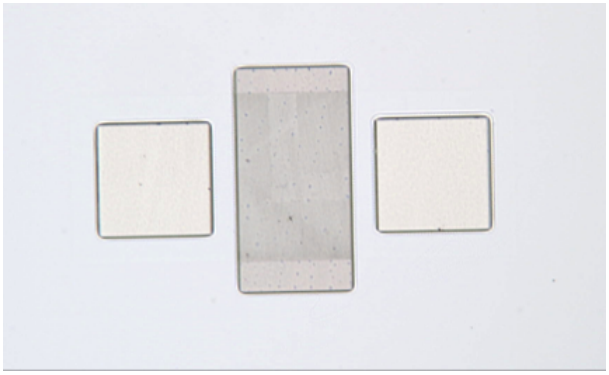

Figure 12. Bad Film of Mo from E-Beam Evaporation

Due to time constraints E-Beam evaporation with Mo couldn't be further characterized. Instead sputtering was used even if it wasn't the best option. Figure 13 shows a much better quality film.

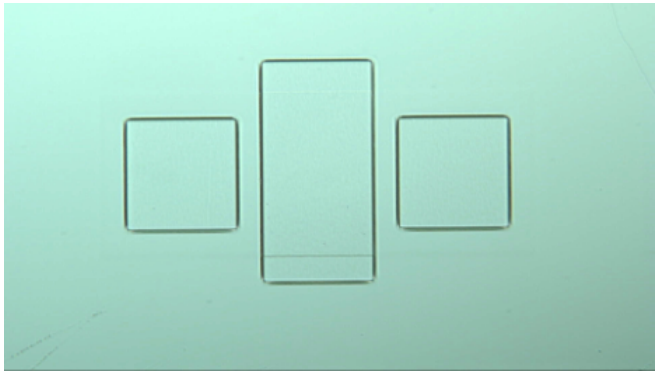

Figure 13. Film of Mo Deposited with Sputtering

The LOR5A layer's thickness was increased to try and compensate for the conformal film, and the lift off process worked with the sputtered film. This resulted in finished devices, shown in Figure 14.

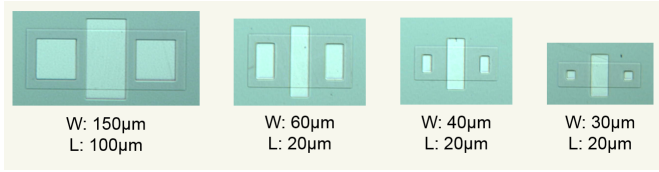

Figure 14. Finished InGaAs MOSFETs

With the devices fabricated, they were then electrically tested. The gates were shown to be electrically isolated from the drain and source. However, the results showed that all of the devices were shorted from the source to the drain. This was found to be due to the metal Mo contacts reaching down from the source/drain to the intrinsic InGaAs region, shorting the device. This was caused by improper design rules for the metal contacts, paired with fencing due to sputtering. An image showing the metal reaching over can be seen in Figure 15.

Figure 15. Mo Reaching from N+ InGaAs to Instrinic InGaAs

5. CONCLUSIONS

Errors in the initial design of the mask layout, paired with fencing from using sputtering with a lift-off process, led to the shorting of the fabricated devices. In the future, larger design rules for the metal contacts should be used for the layout. Sputtering was shown to be a viable choice for lift-off processes, however, E-Beam evaporation of Mo in the SMFL should be further characterized. Even though the devices were shorted from source to drain, the gate was electrically isolated from the rest of the device. This leads the author to believe that a viable process for the fabrication of InGaAs MOSFETs using only the tools available at the SMFL was designed and that fixing the mask design issue should lead to working devices.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

[1]J. del Alamo, "Nanometre-scale electronics with IIIV compound semiconductors", Nature, vol. 479, no. 7373, pp. 317-323, 2011.