MEMS Fabrication of a Peristaltic Pump

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ABSTRACT

From Merriam-Webster dictionary, it states that peristalsis can best be described as "successive waves of involuntary contraction passing along the walls of a hollow muscular structure (such as the esophagus or intestine) and forcing the contents onward"[1]. The objective of this project was to create a peristaltic micropump at the Rochester Institute of Technology (RIT) Semiconductor and Microsystem Fabrication Laboratory (SMFL). Using Micro-Electro-Mechanical Systems (MEMS) to create a peristaltic pump to lower the energy used to move a fluid through a tube. Using three single micromachined micro-pumps in a straight line to create this type of action. Fabrication was done on 4 inch silicon substrates that were plasma etched use STS Plasma etcher.

Keywords: Peristalsis, Micropump, Silcion, MEMS

1. INTRODUCTION

In roughly 1978 the first micro-pump was created. A singular micro-pump will be created using micromachining. In the project design, multiple pump sizes were made to try and optimize results. Peristaltic micro-pumps can be used for numerous reasons ranging from blood sampling, drug delivery systems, and movement of minute amounts of fluids. The usage of this device varies, just like the type of pump changes. A few examples of micro-pumps are electrostatic, thermo-pneumatic, piezoelectric, and electromagnetic. The basis behind this design, uses a piezoelectric style of pulsing. In the testing phase, a mechanical press will be used, though in the future Lead Zirconate Titanate (PZT) a piezoelectric materialwill be used to actuate the pump.

2. THEORY

2.1 Displacement

Using a sealed incompressible fluid inside of the pump, allows the membranes of the pump to displace the fluid in the device. Fomblin oil was used as the incompressible fluid. Displacement is simply the movement of something, in this case fluid, from one area to another.

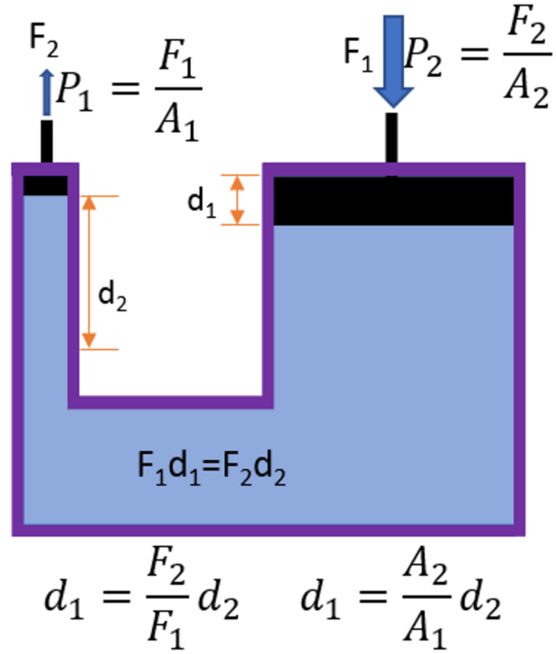

Figure 1: Displacement Theory.

Viewing figure 1, it shows that the force (F) applied on the larger membrane will create a small displacement (d) of fluid. The number 1 represents the larger membrane of the pump where the number 2 is deemed as the smaller membrane.

$$Pressure = \frac{Force}{Area} \quad (1)$$

The pressure being placed on this membrane will be mechanical in the first stage of testing, while a PZT material will later be used to actuate the membrane. Maximum amount of pressure to be placed on the large membrane is 100 kPa. If more pressure is used, there will be a great chance of breaking the membrane.

Displacement theory amplifies the bend of the smaller membrane. This causes a multiplication property to occur. A small displacement of membrane 1, will cause a large displacement of membrane 2 due

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to the condensing of the chamber where the fluid will be pushed. In this project the membranes are designed to be circular while other shapes may be an option. Area of a circle is:

$$A = \pi r^2$$

A = area and r = radius (2)

After substituting into the equations shown in figure 1, the output displacement can be found by using:

$$d_2 = \frac{A_1}{A_2} d_1 \quad (3)$$

The ratio of the membranes areas times the displacement of the actuating membrane will show the resulting displacement.

2.2 Peristalsis

As previously stated, peristalsis is the wave like motion created by the lining of the intestines that moves material forward. In this project, the membrane act as the muscle pushing and retracting to pinch the micro-tubing. The micro-tubing allows the fluid to flow linearly over the membranes. The membranes are made out of an oxide layer that was thermally grown. This infused the oxide with the silicon wafer.

Creating the peristaltic pump comes from three micro-pumps in series with one another. The large chamber was 3 mm in diameter while the small chamber was 1 mm. In the figure 2 it shows a diagram of the what it will look like from the top down. This shows the micro-tubing over the smaller membranes.

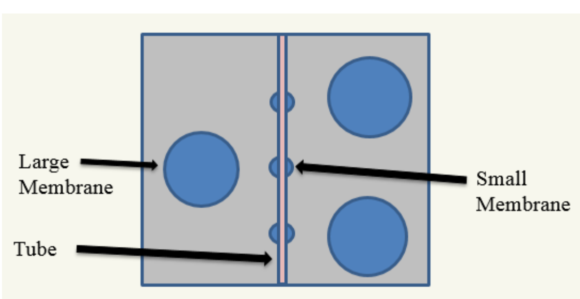

Figure 2: Top down view of a Peristaltic pump

The large membranes have to alternate sides on the chip. This allows the peristaltic pump to work. While the pump is actuating, nL of fluid will be pushed through the system.

The purpose of using a peristaltic pump is to reduce energy being used in the device. Other micro-pumps need a high voltage to create actuation and other mechanical devices to move the liquid forward. This energy reduction makes this device more ideal. In the beginning models, testing of the device will be done by a mechanical press, though the end goal is to use a piezoelectric material.

2.3 Piezoelectric Effect

The piezoelectric effect can best be defined as the mechanical stress placed on a material that creates an output voltage. This effect can all work in reverse, in this project that is desired. A voltage will be applied to a piezoelectric material; Lead Zirconate Titanate (PZT). This material will placed on top of the large membrane. When a voltage is applied to the material, it will deform hitting the incompressible fluid. That fluid uses the displacement theory to push upwards on the small membrane.

PZT is lead based, this is a concern depending on some of the devices this pump will be placed in. Some countries do not allow lead devices into their country due to the hazards. There aren't very many substitutes at the moment. More research is being conductive to find more piezoelectric materials that are environmentally friendly.

2.4 STS Plasma Etcher

In order to create the chambers and channels of the device, a STS Plasma Etcher was used. This etcher uses a plasma which comes from the gases flowing into the system. Once the gas atoms get ionized, a plasma is formed. This type of etcher etches Si. There are four main gases used in the plasma etcher; SF_6, C_4F_8, Ar, O_2.

Etching process is broken down into two steps, the first step is the passivation of the sidewalls which protects them. Followed by an etch process that ran for 7 seconds. The passivation runs for 14 seconds, an etch cycle takes 21 second for 1 micron of etching. This cycle goes back and forth until the number of cycles has been ran.

The wafer is backside cooled with Helium. In order to start etching, a helium leak check is ran to verify the wafer will not move and is clean enough to be etched. Max tolerance was 10 mT/min leak rate, anything above this would be kicked out. Cleaning of the backside is done by with acetone to remove resist or other particles.

3. EXPERIMENT DETIALS

This peristaltic micro-pump is a 3 layer lithography design, with an option for a 4^{th} layer. An extra photolithography step can be added to create vias in order to hold the membrane down. To begin fabrication of this design, wafers were needed; four inch wafers were used. No specific type of wafer was needed since bulk Si etching was done and the device didn't need to be doped.

At first, the wafers were cleaned using an RCA clean and placed into a thermal furnace were 1 μm was grown on both sides of the wafer. Wafers were coated with photoresist and baked. The first mask was directly contacted using a Suss MA150 Mask Aligner. The Suss Mask Aligner is a 1X direct contact machine that allows for i-line and g-line wavelengths. Mask 1 created the membranes of the device.

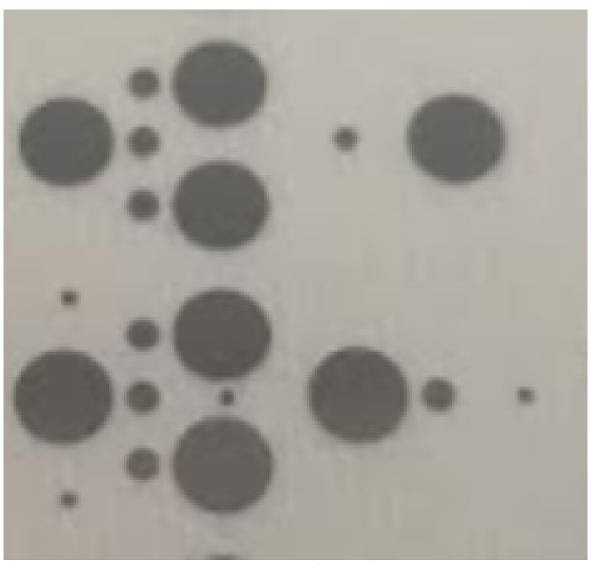

Figure 3: Mask 1 design.

After the exposure of the wafers, they were developed by hand using CD-26 developer for 60 seconds. Wafers were quickly removed from solution and rinsed with DI water. The wafers went directly into a BOE solution to remove the oxide layer that was just exposed. This oxide etch was conducted in order to create a hard mask. The resist was stripped and cleaned once again. Second mask layer was next, using mask 2 to create the channels of the device.

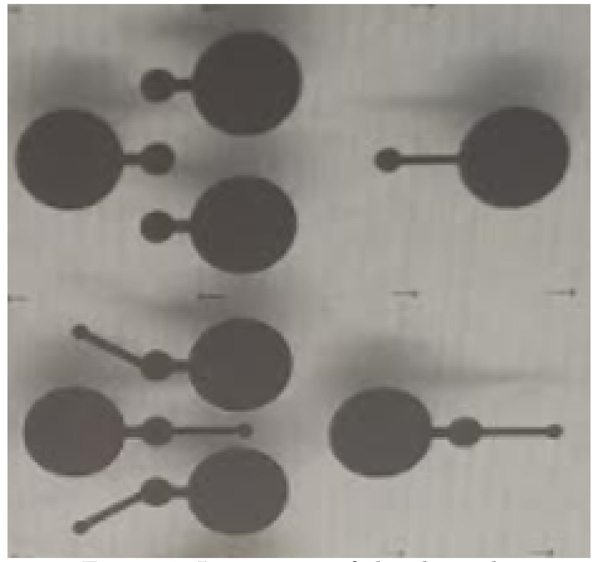

Figure 4: Integration of the channels.

Once the mask 2 was exposed and developed, the device wafer was bonded to a 6 inch carrier wafer using photoresist. The STS plasma etcher only accepts 6 inch wafers. The first etch was ran at 345 cycles to roughly etch $\frac{2}{3}$ of the way through the wafer. The four inch wafer was measured at roughly 533 μm thick. Once the etching was completed, the device wafer was removed from the carrier wafer. Heating the photoresist up to 140 °C, allowing the 4 inch wafer to slide off. An oxide etch was performed to create the channels. It was bonded to the carrier wafer once again to finish the etching process.

Etching all the way through wafer takes roughly 3 hours, since 533 cycles were ran using the STS plasma etcher. The membranes have been completed and the resist and oxide are removed. The device wafer is bonded using anodic bonding. Anodic bonding uses a hot plate, a mechanical clamp, and a high voltage to bond two wafers together. Placing the etched wafer on top of a bare wafer to close the device. A voltage of 400 VDC could be used to fuse the dangling bonds together.

After bonding the wafer, the third mask is used to open up the fluid ports and some small membranes depending on the chip design. The now top side of the wafer is coated with photoresist, exposed, and developed.

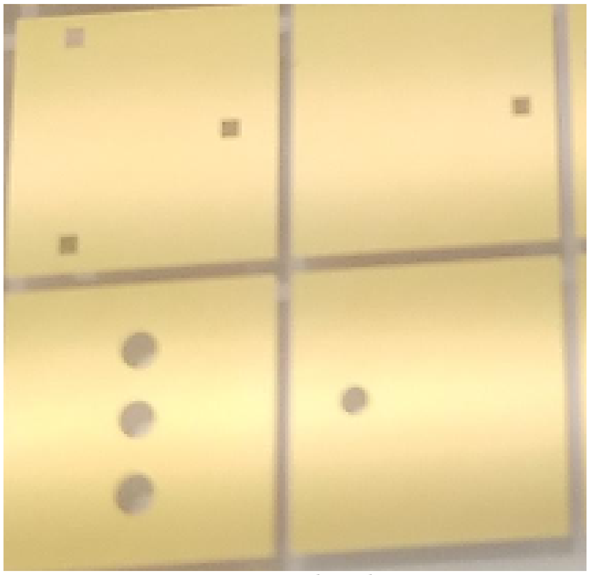

Figure 5: Mask 3 design.

The final clean room step is to use an oxide etch to open up the proper areas. After completion the device is filled with Fomblin fluid using a vacuum filling technique. This technique allows the device to be placed under vacuum and the fluid is introduced to the system. Once vacuum is broken the fluid goes into the device. The device is temporarily sealed using tape, then gets placed into the SMFL Parylene. This coats the wafer in a thin layer of parylene. The wafer is then sawed into 8 mm x 8 mm chips.

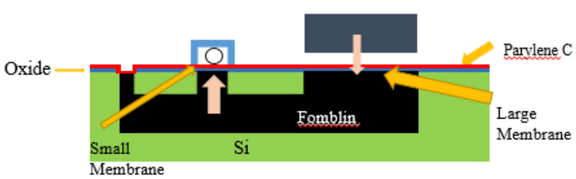

Figure 6: Cross section sketch of a micro-pump.

For final touches, the micro-tubing was placed over the small membrane and a small housing unit was placed over the tubing to help with compression of the tubing.

4. FABRICATION ERRORS AND RESULTS

Throughout the fabrication there were some errors discovered, these errors are crucial but solutions or other different methods have been found to solve the issues. The first issue was inverted masks for mask layers 1 and 2. This issue was created during the mask layer when the mask was made in a clear field when the mask needed to be a dark field. This dark field mask would have created the correct image. There are two possible solutions to this solution; remake the mask or use a negative resist. Since there were only a wafers, nLOF 2020 a negative was used.

When using the Mask Aligner, it was noticed that the alignment marks were no on the same plane. One set of alignment marks were higher on the y-axis compared to the other side. Use of theta to rotate the wafer was tried, though no luck was had. Solution to this was direct writing the layer use a Heidelberg DWL 66+. This is not a feasible solution though it worked short term. Finding the alignment marks took roughly 20 minutes and exposure took another 20 minutes. An overall 40 minutes was spent exposing a single level on one wafer.

Etching of the oxide was done in a 10:1 BOE etch bath when using a 5.2:1 BOE etch would of been better. The 10:1 took a roughly 20 minutes since it was thermally grown oxide and started to break down the photoresist barrier layer. After the oxide was etched, photoresist was spun on top of the wafer. This didn't spread evenly due to the 1 μm holes. A possible solution was to place extra resist towards the outside of the wafer and spin at a faster rotation per minute (rpm) rate.

Issues came up when using the STS Plasma etcher. One of the errors consisted with uneven etching of the silicon. The second error was found when the oxide and photoresist were removed during the etching. Both of these layers were suppose to be used as a hard masking layer. The third error was the debris found in the Si membranes shown in figure 7.

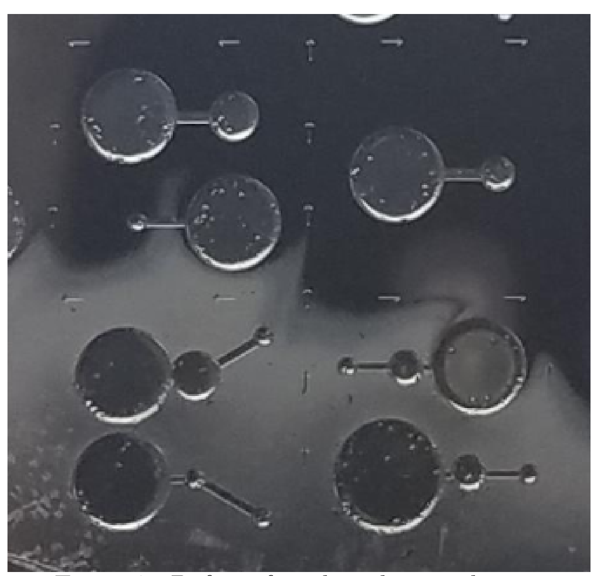

Figure 7: Defects found in the membrane.

A possible solution to the first error was to try and rotate the device wafer evenly until completion. This took time removing the wafer from the carrier wafer and rotating, then putting new resist on top and baking the device wafer on top of it. In order to solve the second issue of the hard mask removal, a few extra microns of PECVD oxide was deposited. This doubled the hard masking layer. Finally the third solution is to keep the wafer as clean as possible.

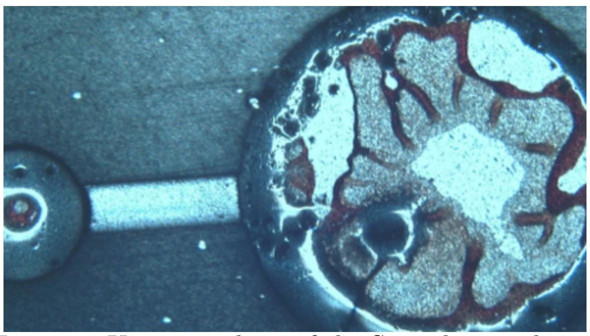

Figure 8: Uneven etching of the Si in the membrane

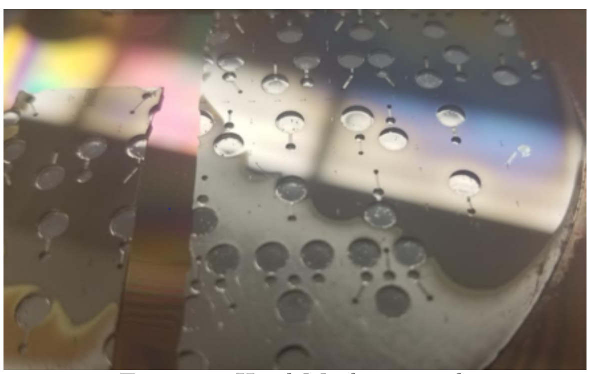

Figure 9: Hard Mark removal.

Figure 8 shows an almost etch membrane though there is still silicon in the center of the membrane. Figure 9 shows the uneven hard mask removal caused by the STS Plasma Etcher. This process was halted due to the STS Plasma Etcher, the etching was inconsistent. In order to continue the process the solutions above need to be implemented and solved. The STS Plasma Etcher needs to characterized in order to complete the process.

5. CONCLUSION AND FUTURE WORK

This project taught a lot about the errors that can occur and what occurs during fabrication. Though this project wasn't completely finished, more work will be made towards finishing it. This project has a lot of potential especially with its future work. Anodic bonding would be the first thing needed to be finished along with filling the device with Fomblin.

After testing the device using a mechanically device to press down 2-4 μm adding the PZT to control the device will replace the mechanical press. This will move the project forward, making it a realistic device that can be potentially used in devices. Testing of the micro-tubing closure in order to verify that nL amounts of fluid can be dispensed.

6. ACKNOWLEDGMENTS

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7. REFERENCES

[1] "Peristalsis."Merriam-Webster.com. Merriam-Webster, n.d. Web. 11 Apr. 2018.