Process Development Challenges Associated with Gallium Nitride Materials

Eric A. Evangelou

Abstract **—** While attempting to fabricate low resistance Ohmic contacts to n-GaN and n-AlGaN, processing setbacks necessitated the development of new procedures within the Semiconductor and Microsystems Fabrication Lab (SMFL) at RIT. Photoresist coating recipes usable on GaN pieces were developed for OiR-620 and LOR-5A photoresists, and GaN was etched for the first time on the LAM4600 reactive ion etcher (RIE). The etch was successful, etched GaN at a rate of 187.2 Å/min, and exhibited selectivity between GaN and hard-baked photoresist comparable to an inductively coupled plasma (ICP) etch of the same chemical makeup. An Ohmic Ti to n-GaN contact was fabricated, but was not optimized for low resistance due to time constraints. These processing solutions will enable future GaN-based projects in the SMFL.

Index Terms **— Gallium Nitride; GaN; Reactive Ion Etch; RIE; Transfer Length Measurement; TLM**

I. Introduction

For decades silicon has been the semiconductor of choice used in the manufacturing of integrated transistors. Its material system is well suited for a variety of applications, and years of scientific advances and industry development have made it by far and away the cheapest semiconductor to process. As the scaling of Si-based devices begins to near its physical limit alternative materials with superior electrical performance need to be considered if the development of new and improved power transistors is to be maintained for future device generations. To this end, there has recently been an increased effort in the development of production-ready III-V compound semiconductors.

Gallium nitride (GaN) is one such semiconductor that is rapidly developing as an alternative to Si in this field. GaN high electron mobility transistors (HEMTs) are a viable replacement for traditional Si RF devices, such as laterally diffused metal oxide semiconductor (LDMOS) transistors, because of GaN's superior characteristics in this area. GaN has a wider bandgap (~3.4eV), is capable of blocking higher voltages, has better thermal stability, and has a higher electron mobility than bulk Si [6][7].

In order for GaN-based RF and high power devices to achieve their optimal device performance, low resistance contacts need to be developed for the material system. At its outset, this project focused on the characterization of various metallization schemes in order to verify which is best for use as a contact on future GaN FETs developed at RIT. The goal was to make transfer length measurement (TLM) test structures to quantify the specific contact resistance of different metal stacks to n-GaN and n-AlGaN films. The processing of GaN is new to the Semiconductor and Microsystems Fabrication Lab (SMFL), and as such procedures needed to be developed before test structures could be fully fabricated. Due to limited time, the goal of this project evolved into developing reliable solutions to some of the processing challenges associated with GaN materials in the SMFL.

II. Theory

A. Transfer Length Measurement (TLM) Theory

TLM structures are an effective means of characterizing the contact resistance between a semiconductor and a metal. The structure is essentially a row of identical metal contacts spaced at varying distances from one another on a semiconductor surface. These contacts are then probed sequentially using a current source and a voltmeter, and the resistance measured from each set of contacts is plotted against the distance between them (see Figure 1).

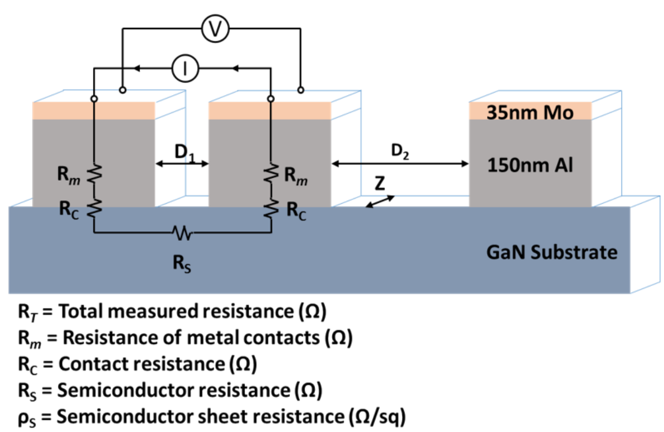

Figure 1 – A cross section of an example TLM being probed [5].

From this plot, the contact resistance of the contact can be obtained, as well as the sheet resistance of the semiconductor (see Figure 2). Additionally, the transfer length of the contact can also be derived from the x-intercept of the plotted line as well. The transfer length of the contact (L_T) is defined to be the average length that the current flows in the semiconductor beneath the contact pad before entering the contact itself.

Eric A. Evangelou is a student at the Rochester Institute of Technology in the Department of Electrical and Microelectronic Engineering.

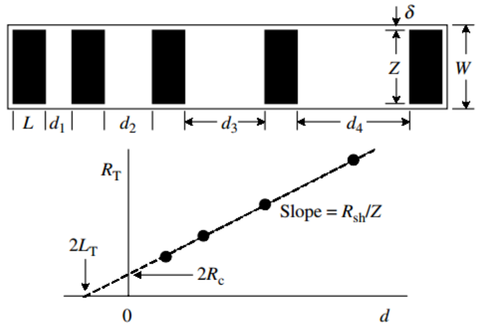

Figure 2 – An aerial view of a TLM structure labeled with the basic parameters necessary to derive the contact resistance, transfer length, and sheet resistance of the semiconductor [5].

In this simple model the total resistance measured (R_T) is equal to:

$$R_T = 2R_m + 2R_C + R_S \tag{1}$$

With the assumption that the resistance of the metal is negligible, and by putting the semiconductor resistance in terms of the semiconductor's sheet resistance (R_{sh}), the total measured resistance can be re-stated as:

$$R_m \ll R_S \; or \; R_C \tag{2}$$

$$R_T \approx 2R_C + R_S \tag{3}$$

$$R_S = \frac{D\, R_{sh}}{Z} \tag{4}$$

$$R_T = \frac{D\, R_{sh}}{Z} + 2R_C \tag{5}$$

For a more in-depth model of the current flow through these devices, see the discussion on TLM structures in Reference [5] by Schroder.

B. GaN Dry Etching Theory

GaN is a tough material to etch. The gallium and nitrogen atoms are ionically bonded to one another, and as such it has a higher bonding energy than silicon and other III-V semiconductors, which are typically covalently bonded [8]. GaN is typically etched through a combination of chemical and physical mechanisms. In a dry plasma etch, chlorine is used to chemically react with the gallium to form $GaCl_3$, while argon is used to physically sputter away the chemical product $GaCl_3$ and the GaN beneath it [3]. In a reactive ion etch (RIE) of GaN, higher RF power applied to the electrodes in the chamber will result in a smoother GaN surface after the etch is complete [3]. Additionally, keeping the chlorine gas concentration just below fifty percent of the total gaseous content in the chamber will result in the highest possible etch rate for the chamber, as it allows for the argon to sputter away the $GaCl_3$ at an optimized rate [3].

The dry etch for this project was to occur in the LAM4600, a reactive ion etcher traditionally devoted to the etching of aluminum thin films. In order to ensure that the byproducts of a chlorine-based GaN etch would not adsorb onto the chamber wall, the volatility of $GaCl_3$ was compared against that of $AlCl_3$ (see Figure 3). At the operating temperature of the LAM4600, $GaCl_3$ is more volatile than $AlCl_3$, meaning that it would be okay to etch the GaN in the same chamber without concern over its byproducts.

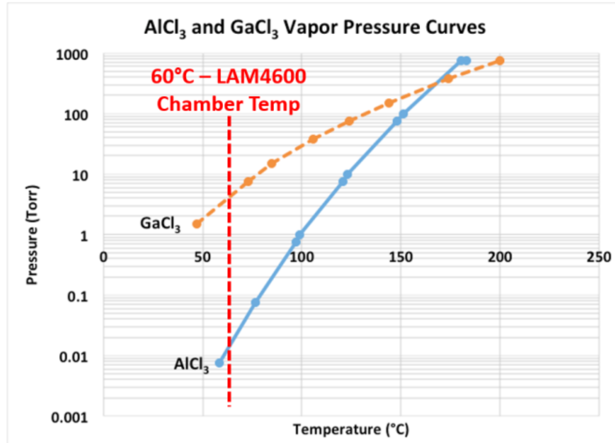

Figure 3 – The vapor pressure curves of GaCl3 and AlCl3. The LAM4600 operating temperature of 60°C is highlighted [2][4].

III. Fabrication Process

The following is a summarized version of the process flow for the fabrication of these TLM devices:

1) ***Sample Acquisition:*** Obtain GaN samples
2) ***Sample Preparation:*** Cleaving and cleaning of pieces
3) ***Mesa Level Lithography:*** Coat pieces with OiR-620 photoresist and expose them using mesa level mask
4) ***Mesa Etch:*** Dry etch mesas into the GaN film
5) ***Contact Cut Level Lithography:*** Coat pieces with LOR-5A and HPR-504 resists and expose them using the contact cut level mask
6) ***Metal Deposition:*** Deposit a different metal stack on each piece via an electron beam evaporation process
7) ***Metal Liftoff:*** Liftoff the unwanted photoresist and metal on each piece in a remover base using an ultrasonic bath
8) ***Rapid Thermal Anneal:*** Anneal each piece at 600°C for thirty seconds
9) ***Electrical Characterization:*** Test each piece and verify the contact resistance for each metal stack

Fabrication of the TLM structures began with the acquisition of GaN samples. The SMFL does not have metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) processes that can grow GaN films, therefore materials needed to be obtained from outside sources. Donated GaN materials were obtained from Texas Instruments (TI), Veeco, and RIT alumnus Brian Romanczyk (UCSB).

Samples were then prepared for subsequent processing steps. The six inch GaN-on-Si wafer donated by TI was cleaved with a diamond scribe into several $4cm^2$ pieces, which were then cleaned with acetone and dipped in a 50:1 hydrofluoric acid bath for a minute to remove native surface oxides. Immediately afterwards the pieces were coated with OiR-620 positive photoresist, and were then exposed with the mesa-level mask. The optimal focus and exposure were determined through a focus-exposure matrix (FEM) performed previously on dummy

Si wafers coated with comparable resist thickness. The pieces were developed in CD-26 and hard baked.

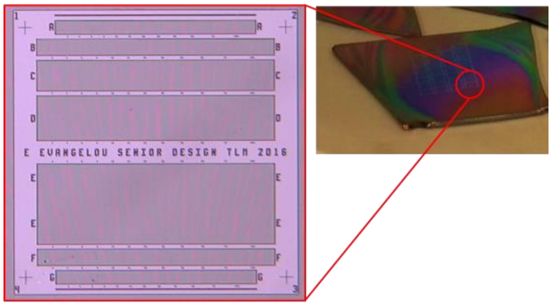

Figure 4 – The mesa level pattern developed on a piece.

Samples were etched in the LAM4600 RIE tool using a newly developed/characterized etch recipe, and subsequently had the remaining photoresist stripped off via an O_2 plasma ash. The pieces were then cleaned in an ultrasonic bath of PG Remover, rinsed in DI water, primed with a single drop of liquid HMDS, and then coated with LOR-5A and HPR-504 to form a liftoff-capable bilayer photoresist stack. Pieces were then exposed with the contact cut level mask at an optimized focus and exposure determined previously by a FEM performed on dummy Si wafers. Pieces were developed in CD-26 but were not hard baked so as to not destroy the overhang profile of the bilayer resist stack. The contact metals were then deposited. Five principle metal stacks were to be fabricated, as seen in Figure 5.

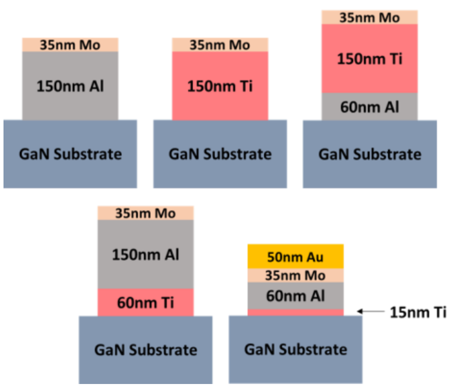

Figure 5 – The five principle metal contacts to be tested.

With the metals deposited, a liftoff process was performed. Samples were placed in an ultrasonic bath of PG Remover for approximately twenty minutes, and were then rinsed in DI water.

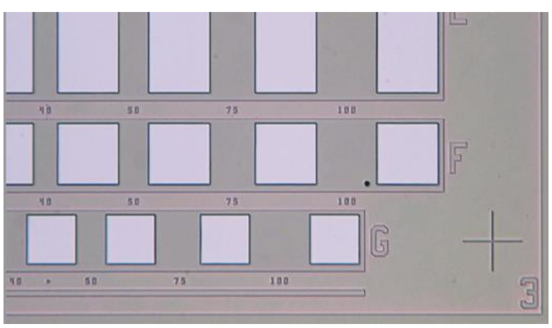

Figure 6 – The contact cut level pattern developed in liftoff-capable photoresist. The spacing between each contact window is listed in µm.

A thirty second anneal at 600°C was then performed, and devices were electrically tested.

IV. Results and Analysis

A. OiR-620 Coating Procedure

The procedure for spin coating OiR-620 on GaN was determined iteratively. Pre-existing coating recipes designed for 4-6” wafers were resulting in poor uniformity, and as such a new recipe needed to be developed. The full procedure can be seen in Table A1 in the Appendix, but simply put it involved rapidly ramping up the speed of the SCS coater, keeping it constant at 3500 rotations per minute for 45 seconds, and then slowly stopping it over the course of 10 seconds. This resulted in an evenly coated square piece with about 1.1µm of resist. Piece-to-piece variation in resist thickness was about +/- 0.3µm, while within piece variation in resist thickness was only +/- 0.1µm. The relatively high piece to piece variation in resist thickness can be attributed to the various shapes of the cleaved samples.

B. LAM4600 GaN Etch Results

The GaN etch recipe developed on the LAM4600 was created by adjusting a pre-existing aluminum etch recipe on the tool developed by Dr. Lynn Fuller for his CMOS manufacturing class. Argon and chlorine flow rates were determined based upon literature recommendations to keep the etch rate high while maintaining a low surface roughness for the etched GaN. Additionally, the power was kept at 125W so as to not bake the photoresist onto the piece. The full etch recipe can be seen in Table A3.

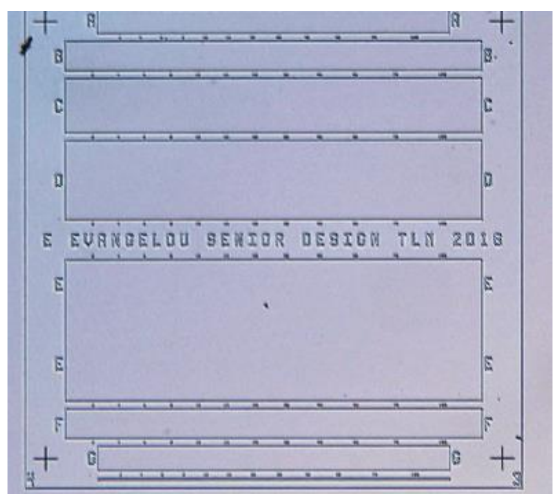

Figure 5 – The mesa level pattern etched into a GaN film.

The GaN was etched at a rate of 3.12 Å/s, while the photoresist was etched at a rate of 7.65 Å/s. This meant a selectivity of 1/2.45 between GaN and OiR-620 photoresist. This poor selectivity is common for a dry GaN etch, as comparable selectivity was calculated on the inductively coupled plasma etcher at Cornell’s Center for Nanoscale Fabrication.

C. LOR-5A Coating Procedure

The procedure for spin coating LOR-5A on GaN was determined through a trial and error process. Poor adhesion

between the LOR-5A and the GaN surface necessitated the development of a new coating procedure beyond the scope of the one recommended by the manufacturer of the resist. The full contact cut lithography procedure can be seen in Table A2 in the Appendix, but for a conformal resist coating the pieces needed (in summary):

- A PG Remover/DI water rinse to remove residual acetone from the surface of the piece
- An O_2 plasma surface treatment
- A longer and hotter pre-application bake than what was recommended by the resist manufacturer
- An HMDS liquid prime prior to coating

Additionally during the application of the LOR-5A, residual acetone on the chuck of the tool reacted with the resist to form latex films on the backsides of the pieces. In order to remove these tough films, pieces were cleaned with wipes dabbed in PG Remover.

D. Electrical Results

Due to limited time, only a single contact scheme was evaluated. Fifty nanometers of titanium was deposited on an n-GaN sample, and without performing a rapid thermal anneal, was electrically tested to verify whether or not a contact was made. Resistances measured were fairly low (1.0 kΩ - 1.4 kΩ), but also exhibited some moderate rectification at negative voltages below -5V. Contact resistance and transfer length were not determined, again due to time constraints.

V. Conclusion

Through this project several solutions to processing challenges involving GaN within the SMFL were developed. Coating procedures for OiR-620 and LOR-5A photoresists on a GaN film were created, and for the first time at RIT a reactive ion etch of GaN was performed on the LAM4600 tool. A Ti to n-GaN contact was fabricated and demonstrated moderately Ohmic behavior. The original goal of performing a full characterization of various metal schemes to n-GaN and n-AlGaN was not achieved, but groundwork was laid for future processing of GaN at RIT.

VI. References

[1] (2015) *Metal Lift-off Using a Bi-layer Process - SMFL - RIT Wiki*. Available: https://wiki.rit.edu/display/smfl/Metal+Lift-off+Using+a+Bi-layer+Process

[2] D. Ambrose. (2016) *Vapour pressures from 0.2 to 101.325 kPa 3.4.4*. Available: http://www.kayelaby.npl.co.uk/chemistry/3_4/3_4_4.html

[3] D. S. Rawal, *et al.*, "Cl2/Ar based inductively coupled plasma etching of GaN/AlGaN structure," in *16th International Workshop on Physics of Semiconductor Devices*, 2016, pp. 85490L-85490L-9.

[4] D. R. Stull, "Vapor Pressure of Pure Substances. Organic and Inorganic Compounds," May 1, 2002 2002.

[5] D. K. Schroder, *Semiconductor Material and Device Characterization, 3rd Edition*, 3rd ed., 2015.

[6] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, "GaN-Based RF power devices and amplifiers," *Proceedings of the IEEE,* vol. 96, pp. 287-305, Feb 2008.

[7] U. K. Mishra, C. U. Dept. of Electr. & Comput. Eng., Santa Barbara, CA, USA, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE,* vol. 90, pp. 1022-1031, Jun 2002 2002.

[8] S. J. Pearton, C. R. Abernathy, F. Ren, and SpringerLink (Online service). (2006). *Gallium Nitride Processing for Electronics, Sensors and Spintronics*.

[9] L. Wang. "Ohmic Metallizations to aluminum gallium nitride/gallium nitride high electron mobility transistors: Electrical and microstructural studies." *ProQuest Dissertations and Theses* pp. 301. 2008.

VII. Appendix

OiR-620 Coat/Expose/Develop Procedure			
Pre-Bake		**Units**	**Notes**
Time	60	s	
Temp	93	°C	
SCS Coating Recipe		**Units**	**Notes**
RPM 1	1500	rpm	Place piece on chuck, run recipe to ensure proper vacuum, then puddle coat piece with OiR-620, then run recipe.
Ramp 1	1	s	
Time 1	1	s	
RPM 2	3500	rpm	
Ramp 2	1	s	
Time 2	40	s	
RPM 3	3600	rpm	
Ramp 3	1	s	
Time 3	0	s	
Ramp 4	10	s	
Chuck Radius	3/8	Inch	
Post Application Bake		**Units**	**Notes**
Time	60	s	
Temp	93	°C	
GCA Exposure		**Units**	**Notes**
Intensity	37.5	mW/cm^2	Verify dose to clear with an FEM
Time	2.8	s	
Dose	105	mJ/cm^2	
Post Exposure Bake		**Units**	**Notes**
Time	60	s	
Temp	112	°C	
CD-26 Hand Develop		**Units**	**Notes**
Time	60	s	
Hard Bake		**Units**	**Notes**
Time	60	s	
Temp	145	°C	
Resist Thickness	1.1	µm	

Table A1 – Lithography procedure for OiR-620 photoresist on an n-GaN surface.

LOR-5A + HPR-504 Coat/Expose/Develop/Liftoff Procedure			
Sample Prep		**Units**	**Notes**
O2 Plasma Surface Treatment			
Time	190	s	
PG-Remover Ultrasonic Rinse			
Time	10	min	
DI Water Rinse			
Time	1	min	
Pre-Bake		**Units**	**Notes**
Time	120	s	
Temp	200	°C	
LOR-5A SCS Coating Recipe		**Units**	**Notes**
RPM 1	500	rpm	Place piece on chuck, run recipe to ensure proper vacuum, then deposit a single drop of HMDS liquid primer, then run recipe. When the run is complete, puddle coat the piece with LOR-5A and re-run the recipe.
Ramp 1	1	s	
Time 1	3	s	
RPM 2	3000	rpm	
Ramp 2	1	s	
Time 2	45	s	
RPM 3	3600	rpm	
Ramp 3	1	s	
Time 3	0	s	
Ramp 4	10	s	
Chuck Radius	3/8	Inch	
Post Application Bake		**Units**	**Notes**
Time	60	s	
Temp	150	°C	
HPR-504 SCS Coating Recipe		**Units**	**Notes**
RPM 1	500	rpm	Place piece on chuck, run recipe to ensure proper vacuum, then puddle coat, then run recipe. If vacuum check fails, ensure that the backside of the piece is clean. If the piece has residual LOR-5A on its back, use a dab of PG-Remover on a wipe to remove the film at a chemical bench.
Ramp 1	1	s	
Time 1	3	s	
RPM 2	3500	rpm	
Ramp 2	1	s	
Time 2	40	s	
RPM 3	3600	rpm	
Ramp 3	1	s	
Time 3	0	s	
Ramp 4	10	s	
Chuck Radius	3/8	Inch	
Post Application Bake		**Units**	**Notes**
Time	60	s	
Temp	100	°C	
GCA Exposure		**Units**	**Notes**
Intensity	37.5	mW/cm^2	Verify dose to clear with an FEM
Time	0.9	s	
Dose	33.75	mJ/cm^2	
CD-26 Hand Develop		**Units**	**Notes**
Time	60	s	
Resist Thickness	0.7	µm	
Liftoff		**Units**	**Notes**
PG-Remover Ultrasonic Rinse			It might take longer for resist to fully lift off. Visual inspection necessary.
Time	~20	min	

Table A2 – Lithography procedure for LOR-5A and HPR-504 bi-layer photoresist stack on an n-GaN surface.

LAM4600 GaN Etch Recipe					
Step	**1**	**2**	**3**	**4**	**5**
Step Description	**Gas Stabilization**	**Al_20_3 sputter**	**GaN Etch**	**Overetch Step**	**End**
Pressure (mTorr)	100	100	100	100	100
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	250	125	125	0
Gap (cm)	3	3	3	3	5.3
O2 flow (sccm)	0	0	0	0	0
N2 flow (sccm)	0	0	0	0	0
BCl_3 flow (sccm)	50	50	25	25	0
Cl2 flow (sccm)	10	10	30	23	0
Ar flow (sccm)	13	13	20	25	25
CHCl3 flow (sccm)	8	8	8	8	8
Completion Condition	Stable	Time	Time	Time	Time
Time (s)	15	8	**420**	0	15
Recipe Results					
GaN Etch Rate (Å/s)	3.12				
Photoresist Etch Rate (A/s)	7.65				
GaN / PR Selectivity	1 / 2.45				

Table A3 – Etch recipe for n-GaN on the LAM4600 RIE tool.

Eric A. Evangelou (RIT ’16) Raised in Astoria, NY, Eric attended the Rochester Institute of Technology. He obtained a bachelor’s degree in microelectronic engineering from RIT, in Rochester, New York, USA.