Development of a LFLE Double Pattern Process for TE Mode Photonic Devices

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***Abstract*—As the popularity of photonic devices and their uses increases, reliable manufacturing processes will need to be developed to make them more cost effective. Many companies still utilize i-line lithography, with very robust processes. Photonic devices require feature sizes often too small to be fabricated on i-line tools, especially for TE mode devices. In order to fabricate these devices, a form of double patterning will need to be developed.**

Proposed is a Litho-Freeze-Litho-Etch (LFLE) process that can achieve the feature sizes capable of fabricating TE mode photonic devices. This project encompasses design, development, and characterization of a LFLE process that can achieve sub 300 nm spacing and feature widths of 300 nm. The LFLE process will pattern a positive resist (OiR-620), which will be cured using a UV source (250 nm). A negative resist (NLOF-2020) will be patterned over top the cured positive resist, resulting in a compound photoresist image that can be etched. A development mask design was created and utilized to successfully pattern a compound image, feature sizes were resolved down to 150 nm with the negative resist and 200 nm in positive resist, gaps were shown to be in the sub 200 nm range.

Future work will be needed to refine the process to be usable for TE mode devices, however the process has been successfully tested and shows significant promise.

I. Introduction and Motivation

SILICON photonics are rapidly becoming useful on the micro and nano-fabrication scales. Because of this it is beneficial to design new processes that can manufacture these geometries with existing semiconductor fabrication facilities, and legacy tools. As the semiconductor industry has pushed past the minimum resolution of current lithographic systems many different forms of double and triple patterning processes have allowed continued progress toward smaller feature sizes. Variations on these methods include Litho-Etch-Litho-Etch (LELE) Litho-Litho-Etch (LLE), or Litho-Freeze-Litho-Etch (LFLE) [3][4]

Much of the current work on photonic devices at RIT is being done with i-line lithography, which is very reasonable for TM mode devices, but cannot adequately reach the feature size and feature separation needed for TE mode devices. To accommodate the lithographic constraints imposed by TE mode photonic devices some form of double patterning would be necessary when using i-line lithography. The benefit in the proposed LFLE process comes from the limited number of added process steps, as it only requires an extra flood exposure step at elevated temperature in between the two main lithography steps that ”freezes” the first pattern before applying the second. With a properly optimized LFLE process both TM and TE mode devices can be realized using i-line lithography in a single process flow or chip design.

II. Theory

A. Waveguide Geometry

The waveguides that have been chosen for this project are a strip waveguide that is $500nm$ wide and $220nm$ tall, as seen in Figure 1 [2]. These dimensions are chosen so as to confine just a single TE and TM mode within the waveguide structure. Figures 2 and 3 show how a $220nm$ thickness and a $500nm$ width wave guide confine only the $TE0$ and $TM0$ modes.

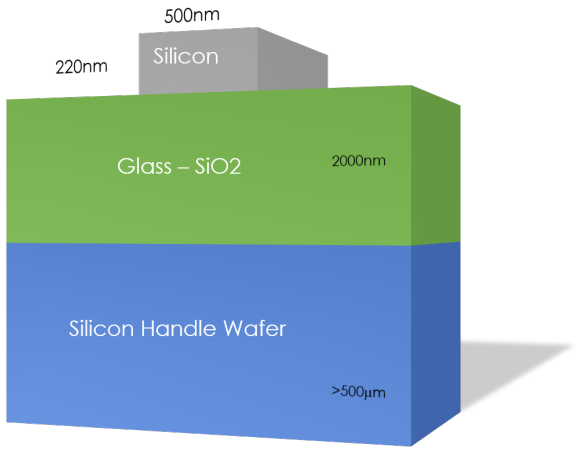


Fig. 1: Thickness versus effective index of a silicon waveguide

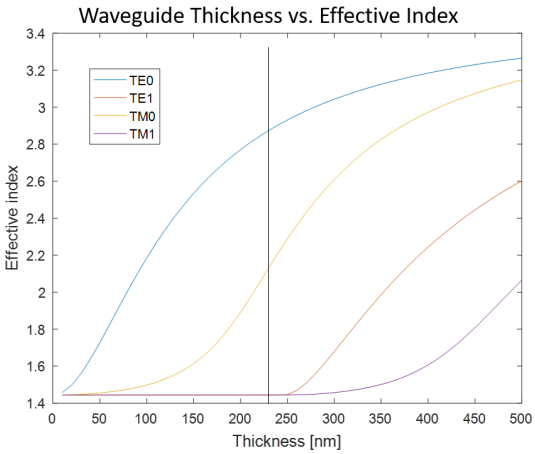


Fig. 2: Thickness versus effective index of a silicon waveguide

B. Evanescent Field Coupling

One of the fundamental properties that photonic devices employ is coupling of light energies from one waveguide

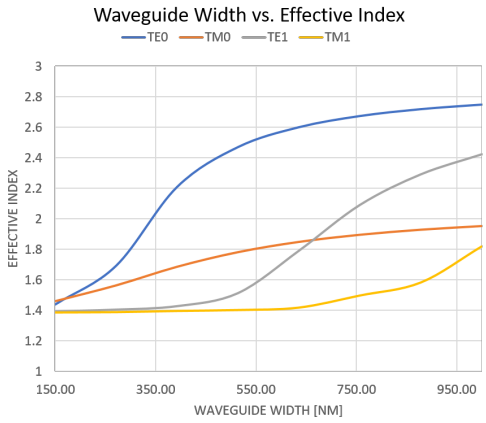


Fig. 3: Width versus effective index of a silicon waveguide

structure to another. This is accomplished through evanescent field coupling where light not fully contained inside the waveguide is transferred into another waveguide. Figure 4 shows the amplitude of the E-field in both TE and TM mode that is inside and outside the wave guide, from this it is clear that TM mode has a larger evanescent field amplitude. To see this more clearly, Figures 5 and 6 show log scale profiles of the E-field energies in both TE and TM output from Lumerical MODE software. Because of this difference in amplitude the TM mode photonic devices can couple energy to another wave guide farther away.

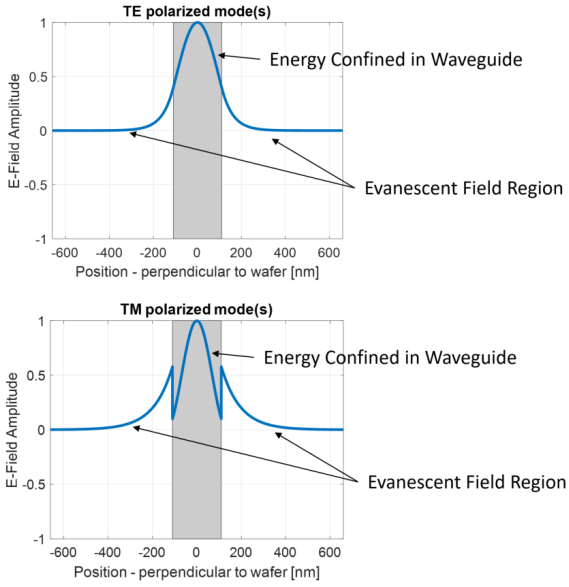


Fig. 4: Evanescent field energies for both TE and TM

III. Process Development

A. Proposed Process

The proposed process is described as a Litho-Freeze-Litho-Etch (LFLE) process, with a first litho pattern being locked in place by a ”freeze’ process, and a second litho pattern being

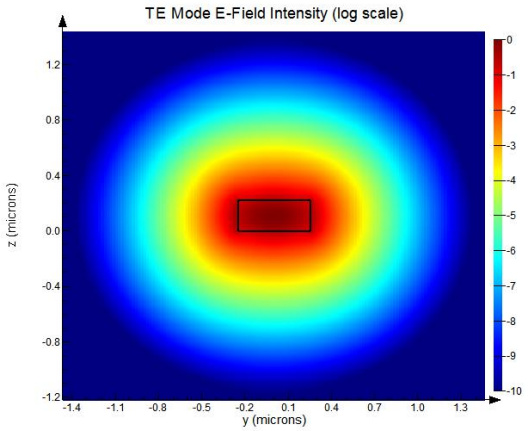


Fig. 5: TE Log scale E-field profile from Lumerical MODE software

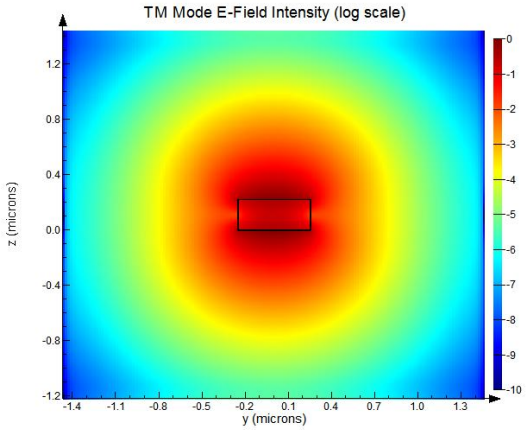


Fig. 6: TM Log scale E-field profile from Lumerical MODE software

imaged over top the first before the etch process. This type of process has also been referred to as a Litho-Process-Litho-Etch (LPLE).

The proposed LFLE process will utilize a first layer in a positive tone resist, OiR-620, with a UV cure ”freeze” process, that forms a protective skin on the first pattern, after which a negative tone resist, NLOF-2020, is coated and patterned, the resulting compound photoresist image is then etched into the substrate. Benefits from the proposed process are that it allows the use of two resists that contain the same solvent, and it only adds a single process step in between the patterning of the first and second layers of resist, also by utilizing a positive tone and negative tone resist the first layer will not be exposed further during the second patterning process.

The proposed LFLE process starts with a bare wafer which is RCA cleaned, followed by the application of ICON-7 BARC, which requires a dehydration bake at $150°C$ before being applied on the CEE-100 coater at a target thickness of $65nm$, followed by a Post Application Bake (PAB) at $170°C$ for $60s$. Next the positive resist, OiR-620 diluted 1:1 with PGMEA, is applied by hand dispensing on the SVG-88 track, with a target thickness of $300nm$, followed by a PAB at $110°C$

for $60s$. This first layer of resist is exposed on the ASML stepper using a clear field mask at $185mJ/cm^2$, followed by a Post Exposure Bake (PEB) at $110°C$ for $60s$, next this first layer of photoresist is developed on the SVG-88 track using TMAH developer for $60s$, followed by a Post Develop Bake (PDB) at $140°C$ for $60s$.

The patterned first layer of resist is then subjected to a flood exposure of UV light at elevated temperature to freeze the image in place, this is accomplished using a hotplate set to $140°C$ and a hand-held UV lamp that outputs $248nm$ wavelength light. A ring stand with a long enough arm to position and stabilize the light over the hotplate was provided by the SMFL staff. Figure 7 shows how this curing station was setup, care was taken to ensure no other lab users were working with photosensitive materials in the area. Exposure under this setup was performed for $8min$ to provide adequate curing dose on the OiR-620 photoresist pattern.

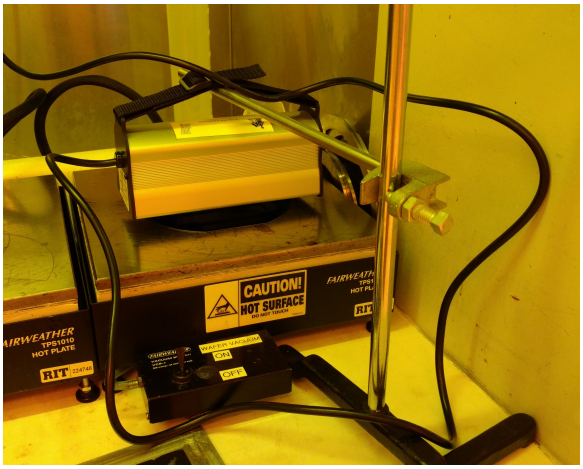


Fig. 7: Custom UV curing station setup

Following the UV cure process, application of the negative resist, NLOF-2020 diluted 3:5 with PGMEA, is hand dispensed on the SVG-88 track with a target thickness of $600nm$, and a PAB is performed at $110°C$ for $60s$. This second layer of resist is exposed on the ASML stepper using a dark field mask at $170mJ/cm^2$, followed by a PEB at $110°C$ for $60s$, after which the second layer of photoresist is developed on the SVG-88 track using TMAH developer for $60s$, followed by a Post Develop Bake (PDB) at $140°C$ for $60s$. The result thus far is a compound photoresist image on top a BARC layer.

The BARC layer is removed in the areas not patterned by the photoresist on the Drytek Quad Reactive Ion Etcher (RIE), chamber 3 was used to perform a O_2 plasma etch at $70mT$ pressure, $100W$ power, with $5sccm$ of O_2, for $30s$. Following the removal of the BARC the primary etch was processed using the STS Deep Etcher, an Inductively Coupled Plasma (ICP) RIE tool, and a recipe developed specifically for the very shallow etch necessary on SOI wafers for photonic devices. This etch is performed at $20mT$ pressure, $725W$ power, with $60sccm$ of C_4F_8, $10sccm$ of O_2, $40sccm$ of Ar, and $20sccm$ of Sf_6, at a rate of $85nm/min$, which for a $220nm$ depth takes approximately two and a half minutes.

The final processing includes an O_2 ash on the GaSonics Aura 1000 Asher, using recipe "FF", followed by an RCA clean, before the final step of coating a cladding material, which in this case is simply OiR-620 photoresist at a thickness of $1.3\mu m$. The full process listing all process steps and recipe information is available in Appendix A.

B. UV Cure Design of Experiment

In order to achieve the primary goal of developing a LFLE process the "freeze" step was a critical component, therefore the primary experiment undertaken during pocess development was the realization and optimization of the UV cure process. Initial challenges to realizing this process were acquiring a source that could deliver the wavelength necessary to perform the curing, as the SMFL was not outfitted with a flood exposure tool at the necessary $248nm$ wavelength, and then determining the proper exposure time and temperature necessary to properly cure the resist, made difficult as there was also no detector available that could provide information on the intensity of a $248nm$ source. Dr Ewbank was able to provide a hand-held lamp capable of emitting the required wavelength of light, and after some initial trial and error a reasonable starting temperature and exposure time was acquired. To further characterize this process a full DOE was performed.

1) Data Collection: Wafer Processing: Data was collected by processing 15 wafers through a modified process very similar to that which is being explored. The modified process seeks to measure the area in cm^2 of cured photoresist that is remaining after a second layer of photoresist is processed over top the first. Because the two photoresist layers contain the same solvent any area of the first layer that is not cured or only partially cured will be penetrated by the solvent when the second layer is applied. This cause the first layer to be completely washed away during the processing of the second layer, or can cause some intermixing of the two layers. The general processing of the wafers is described in Figure 8.

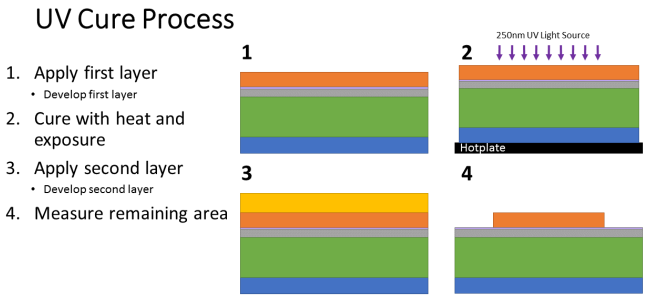


Fig. 8: UV cure experimental process flow

2) Data Collection: Experimental Design: The DOE was set up to explore the effect of exposure time, and exposure temperature on the area of resist that was fully cured. Figure 9 shows the experimental design matrix, which explored three exposure temperatures at five exposure times per exposure temperature, and resultant cured resist at each level.

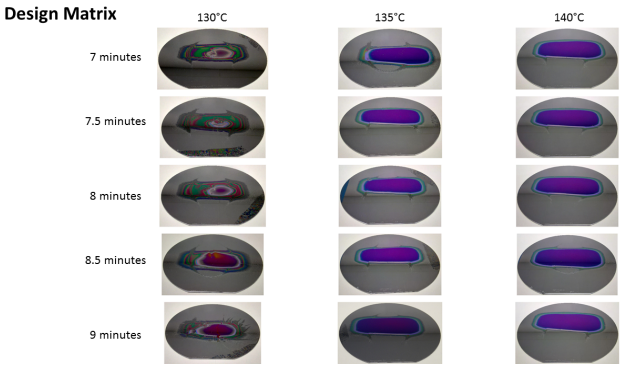


Fig. 9: UV cure DOE experimental design matrix

3) Area Extraction: The source shape of the UV cure lamp was rectangular at a distance away from the wafer of approximately 2 cm this means the exposure shape was roughly rectangular with rounded corners. The method of applying the photoresist layers is a spin coat method at 3000 RPM this can lead to the distortion of the first photoresist layer when applying the second layer. Because of these issues approximation of the area of the remaining photoresist is challenging because it does not conform to any regular geometric shape. To overcome this obstacle pictures were taken of the finished wafers and processed using Matlab image processing tools.

To extract the area of remaining cured photoresist, images of the finished wafers were imported into Matlab, see Figure 10, then using the HSV color space, the area of cured photoresist was isolated from the rest of the wafer, see Figure 11, The resulting image was converted to a binary mask and the pixels were counted, see Figure 12. The final area calculation was performed by determining the area per pixel using the known wafer diameter.

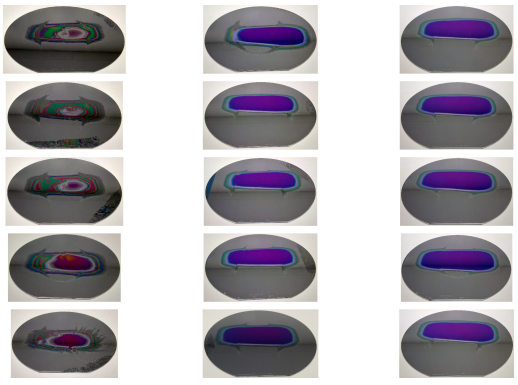


Fig. 10: Images taken of processed wafers

4) Reported Data: See Table I for all reported data.

5) Method of Analysis: Analysis was performed using least squares regression in the SAS software package. The model contained three predictor variables and one response variable. Equation 1 shows the model used. Assumptions of normality, constant variance and independence were applied to the model, and shown to be true. Equation 2 shows the null and alternative hypotheses.

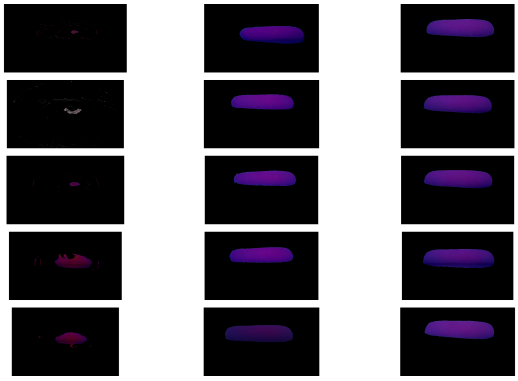


Fig. 11: Images converted to the HSV color space and filtered to show only cured polymer

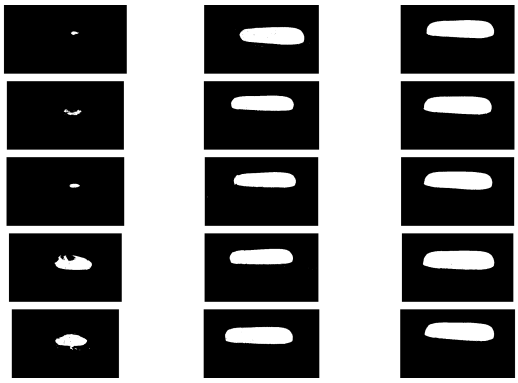


Fig. 12: Images converted to a binary mask

$$Area = B_0 + B_1 * ExposureTemperature + B_2 * ExposureTime + B_3 * Humidity + \epsilon \quad (1)$$

$$H_0 : B_0 = B_1 = B_2 = B_3 = 0$$
$$H_a : not\ H_0 \quad (2)$$

6) Results: When examining the data graphically it can be seen that the area of cured photoresist is generally linear with respect to exposure time but with decreasing slope at longer exposure times as shown in Figure 13. When examining the exposure temperature versus the area of cured photoresist, see Figure 14, there is a strong grouping of data, indicating a stronger correlation between the exposure temperature and area, versus the exposure time and the area.

7) Regression Results:

$$Area = -1832 + 0.59 * ExposureTemperature + 15.76 * ExposureTime - 902 * Humidity + \epsilon \quad (3)$$

When looking at the individual predictive variables each variable in the model is significant with the highest P-value of 0.0018. In addition when running a stepwise parameter selection the best model includes all three predictive variables. This stepwise selection test gave a best Cp of 4.0 when including all three variables.

TABLE I: Experimental data

	Exposure Temperature ($^{\circ}C$)	Exposure Time (sec)	Room Humidity (%)	Area of Cured Photoresist (cm^2)
1	130	420	0.50	4.69
2	130	450	0.50	13.14
3	130	480	0.50	9.04
4	130	510	0.50	114.81
5	130	540	0.50	99.38
6	135	420	0.34	287.66
7	135	450	0.34	251.94
8	135	480	0.34	250.66
9	135	510	0.34	263.37
10	135	540	0.34	302.61
11	140	420	0.37	309.34
12	140	450	0.37	311.90
13	140	480	0.37	313.95
14	140	510	0.37	359.86
15	140	540	0.37	319.81

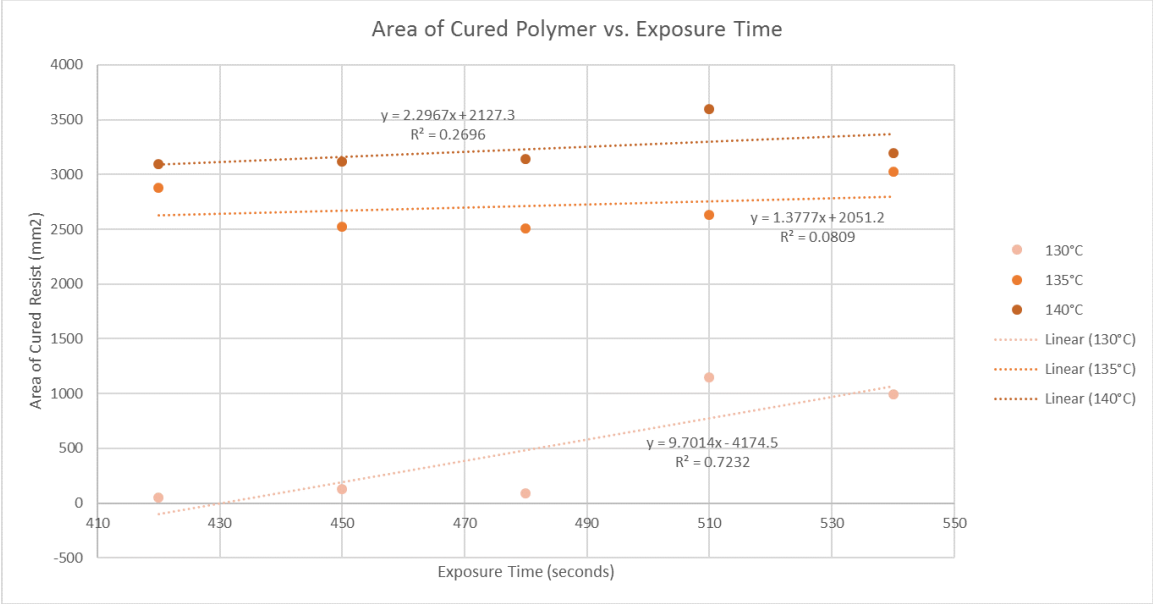


Fig. 13: Area of cured Polymer vs. Exposure Time Plot.

IV. Mask Design

A custom mask design was needed to explore the capability and limitations of the proposed LFLE process. The designed mask contained a vast array of design variation to allow future work with the proposed process to be optimized for a great many different feature widths, and feature separations. A simple overview of the mask design is shown in Figure 25. As TE mode ring resonator structures were the target device they have seen the largest spread of design variation, a smaller set of TM mode ring resonator devices with limited number of variations was also added to the mask to allow for comparison to the current TM mode single pattern process. Some double bus ring resonators for both TE and TM mode devices were also included which will test the limits of the proposed process, as a double bus ring resonator requires the smallest feature separation to obtain working devices. Figure 16 shows a single bus ring resonator design from KLayout software.

As with most masks some custom test structures were included as well as resolution targets in both the clear field and dark field die. These clear field and dark field were designed to align and interleave to form a single composite image after both images were patterned, this can be seen in Figure 17 where a grating coupler is shown with the pink layer as the clear field image and the purple layer as the dark field image. Overall this mask design should allow comprehensive testing, and optimization of the proposed process adequate for TE, TM, and mixed mode device designs. See Appendix B for a full mask overview including a listing of all design variations.

V. Experimental Results

Initial experimental results were very promising with clearly resolved compound photoresist images, and after etch SEM imaging showing well resolved features with very small feature separation. These results show clear validation of the proposed LFLE process.

A. Initial Lithography Results

Initial lithography results are shown below, with Figures 18, 19, and 20 highlighting the positive and negative tone

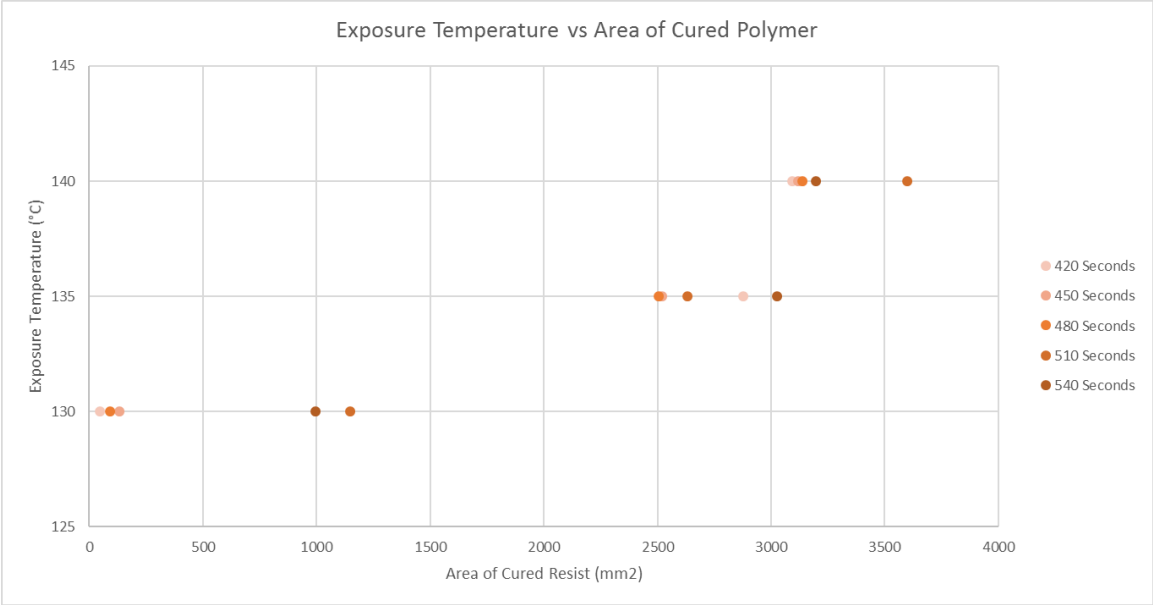


Fig. 14: Exposure Temperature vs. Area of cured Polymer Plot.

images, that were patterned successively and combine to form the compound photoresist image. Figure 20 shows a zoomed in view of the interleaved positive and negative images of the grating coupler arcs. Appendix C has an expanded set of images of these initial results including an array of images showing each pitch and duty ratio of TE mode grating couplers.

B. Initial Etch Results

Initial etch results are shown below, these images were taken using the LEO SEM and show clearly defined features etched into a bulk silicon wafer. Figures 21 and 22 show SEM images of a grating coupler device with clearly resolved arcs that were patterned with interleaved positive and negative tone images. Figures 23 and 24 show SEM images of a ring resonator device highlighting the ring to waveguide gap. Appendix C has an expanded set of SEM images showing measured feature sizes and gaps.

VI. Future Work

Some proposed future work would include:

1) Lithography optimization for SOI wafer
   - Account for changes in stack reflectivity
   - Separate optimization for positive and negative layers
2) Optical Proximity Correction (OPC) mask design
   - Corrections for bulging in ring to wave guides gap
   - Corrections for fine pitch grating couplers
3) Etch Recipe Optimization for compound resist image

VII. Conclusions

This project can be considered a success as the primary goal of developing a working LFLE process was obtained, further success was achieved by obtaining a minimum feature size of $150nm$, with a minimum feature separation of $100nm$. These successes were impactful because they were obtained using readily obtained i-line photoresists, and resists that utilize the same solvent. The UV cure step can be further refined using the same lamp used in this process development, but the addition of a flood exposure tool common in industry could potentially make this process significantly faster and more robust, as the exposure time used for this process is quite long, at a elevated temperature which can lead to potential warping of the photoresist profile. Systems in use in industry use sophisticated flash lamp systems and multi-stage temperature ramping of the photoresist to optimize the UV cure process. The mask design that was created can be utilized for a great many future optimizations of this process and will allow fine tuning of the process for TE mode, TM mode, or mixed mode devices.

The REG Procedure
Model: MODEL1
Dependent Variable: area

Number of Observations Read	15
Number of Observations Used	15

Analysis of Variance					
Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	3	222578	74193	131.76	<.0001
Error	11	6194.17205	563.10655		
Corrected Total	14	228773			

Root MSE	23.72987	R-Square	0.9729
Dependent Mean	214.14413	Adj R-Sq	0.9655
Coeff Var	11.08126		

Parameter Estimates							
Variable	DF	Parameter Estimate	Standard Error	t Value	Pr > |t|	95% Confidence Limits	
Intercept	1	-1832.13806	364.81531	-5.02	0.0004	-2635.09113	-1029.18499
time	1	0.58972	0.14442	4.08	0.0018	0.27187	0.90758
temp	1	15.75464	2.32719	6.77	<.0001	10.63253	20.87675
humidity	1	-901.64008	136.81456	-6.59	<.0001	-1202.76690	-600.51327

Fig. 15: ANOVA table with model parameter estimates.

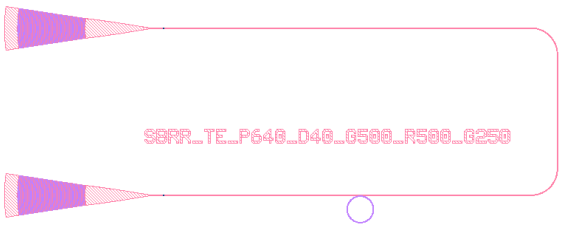


Fig. 16: Single bus ring resonator design from KLayout software

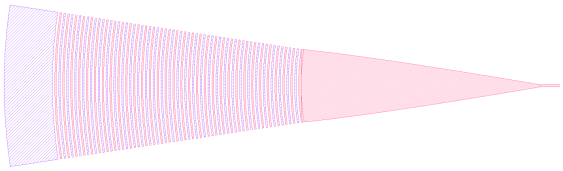


Fig. 17: Grating coupler design showing interleaved positive and negative tone images

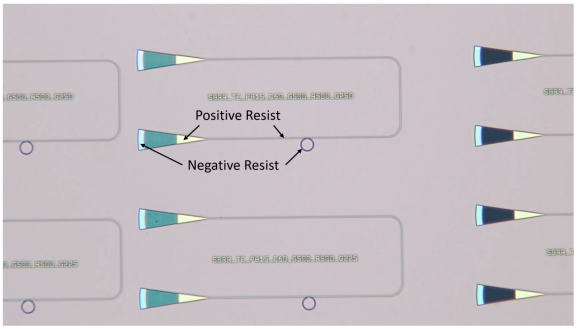


Fig. 18: Optical microscope images of the single bus ring resonator device, highlighting the areas of positive and negative tone resists.

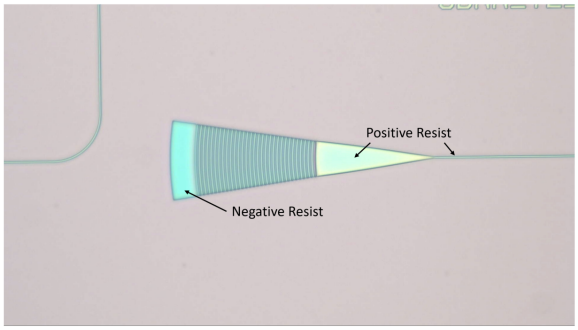


Fig. 19: Optical microscope images of the grating coupler device, highlighting the areas of positive and negative tone resists.

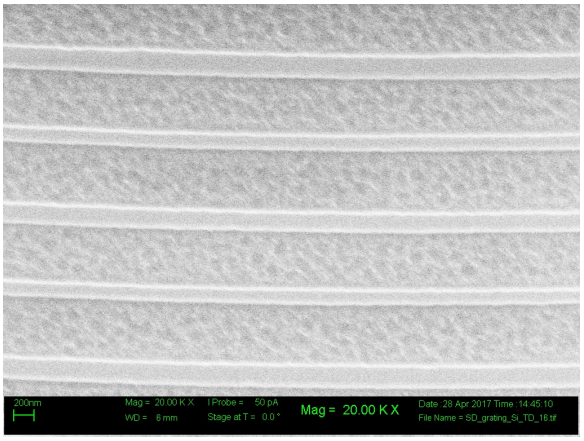


Fig. 22: SEM images of the grating coupler device, highlighting the interleaved arc features.

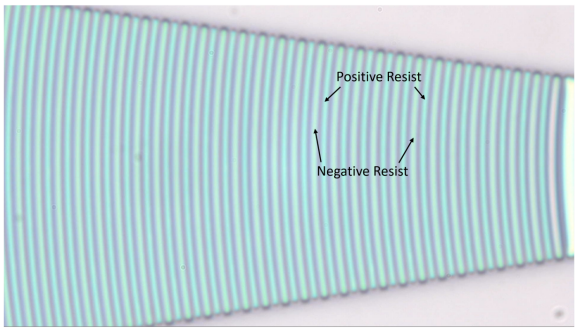


Fig. 20: Optical microscope images of the grating coupler device, highlighting the areas of positive and negative tone resists interleaved at a very fine pitch.

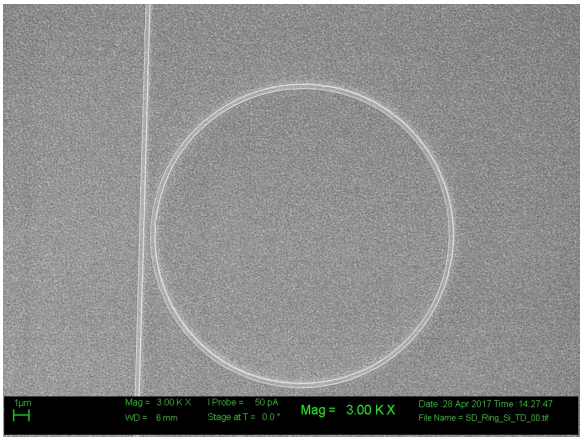


Fig. 23: SEM images of the ring resonator device.

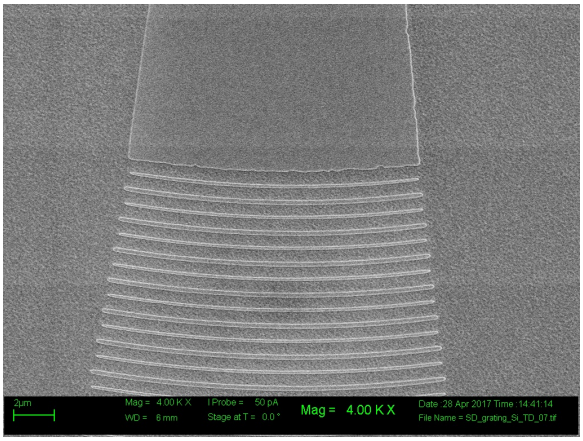


Fig. 21: SEM images of the grating coupler device.

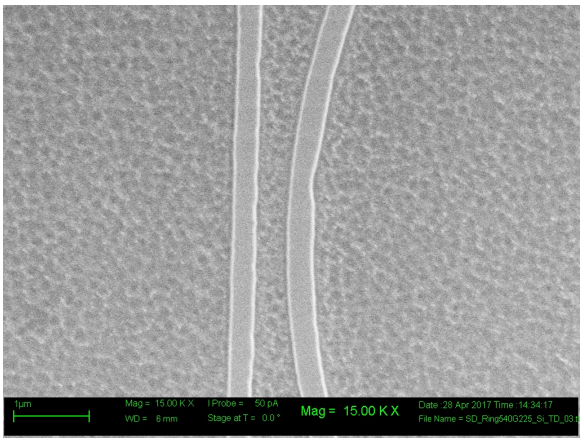


Fig. 24: SEM images of the ring resonator device, highlighting the wave guide to ring gap.

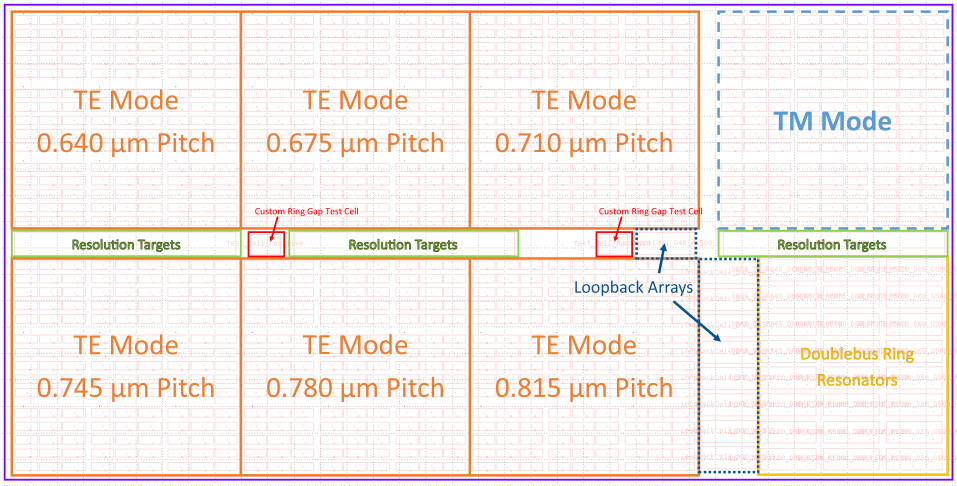


Fig. 25: Mask design overview mapping out the major design areas.

APPENDIX A
PROPOSED PROCESS

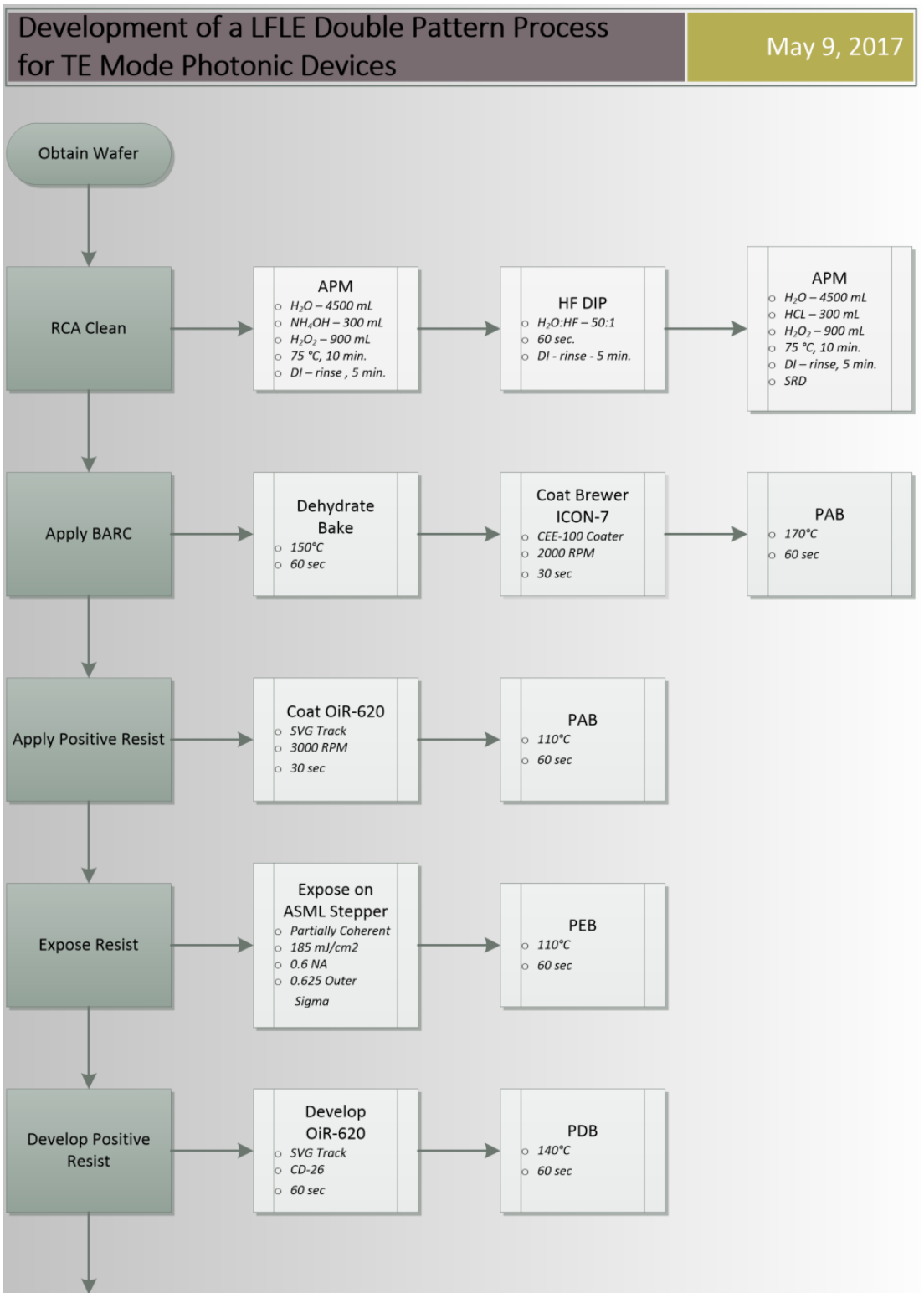


Fig. 26: Process flow.

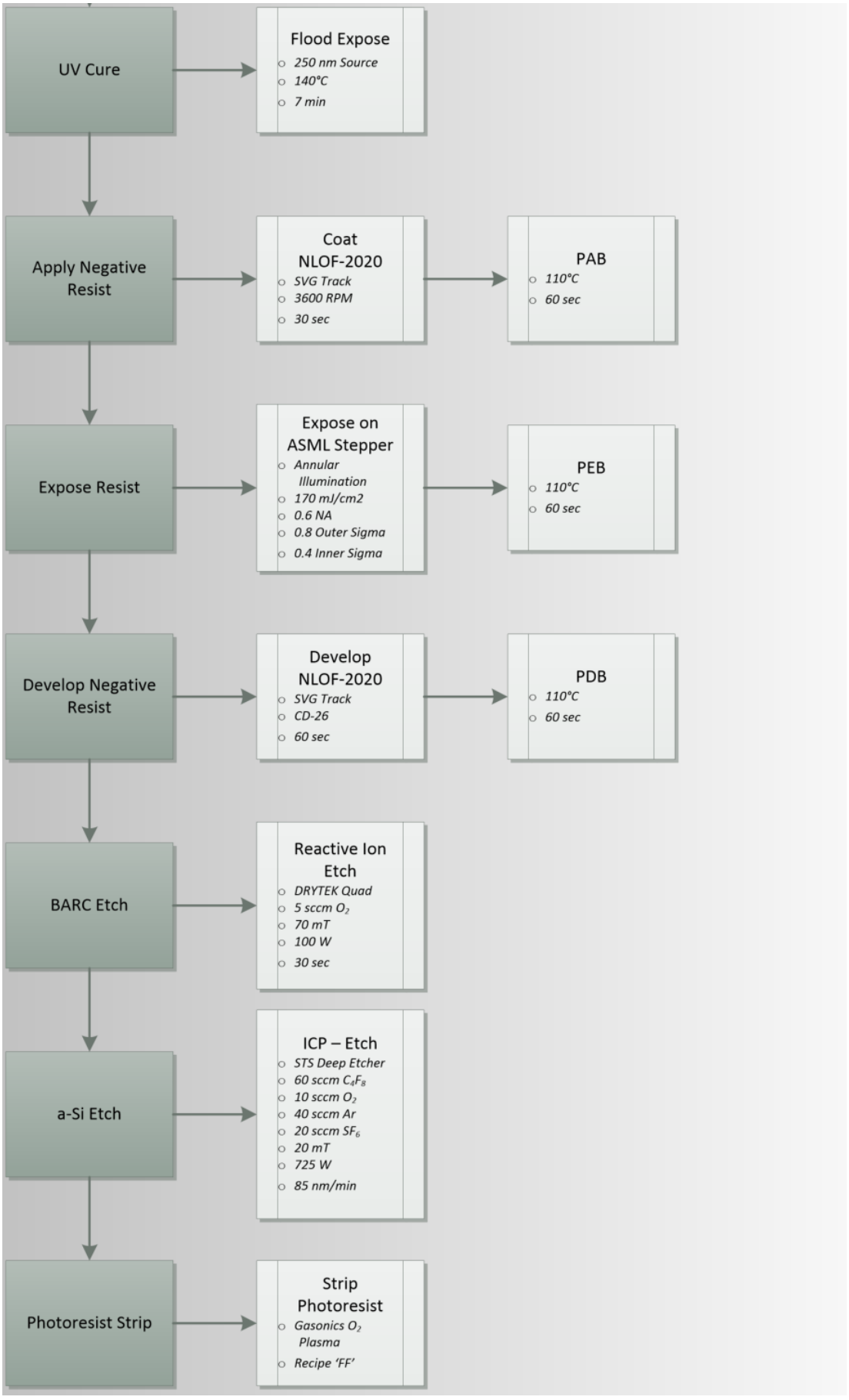


Fig. 27: Process flow continued.

APPENDIX B
MASK DESIGN

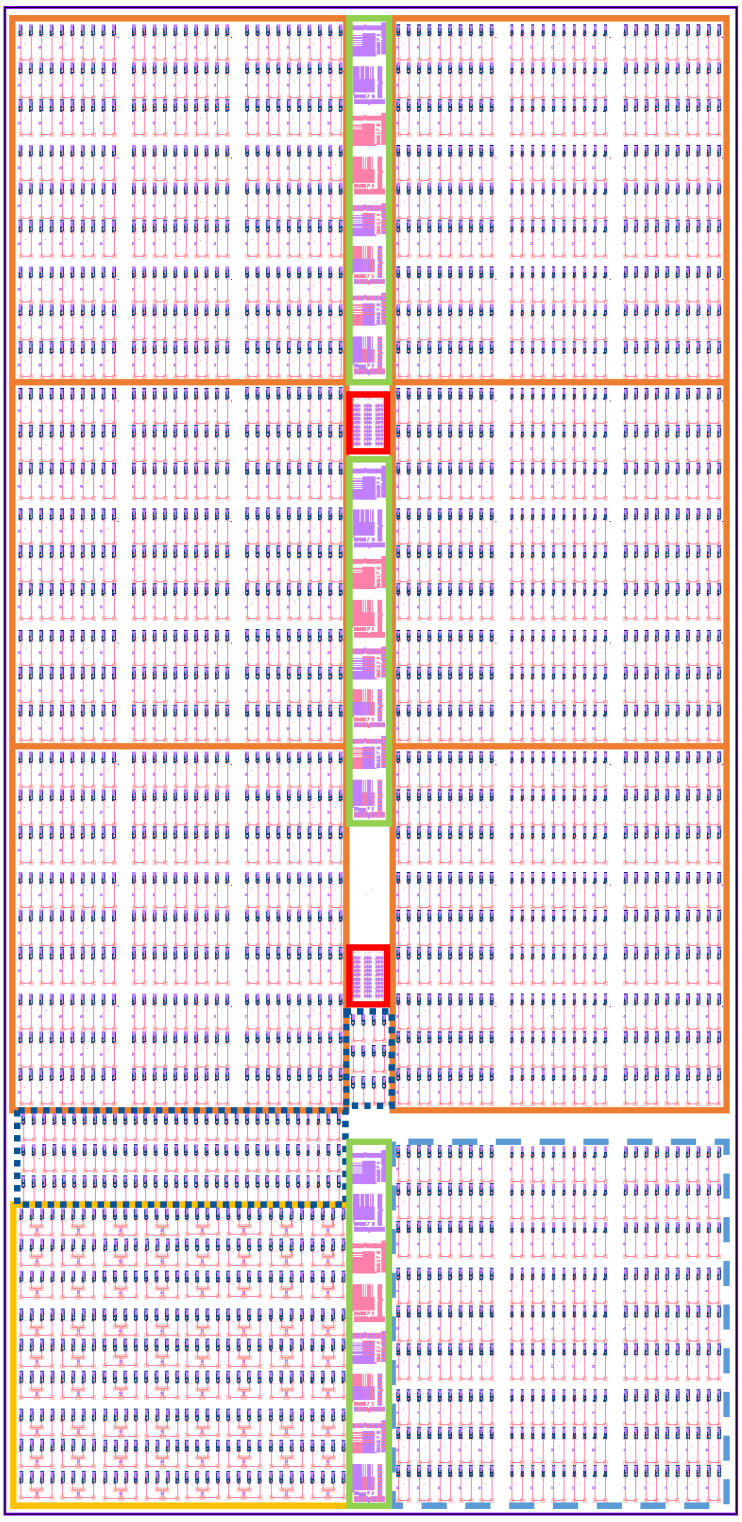


Fig. 28: General mask overview, highlighting regional feature groups.

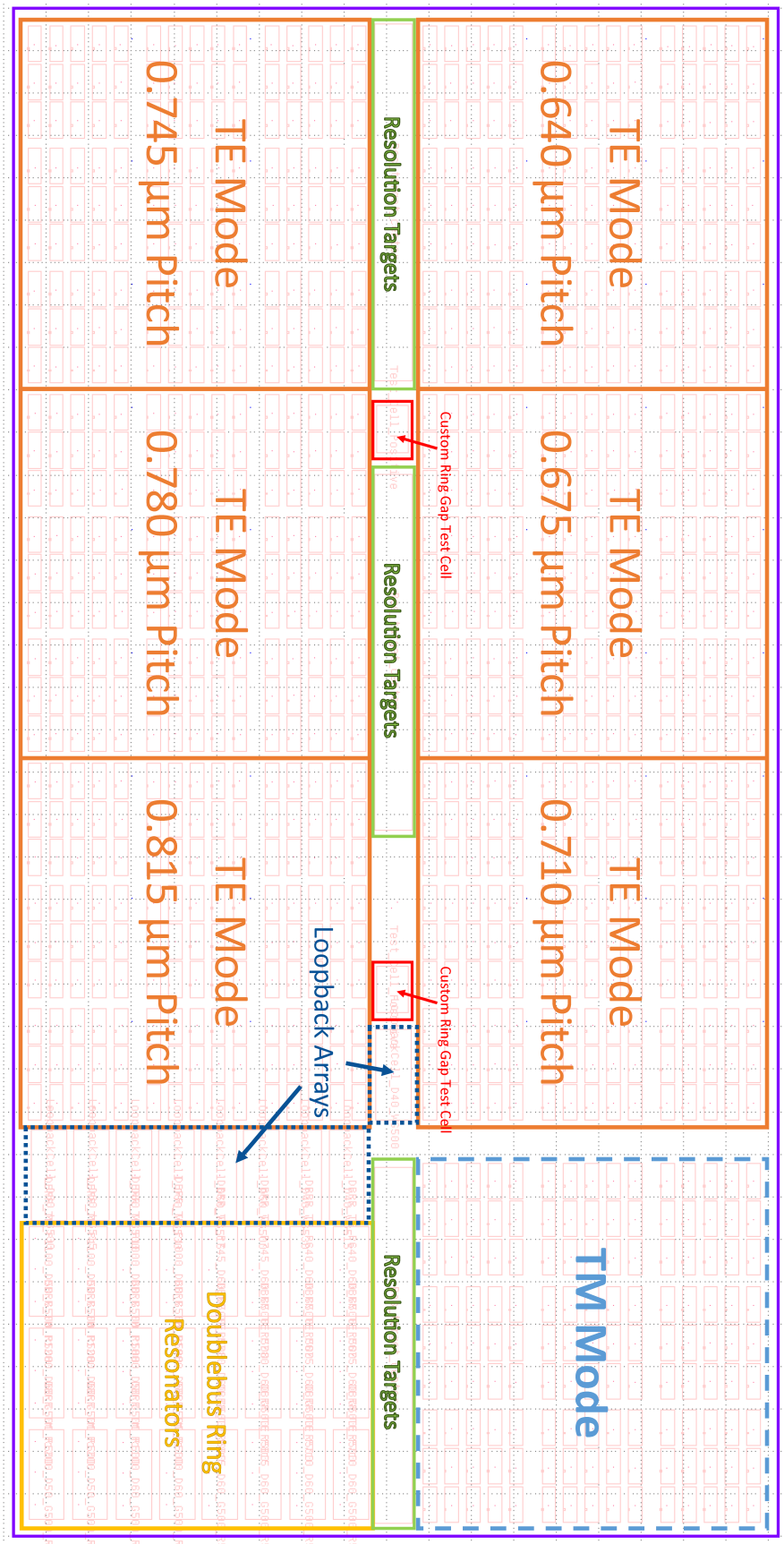


Fig. 29: Labeled regional groupings.

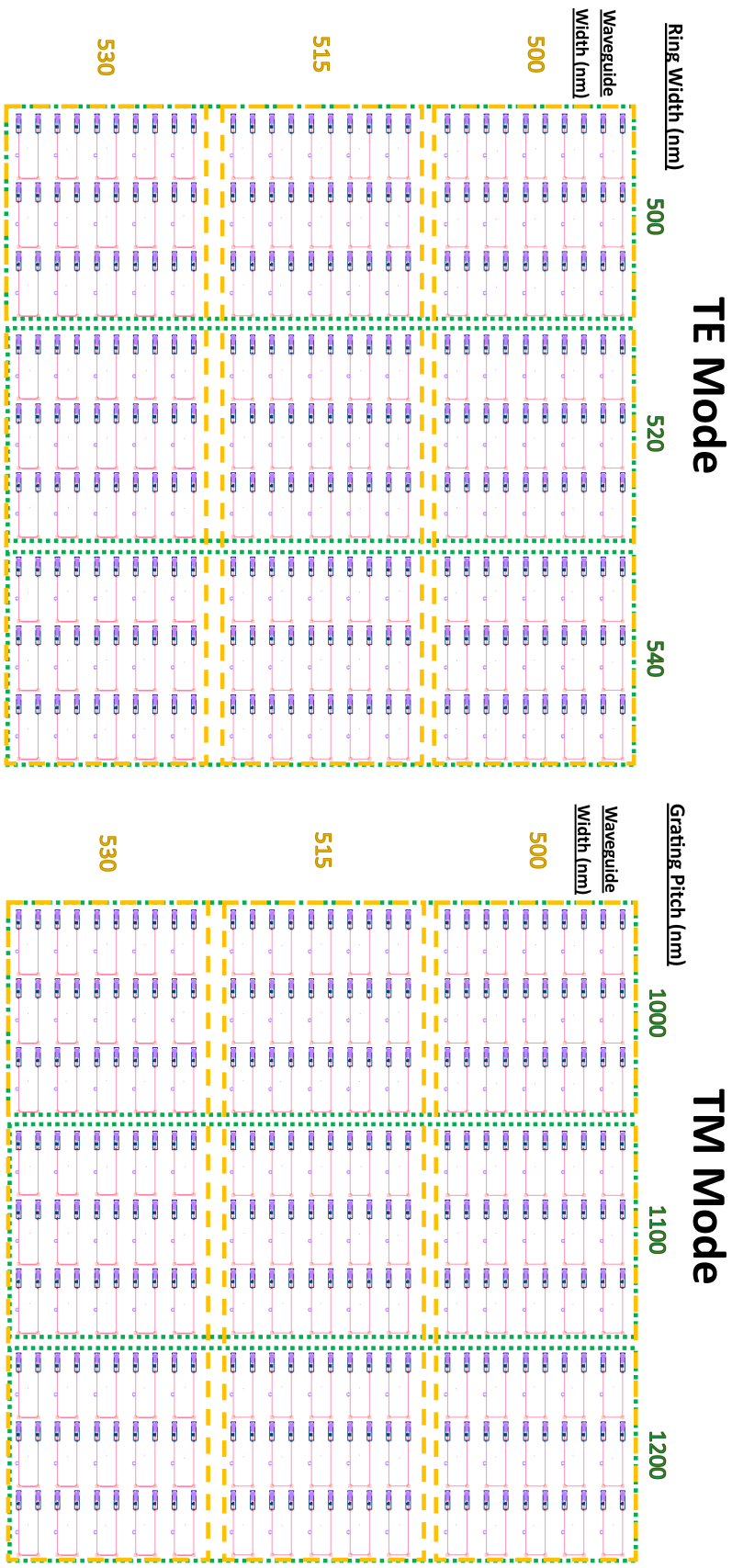


Fig. 30: Top level device variations for TE mode and TM mode regions.

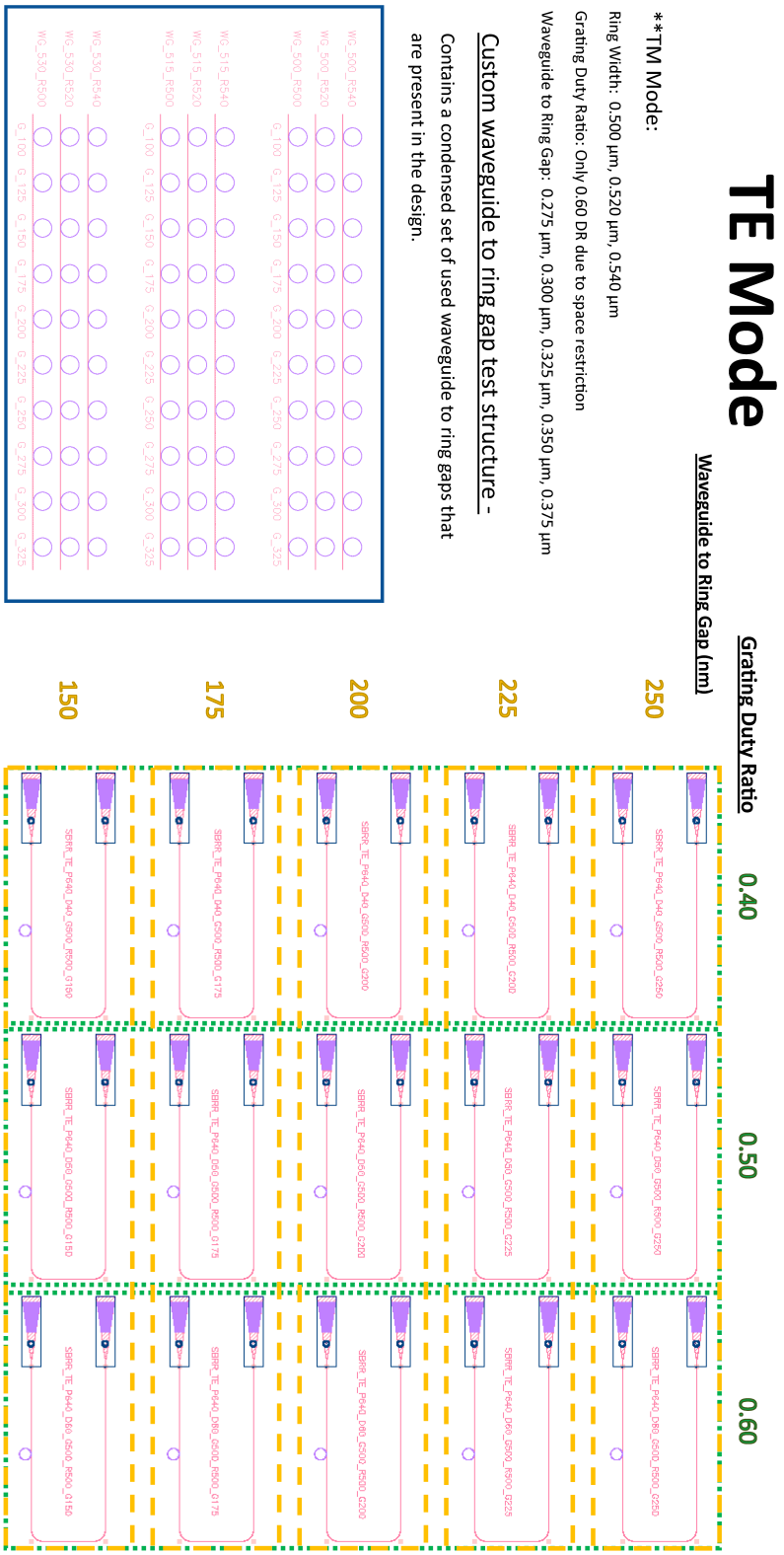


Fig. 31: Second level device variation for TE mode regions, also custom ring gap test structure.

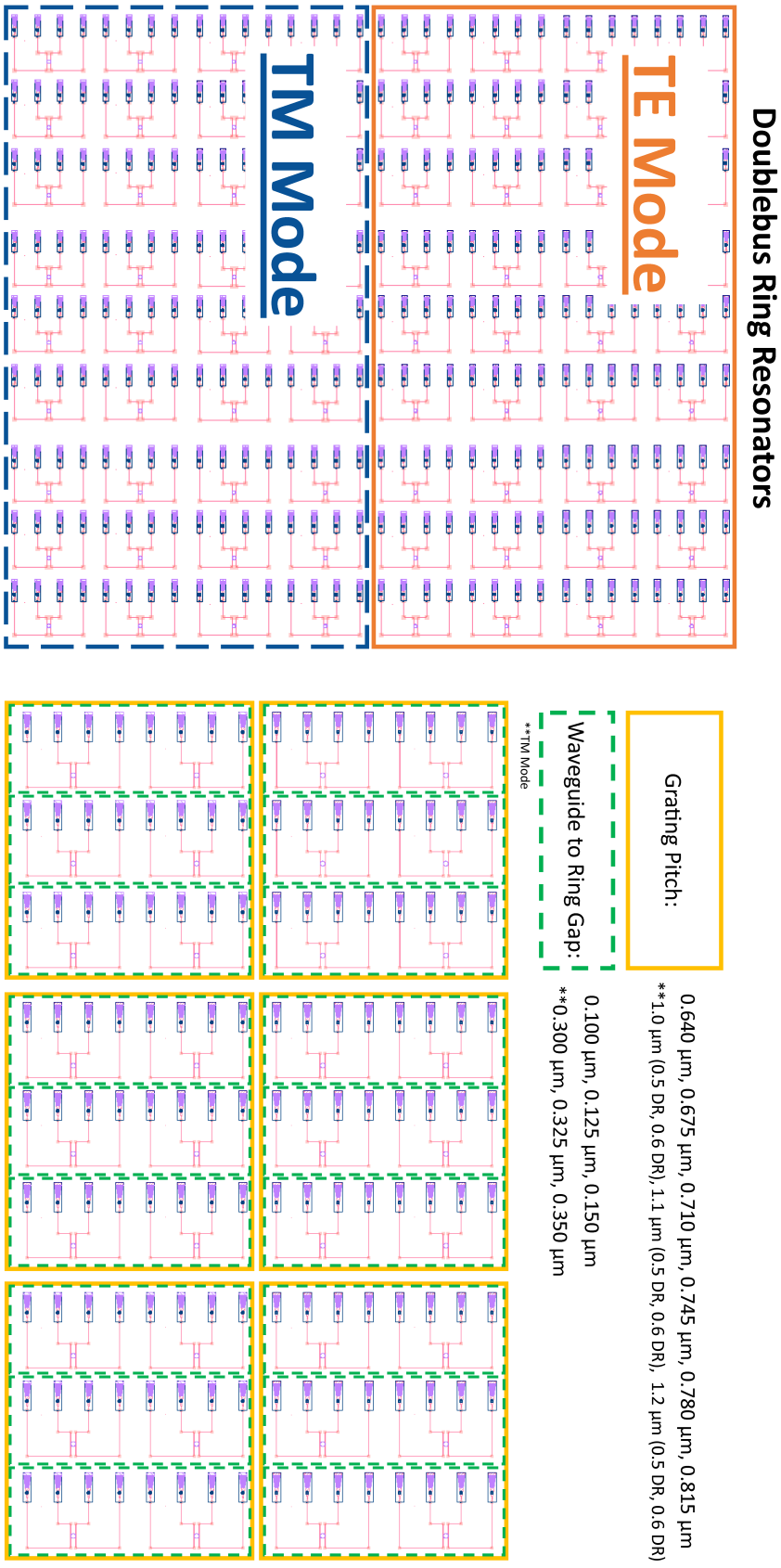


Fig. 32: Double bus ring resonator device variations for TE and TM mode.

APPENDIX C
EXPERIMENT RESULTS EXPANDED

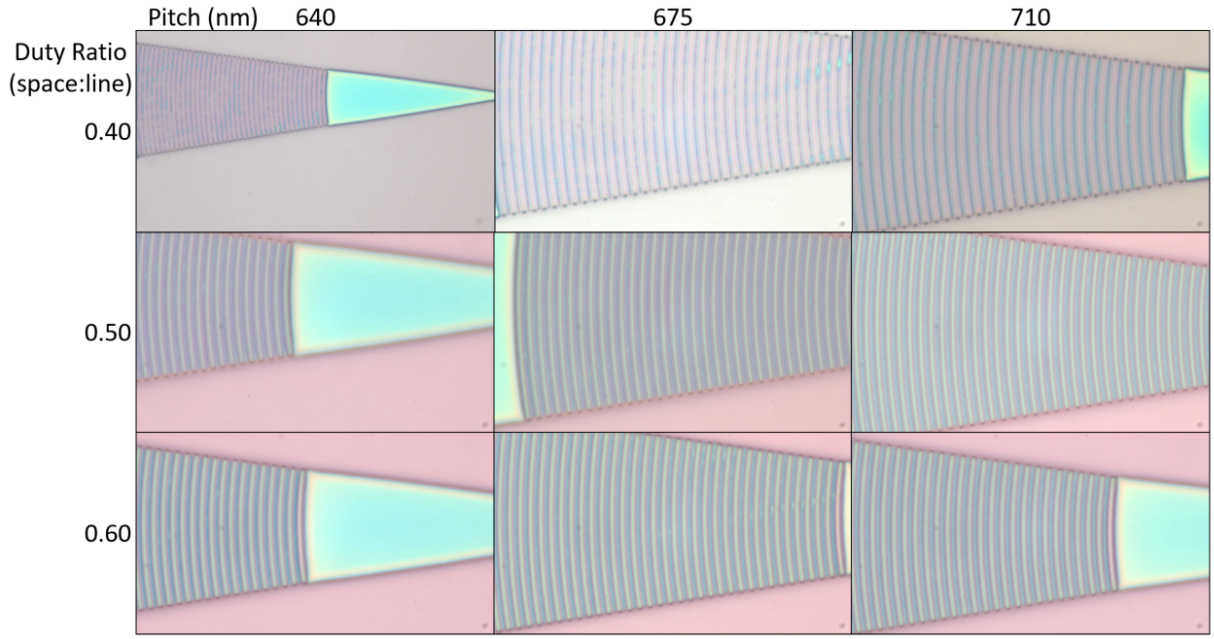


Fig. 33: Array of optical microscope images showing each pitch and duty ratio for TE mode devices.

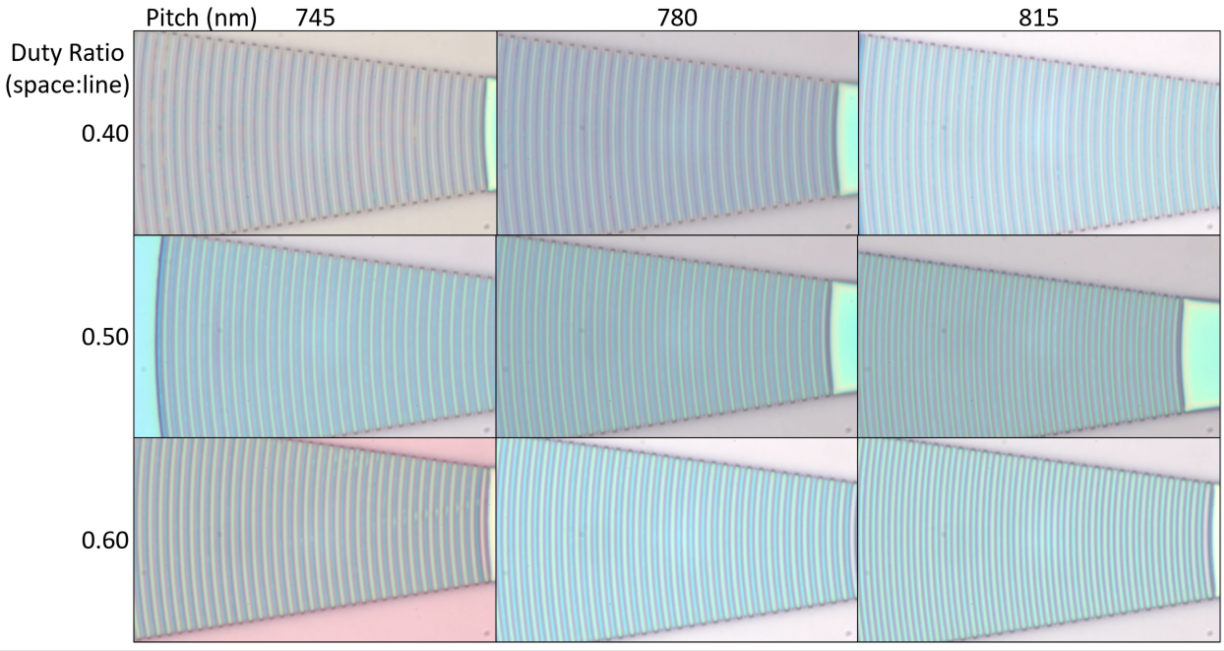
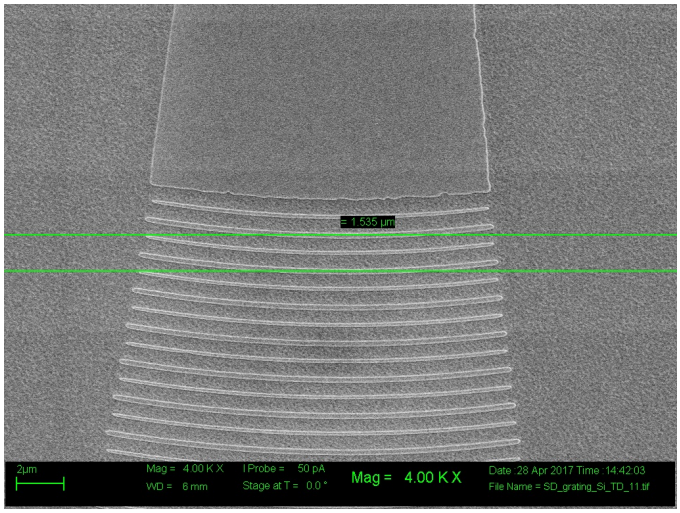
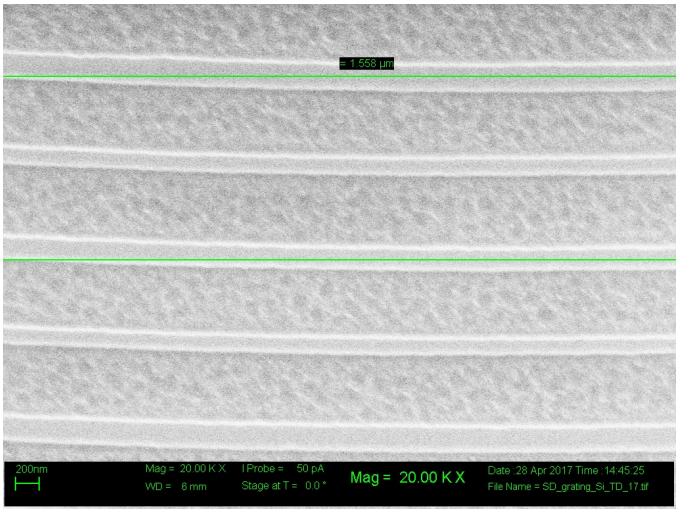


Fig. 34: Array of optical microscope images showing each pitch and duty ratio for TE mode devices continued.

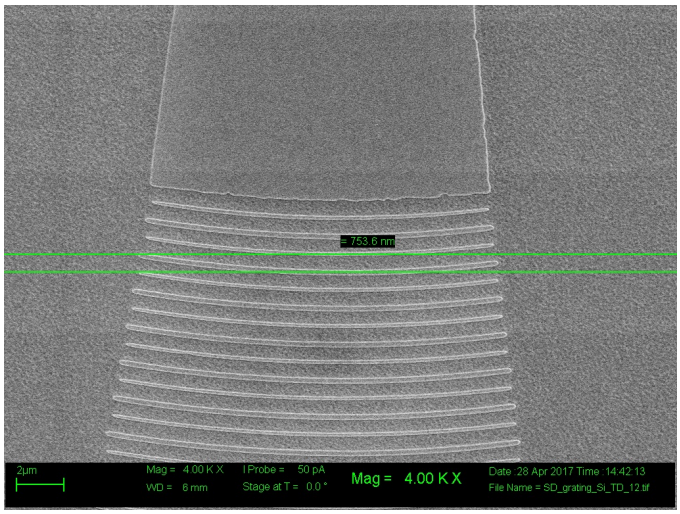


(a) Single litho layer pitch measurement.

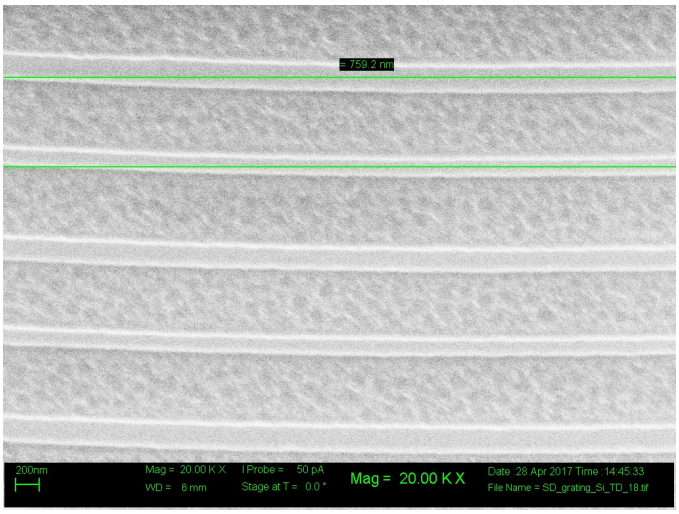


(b) Single litho layer pitch measurement zoomed.

Fig. 35: Measurements taken on SEM images of pitch for a single lithography layer.



(a) Compound litho pitch measurement.



(b) Compound litho pitch measurement zoomed

Fig. 36: Measurements taken on SEM images of pitch for a the compound lithography image.

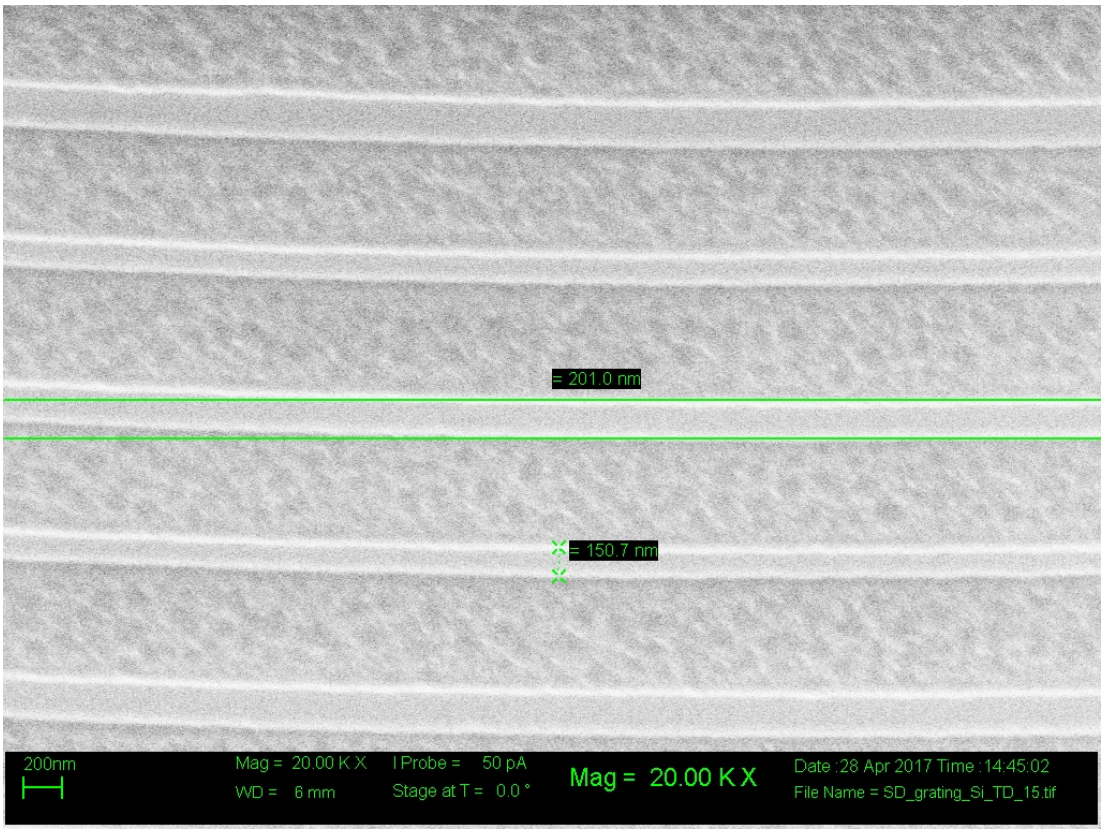


Fig. 37: Measurements taken on SEM images of feature widths in grating coupler.

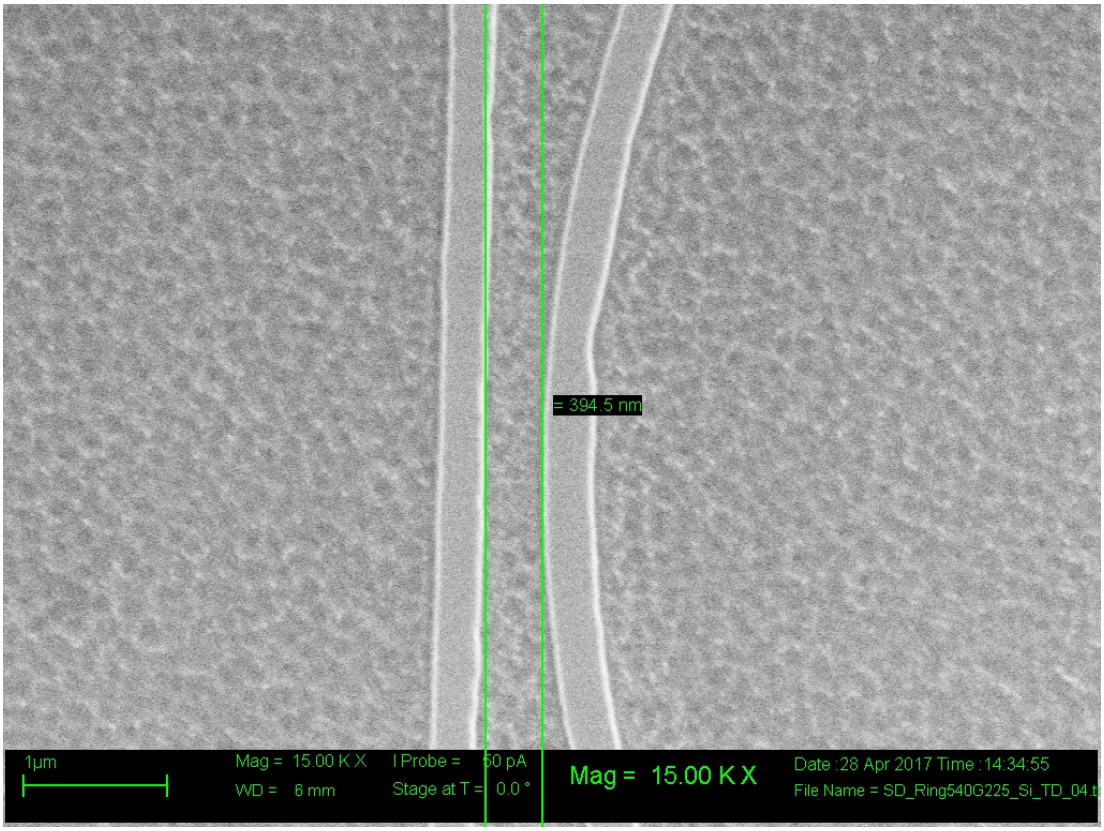


Fig. 38: Measurements taken on SEM images of ring to waveguide gap.

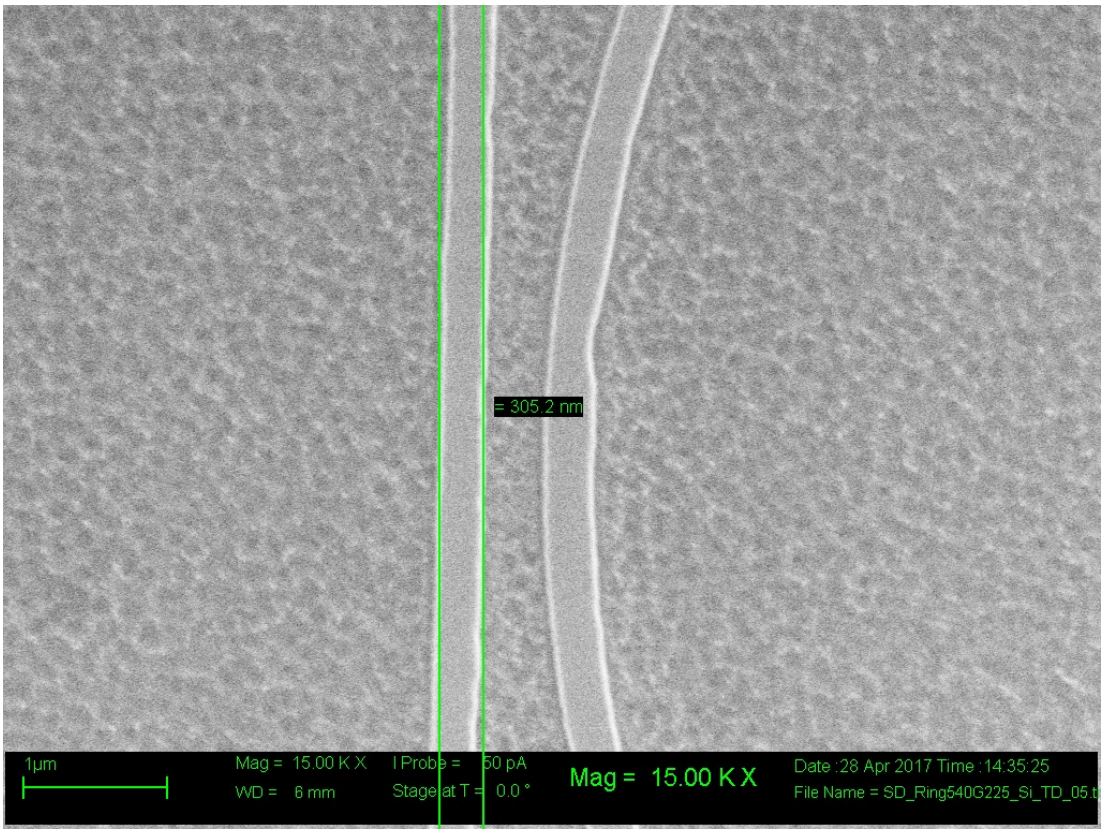


Fig. 39: Measurements taken on SEM images of feature widths in ring resonator device.

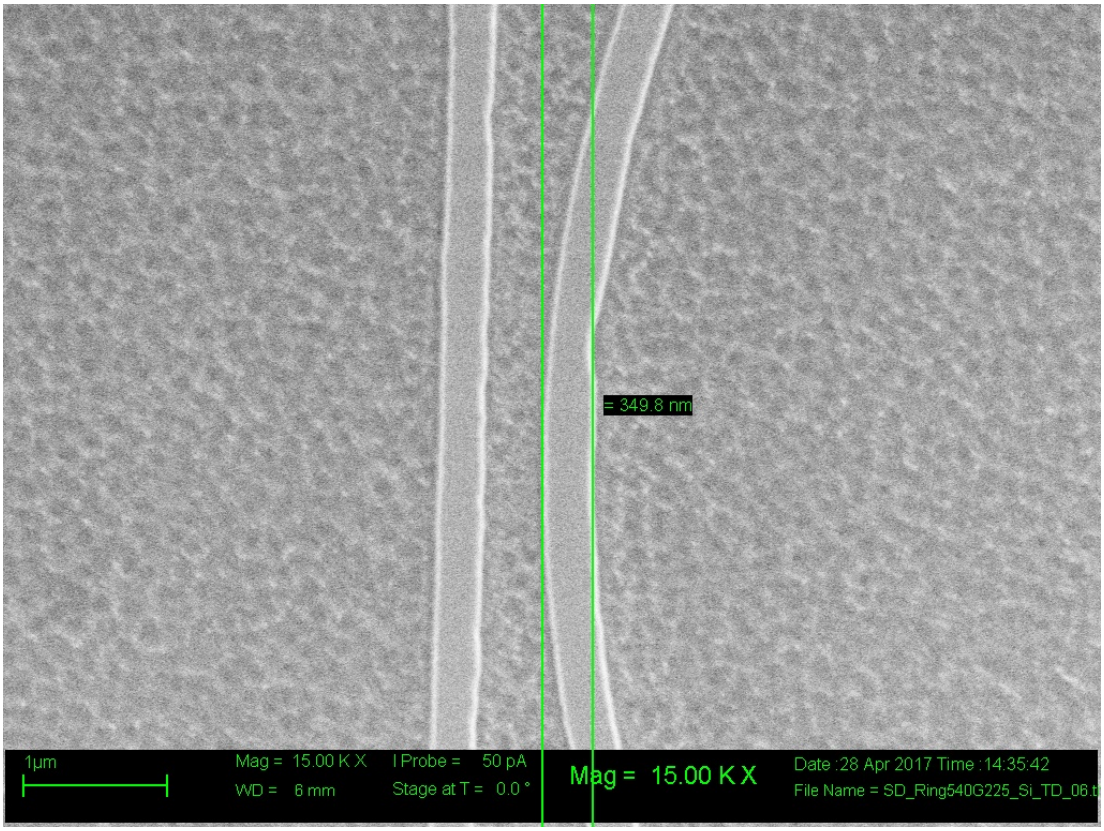


Fig. 40: Measurements taken on SEM images of feature widths in ring resonator device.

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