

# Process Development of Sidewall Spacer Features for sub-300nm Dense Silicon FinFETs

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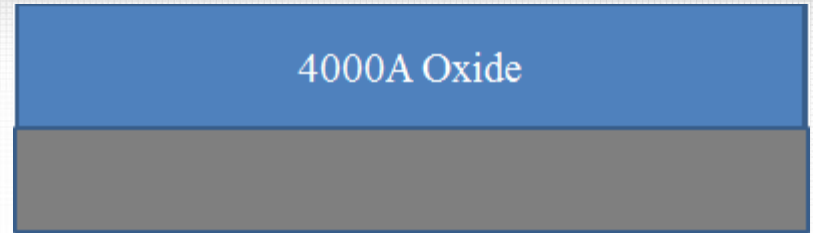
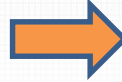
# Overview

To achieve uniform sub-300nm critical dimensions for future FinFETs. A process was developed to demonstrate lithography techniques which utilize resist overexposure, an aluminum hard mask, nitride sidewall spacers and, finally, a reactive ion etch to transfer the nitride patterns to the silicon.

# Proposed Process Flow



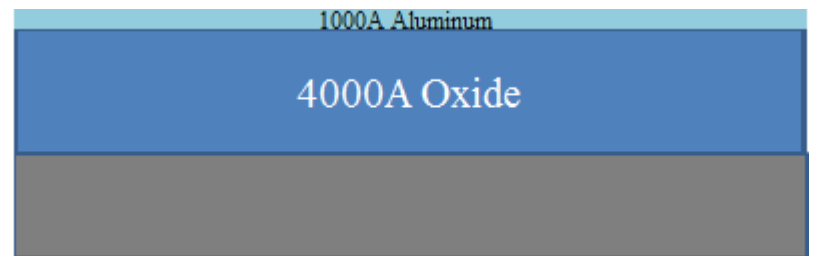
- Wafer cleaning.



- Thermally grow 4000Å wet SiO<sub>2</sub>.

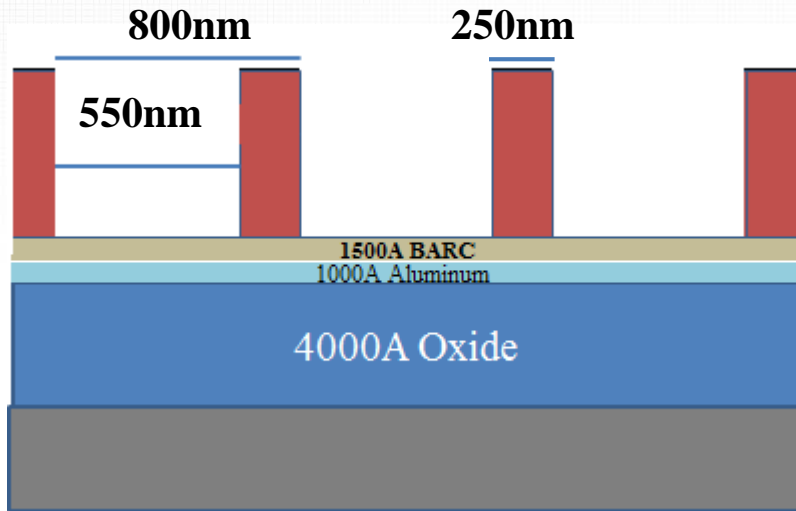


- Spin coat I-CON 7 BARC @ 1500Å.
- Spin coat diluted OiR620 PR @ 5600Å.

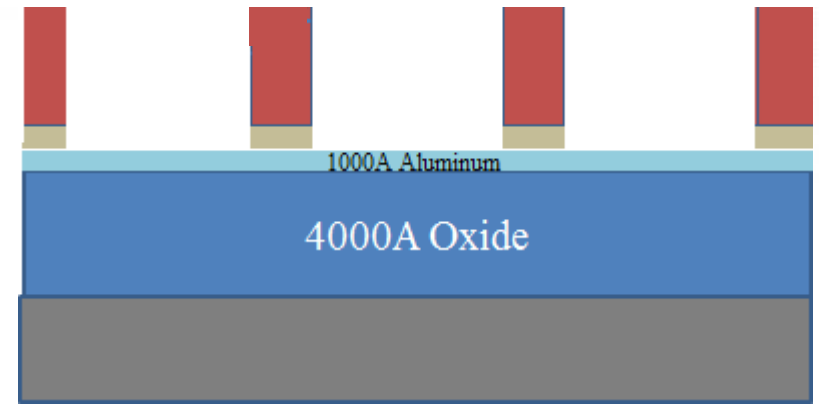
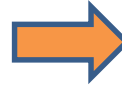


- Deposit ~1000Å of pure aluminum.

# Proposed Process Flow

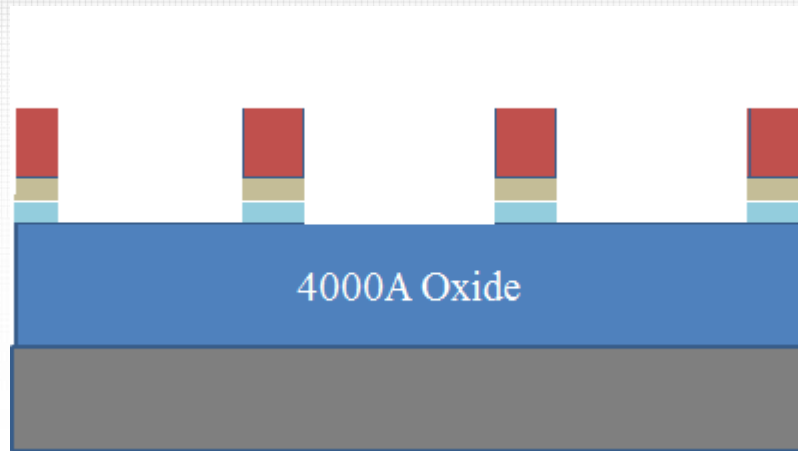


➤ Expose FEM to determine the desired over-exposure dose and focus.

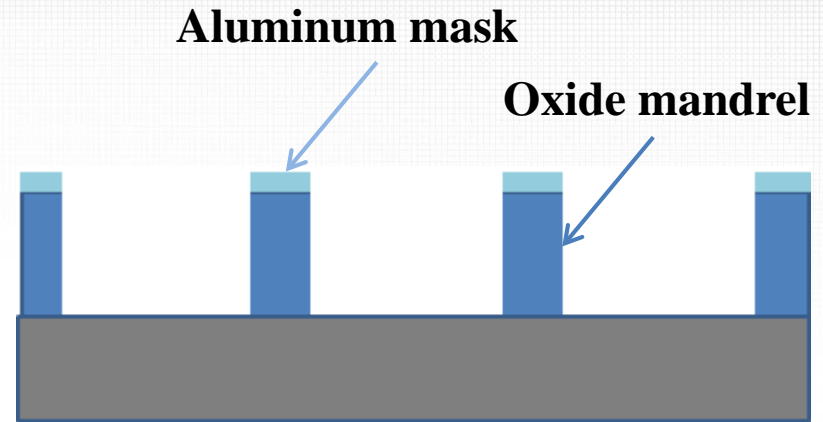


➤ RIE BARC.

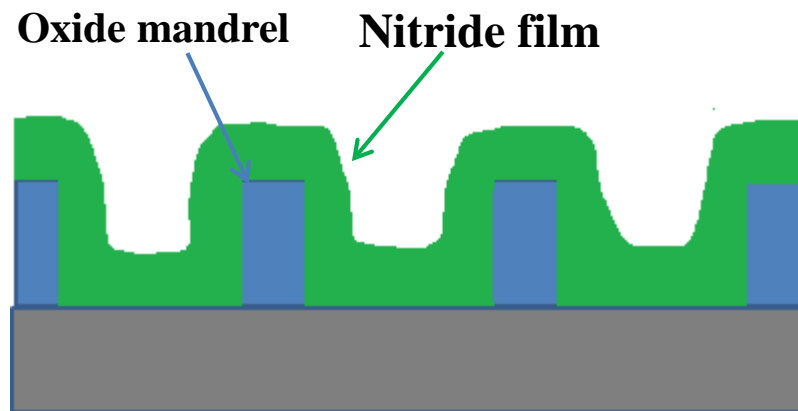
# Proposed Process Flow



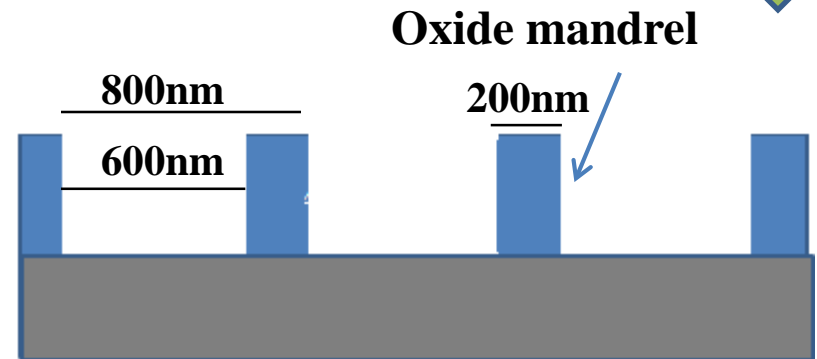
➤ RIE aluminum.



➤ RIE oxide.

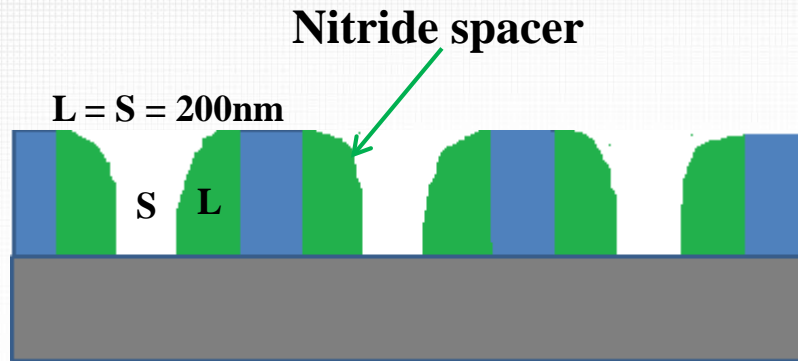


➤ Deposit 2000Å of nitride.

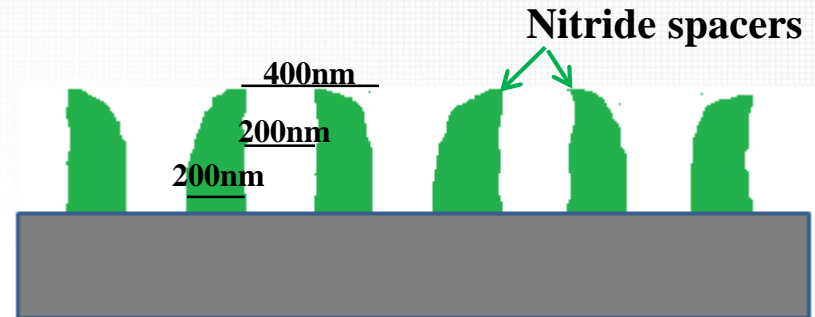
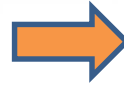


➤ Strip aluminum.

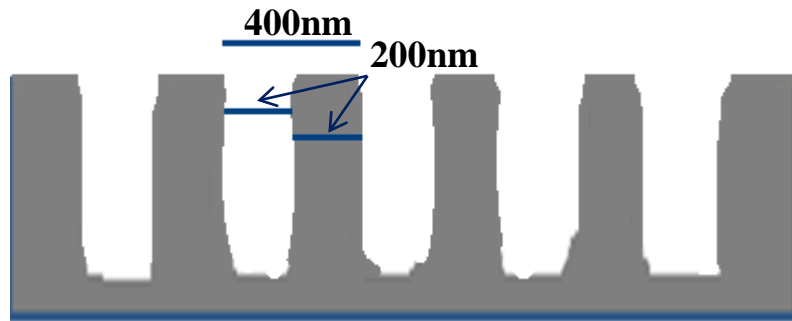
# Proposed Process Flow



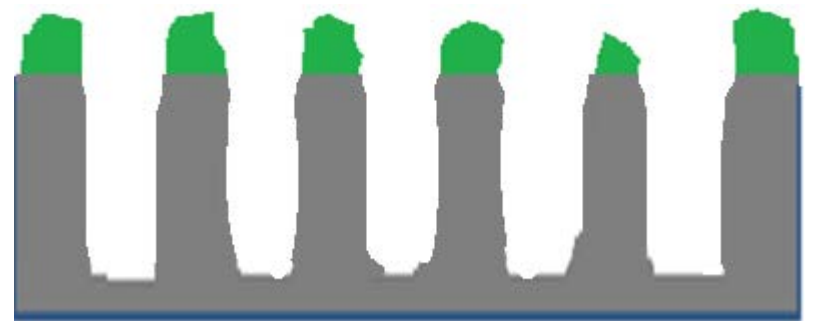
➤ RIE nitride.



➤ Strip oxide.



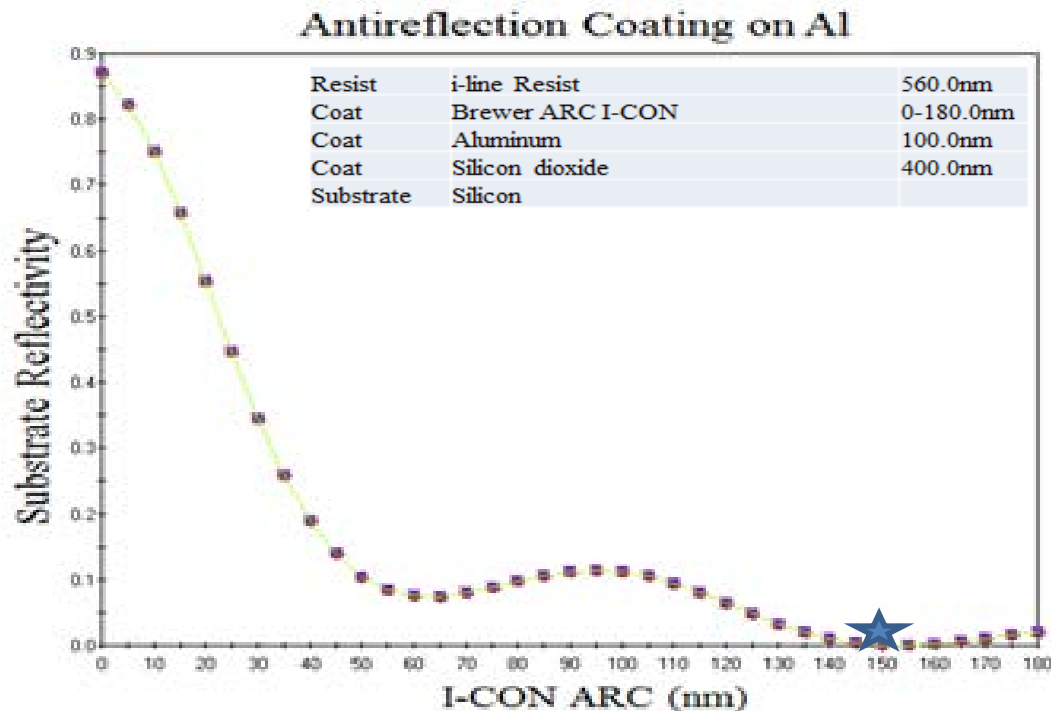
➤ Strip nitride.



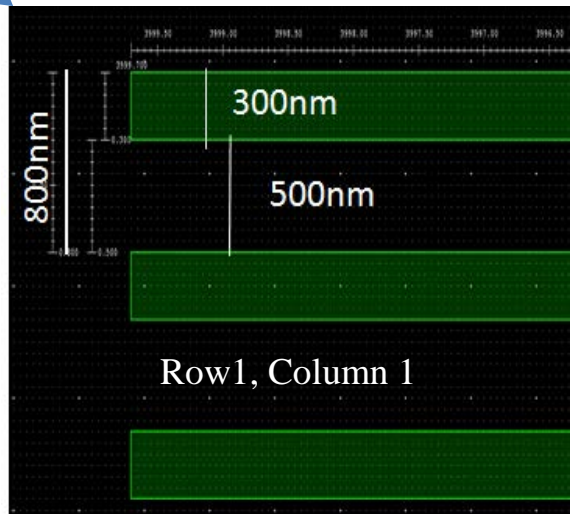
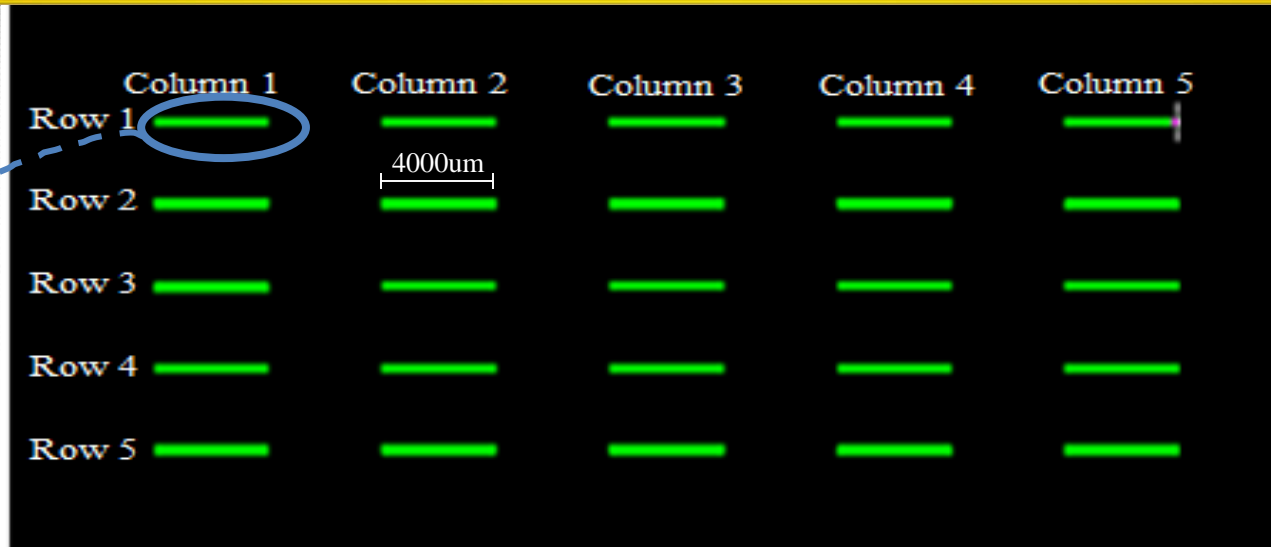
➤ RIE Silicon.

## Optimizing BARC for Minimum Reflectivity

- The PROLITH swing curve simulation for the resist on BARC on aluminum that resulted in high contrast features that can be transferred to the aluminum.
- Optimal BARC thickness is found to be 150nm for the OiR620 thickness.



# Mask Design – Various Pitch and Duty Cycles



		Column 1	Column 2	Column 3	Column 4	Column 5
Row1	L (nm)	300	300	300	300	300
	S (nm)	500	450	400	350	300
	P (nm)	800	750	700	650	600
Row2	L (nm)	350	350	350	350	350
	S (nm)	500	450	400	350	300
	P(nm)	850	800	750	700	650
Row3	L (nm)	400	400	400	400	400
	S (nm)	500	450	400	350	300
	P (nm)	900	850	800	750	700
Row4	L (nm)	450	450	450	450	450
	S (nm)	500	450	400	350	300
	P (nm)	950	900	850	800	750
Row5	L (nm)	500	500	500	500	500
	S (nm)	500	450	400	350	300
	P (nm)	1000	950	900	850	800

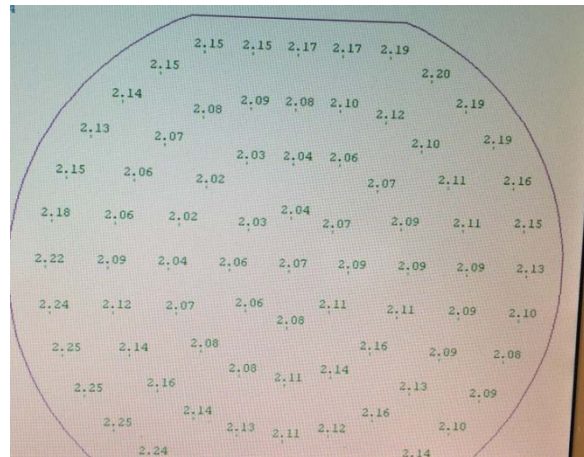


# Oxide Growth and Aluminum Deposition

- Oxide growth: A 4000Å layer of thermal oxide was grown on of the process wafers.

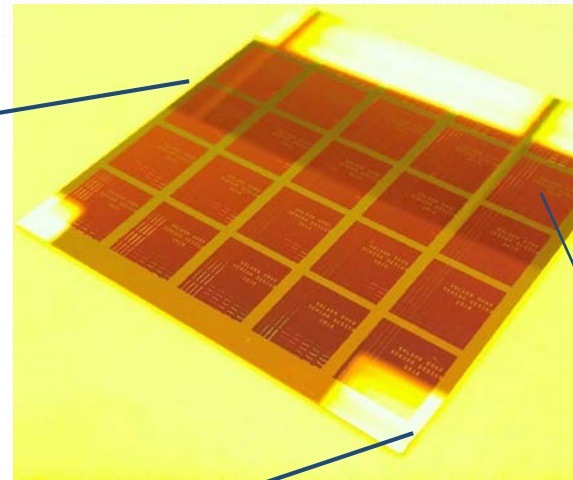
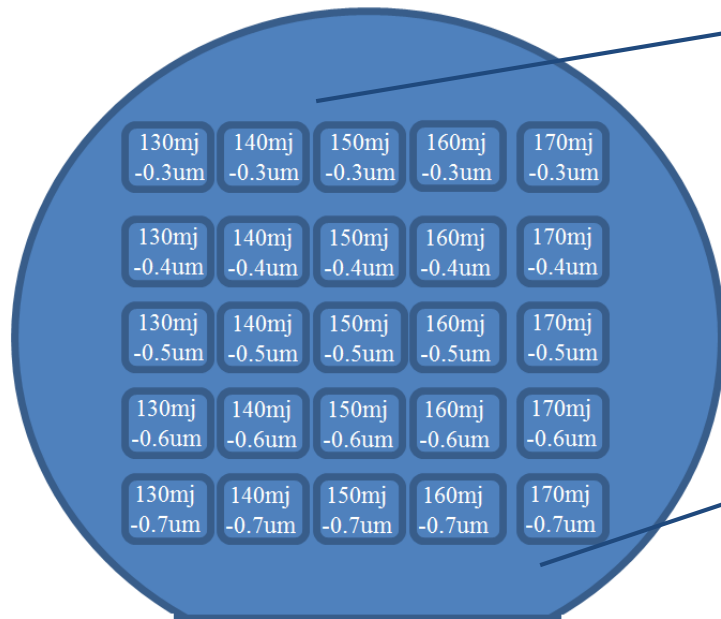
Wafer ID	Mean (Å)	Std.dev.	Min (Å)	Max (Å)	Range (Å)
A1	3982.3	23.3 (0.58%)	3941	4042	101
A2	3994.3	23.0 (0.57%)	3951	4043	92
A3	3961.4	21.0 (0.52%)	3925	4005	80.3
A4	3980.3	22.0 (0.54%)	3937	4019.7	82.8

- Aluminum thickness measurement (via SEM): ~1300Å, used with Resmap data to determine a thickness standard deviation of 2.7%.

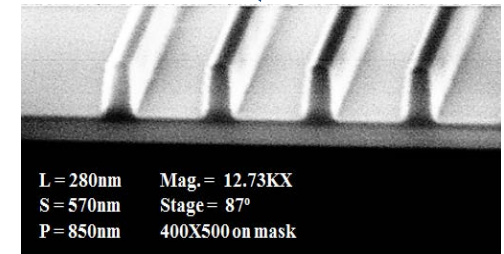


# Focus Exposure Matrix (FEM)

Focus-Exposure-Matrix (FEM) was performed to analyze the process latitude of the ASML stepper. Center dose is set at  $150\text{mj} \pm 10\text{mj}$  and center focus is set at  $-0.5\mu\text{m} \pm 0.1\mu\text{m}$ . Numerical aperture value is set to 0.6, sigma inner and outer are set to 0.535 and 0.9, respectively.



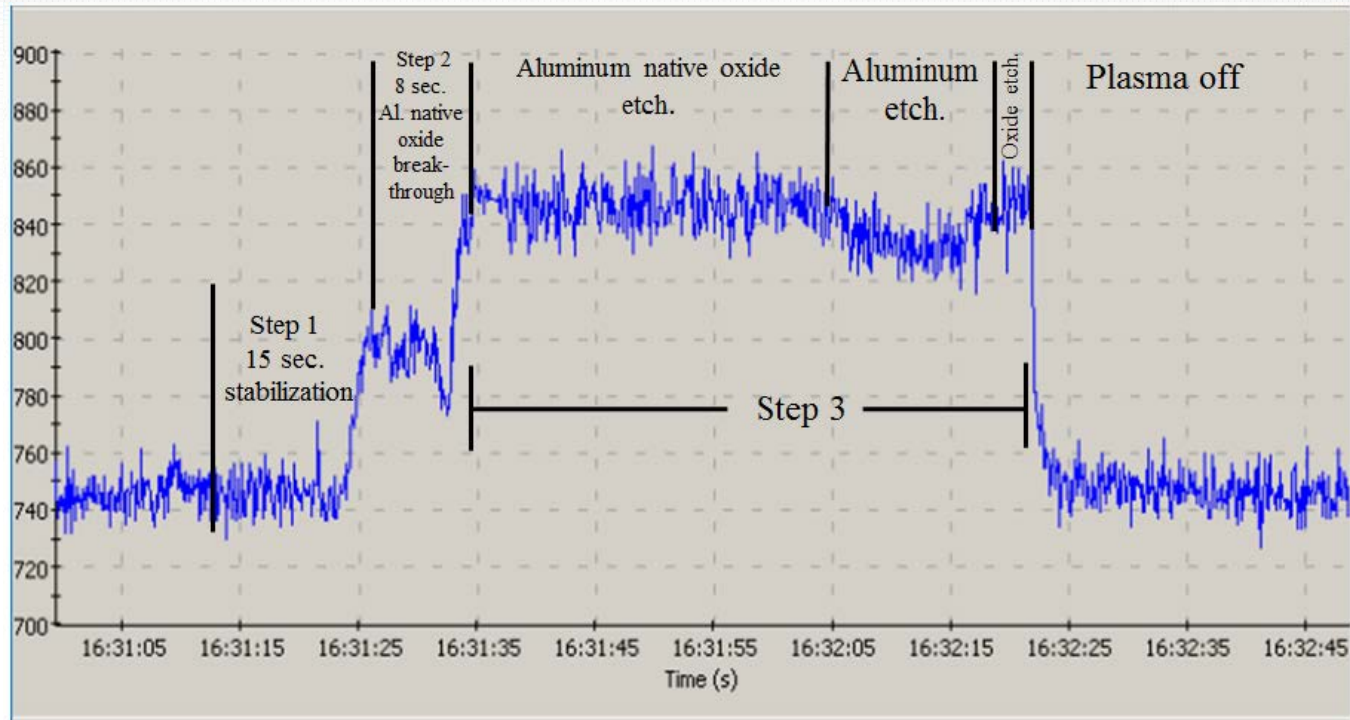
Cleaved wafer



The best dose and focus is found to be optimal at 170mj and  $-0.4\mu\text{m}$ , where it overexposed the desired 400X500nm features on mask to be 280X570nm L/S.

# Aluminum Etch (Intensity Profile)

SpectraSuite software is used to detect the intensity profile.

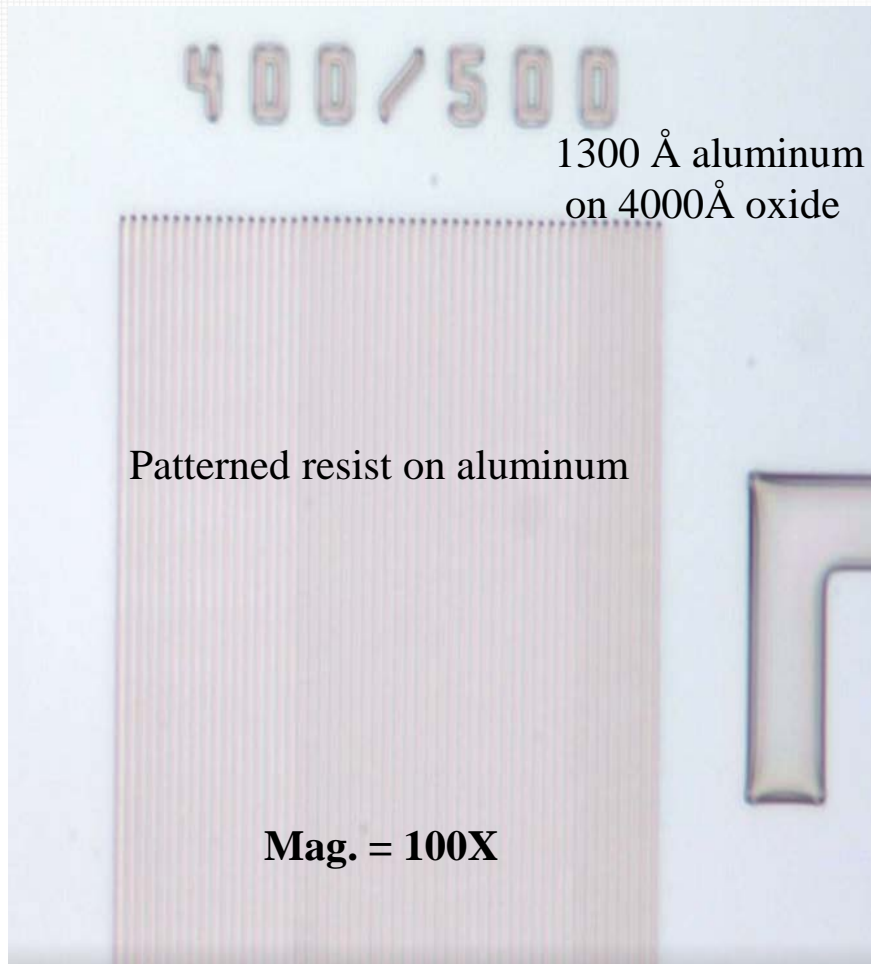


- **Step 1:** 15 second stabilization step to flow the appropriate gases.
- **Step 2:** Initial aluminum native oxide breakthrough for 8 seconds.
- **Step 3:** More aluminum native oxide breakthrough + actual etch of the 1300Å aluminum layer.
- **Endpoint:** The run is terminated once the bottom oxide etch is observed.

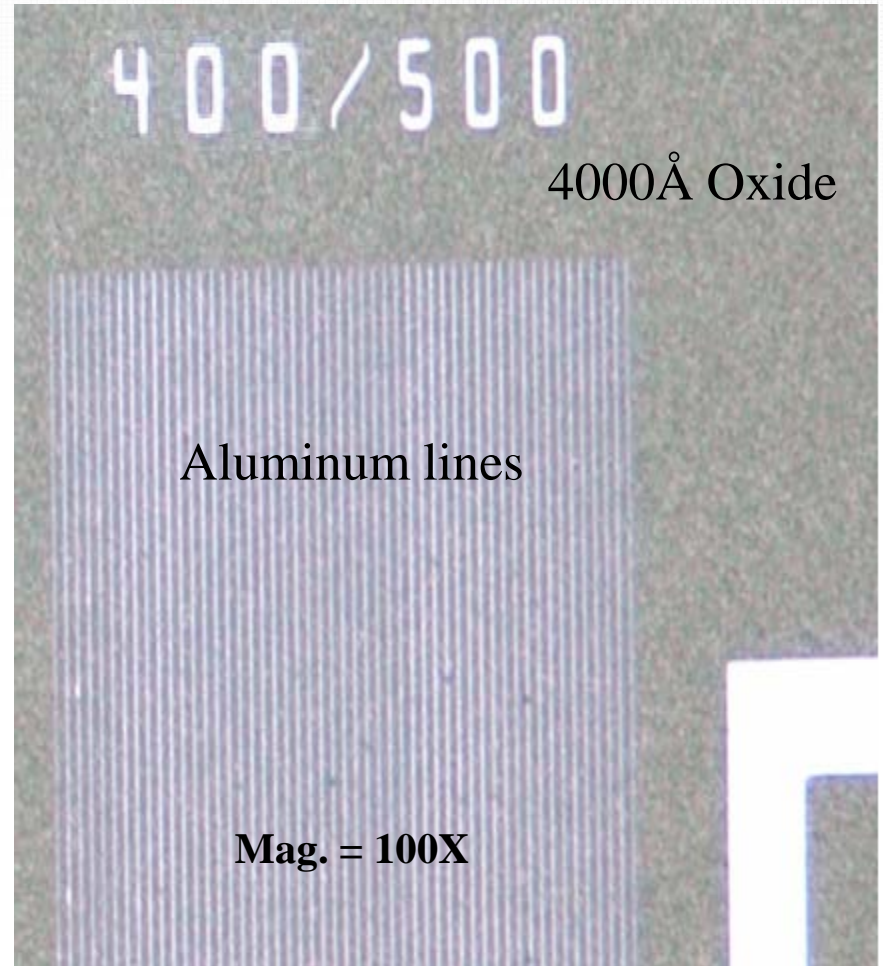


# Aluminum Etch (OM)

Before aluminum etch

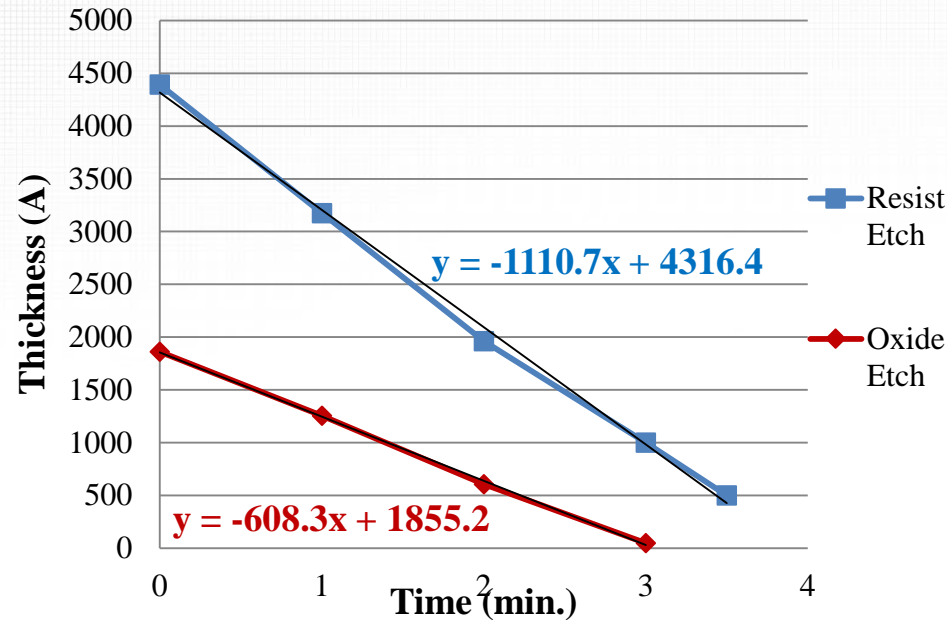


After aluminum etch (Using Endpoint detection)



# Oxide Etch Rate

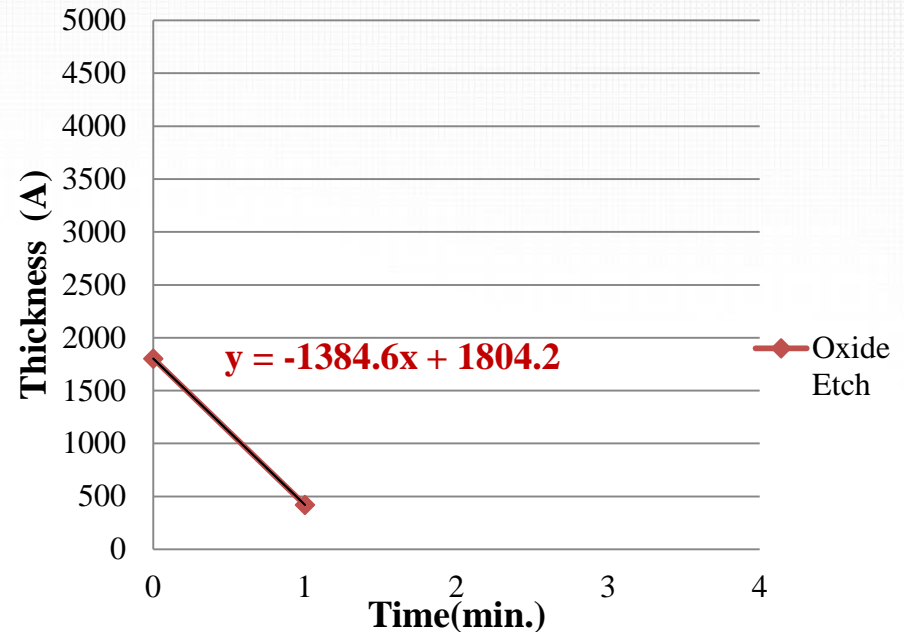
## DryTek Oxide Etch Rate with PR Mask



Oxide etch rate:  $\sim 608 \text{ \AA/min.}$

Photoresist etch rate:  $\sim 1111 \text{ \AA/min.}$

## P-5000 Oxide Etch Rate with Al Hard Mask



Oxide etch rate:  $\sim 1385 \text{ \AA/min.}$

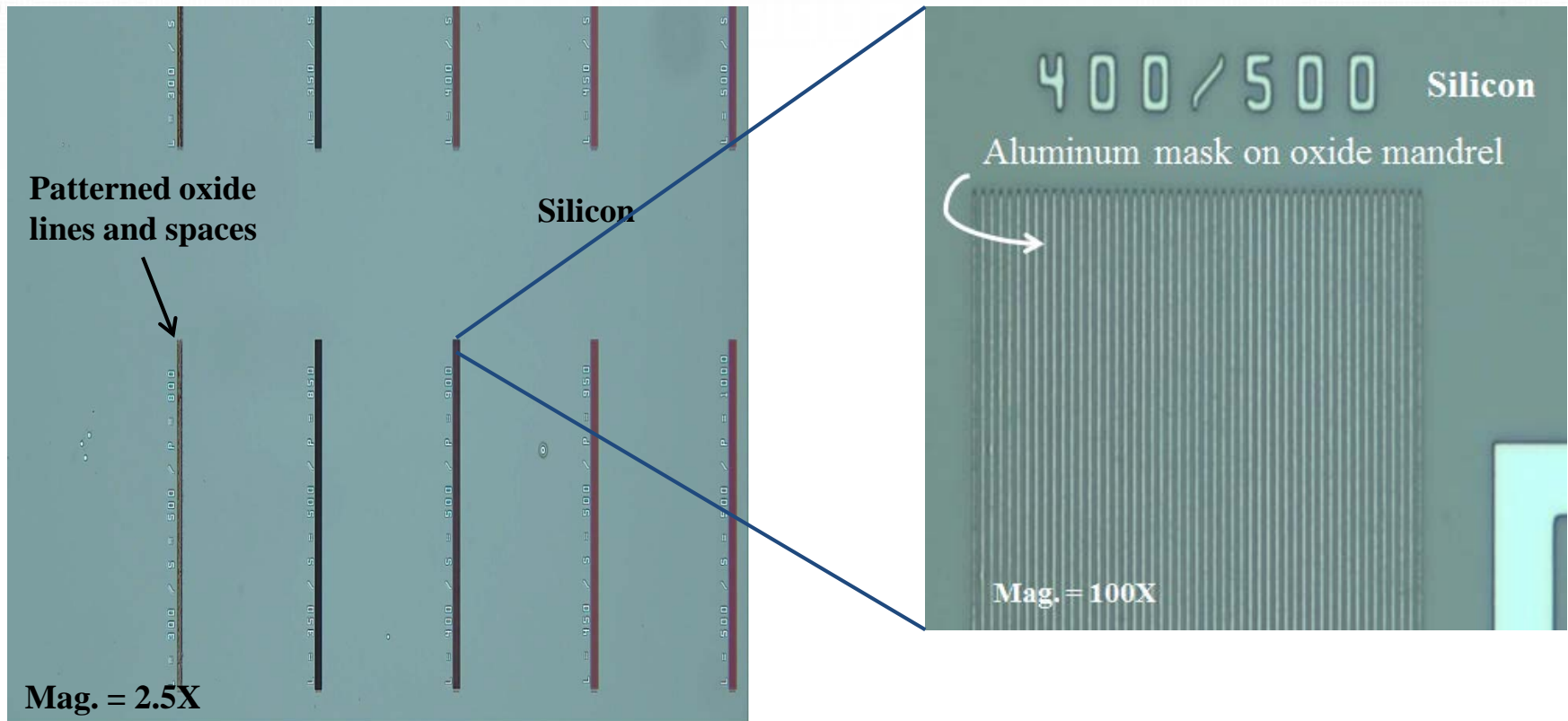
Oxide etch rates were performed on dummy wafers.

# Oxide Etch in P-5000 Chamber C with Al Mask (OM)

## P-5000 Chamber C (With pure aluminum mask)

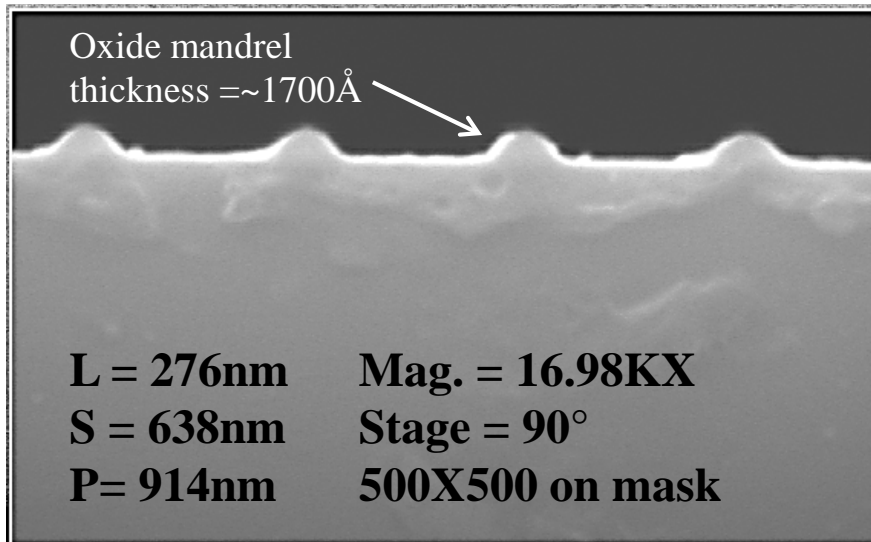
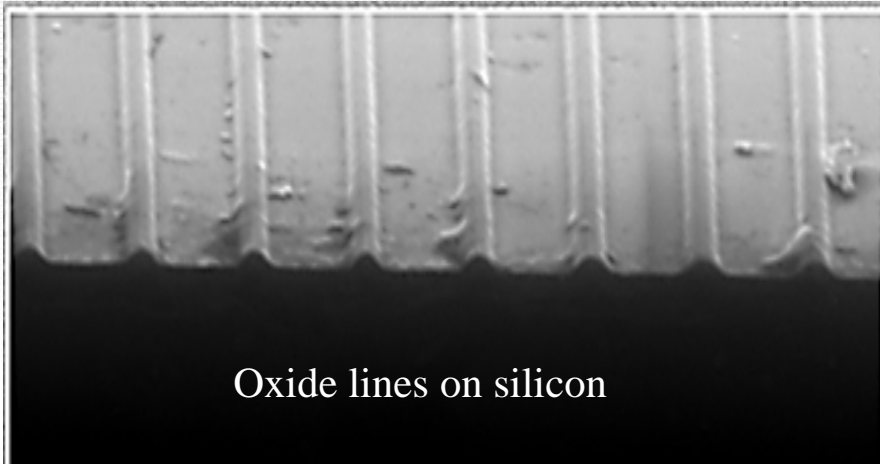
Run 1: 170sec. → Cleared (4000Å oxide).

Pictures bellow show successful oxide RIE patterning with the evaporated aluminum mask.

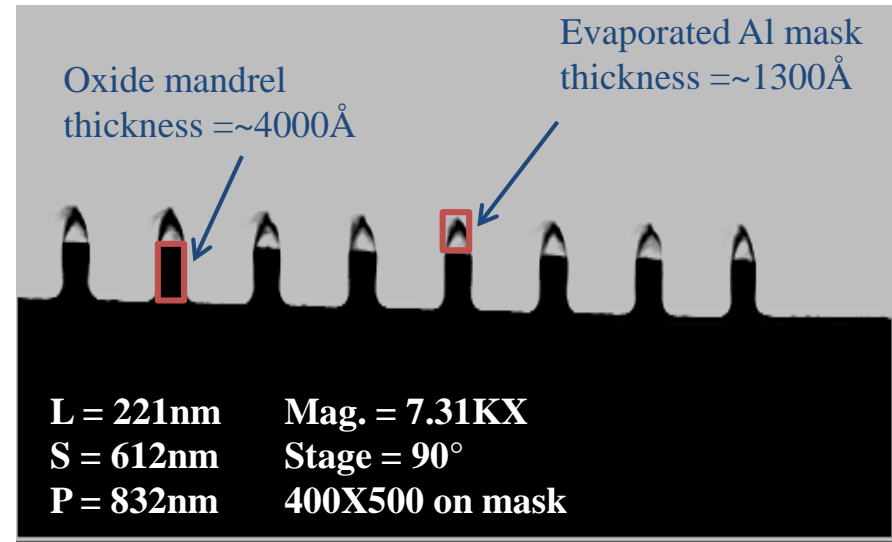
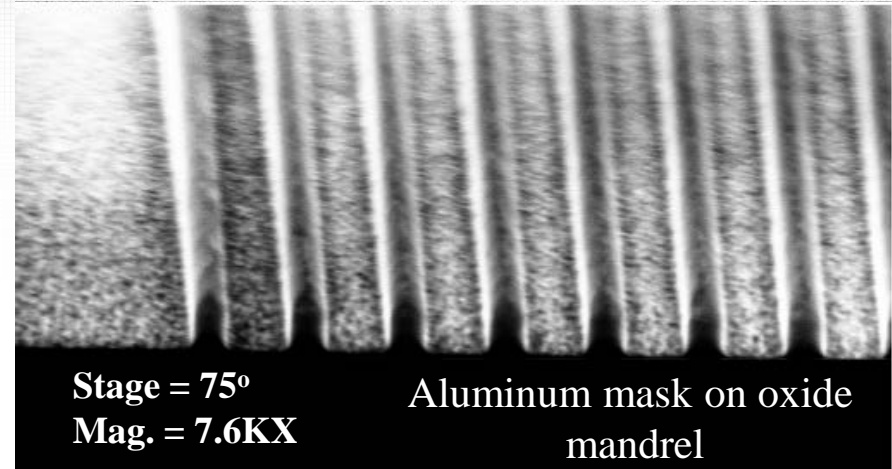


# Oxide Etch in DryTek Chamber vs. P-5000 Chamber C (SEM)

DryTek Quad Chamber 3 (oxide etch using photoresist mask)



P-5000 Chamber 3 (oxide etch using Aluminum mask)





# Nitride Deposition

## Nitride deposition recipe:

Tool	LPCVD Furnace
Recipe	Nitride 810C
Base Pressure	68mT
Dep. Pressure	297mT
DCS	160sccm
NH3	190sccm
Time	33 min.
Measured Thickness	$\sim 1800\text{\AA}$
Measured Dep. Rate	$\sim 55\text{\AA}/\text{min}$



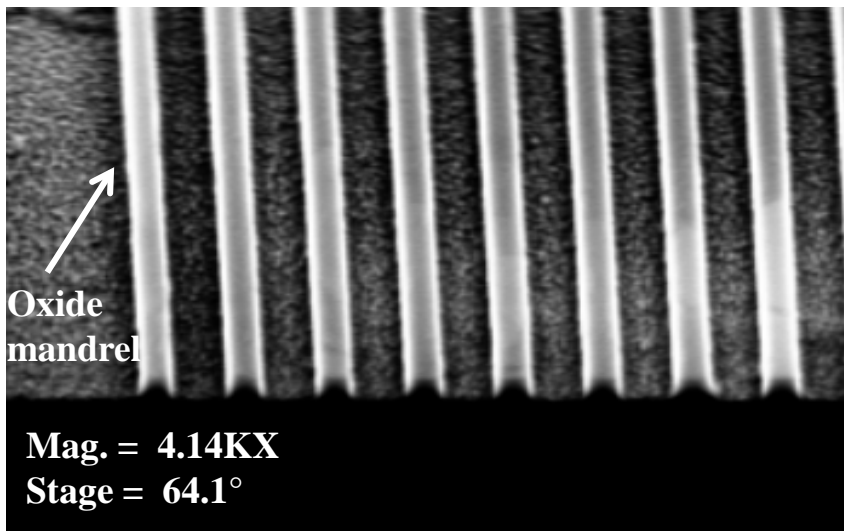
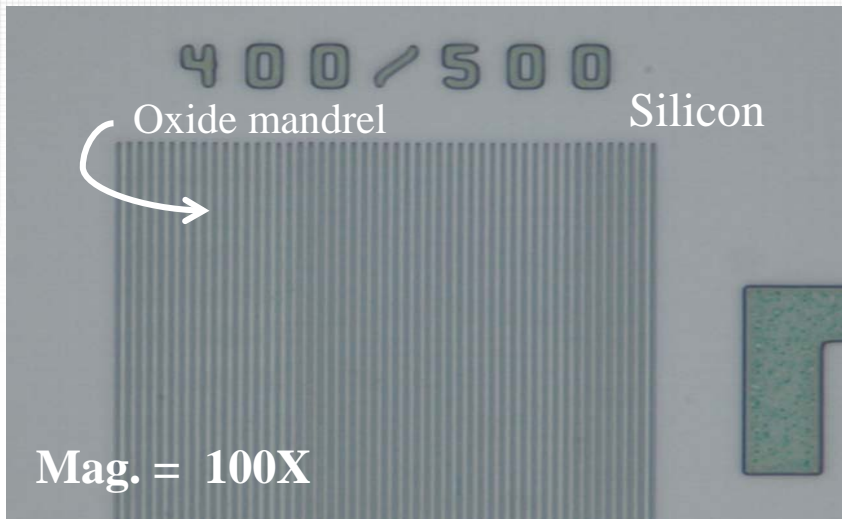
**ASM LPCVD Furnace.**

device wafers + 1 monitor wafer with  $4000\text{\AA}$  oxide.

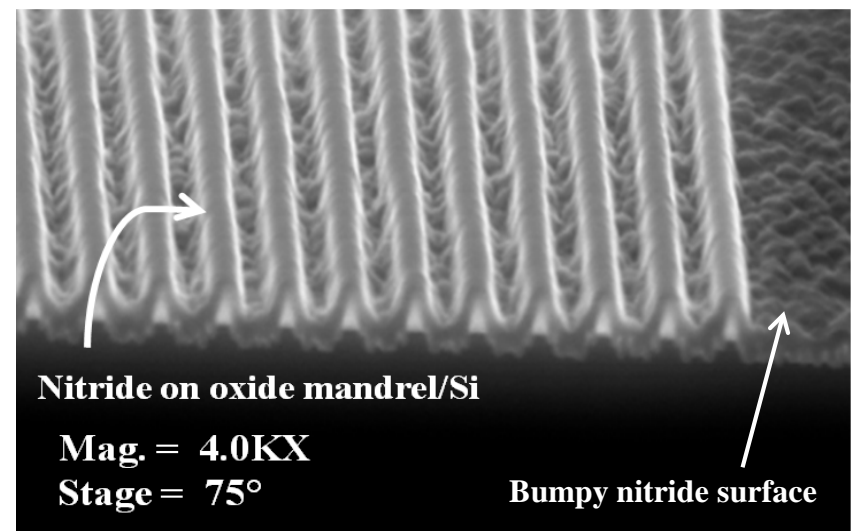
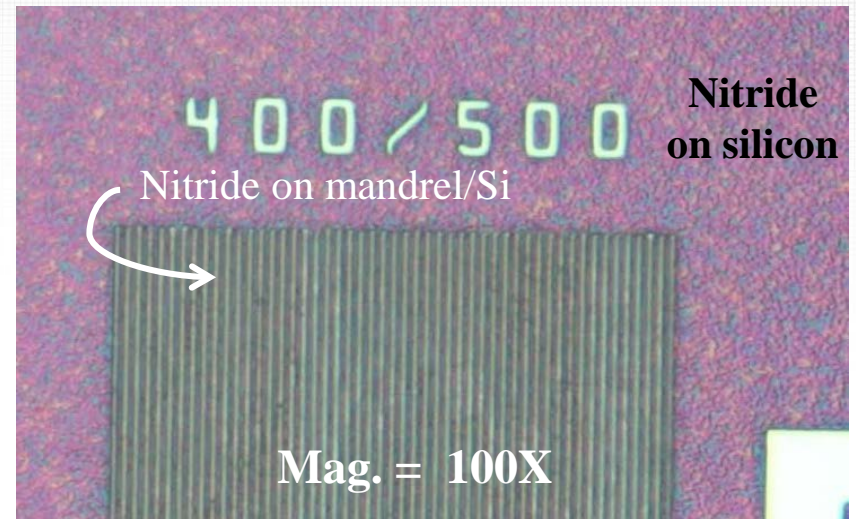


# Nitride Deposition (Cont.)

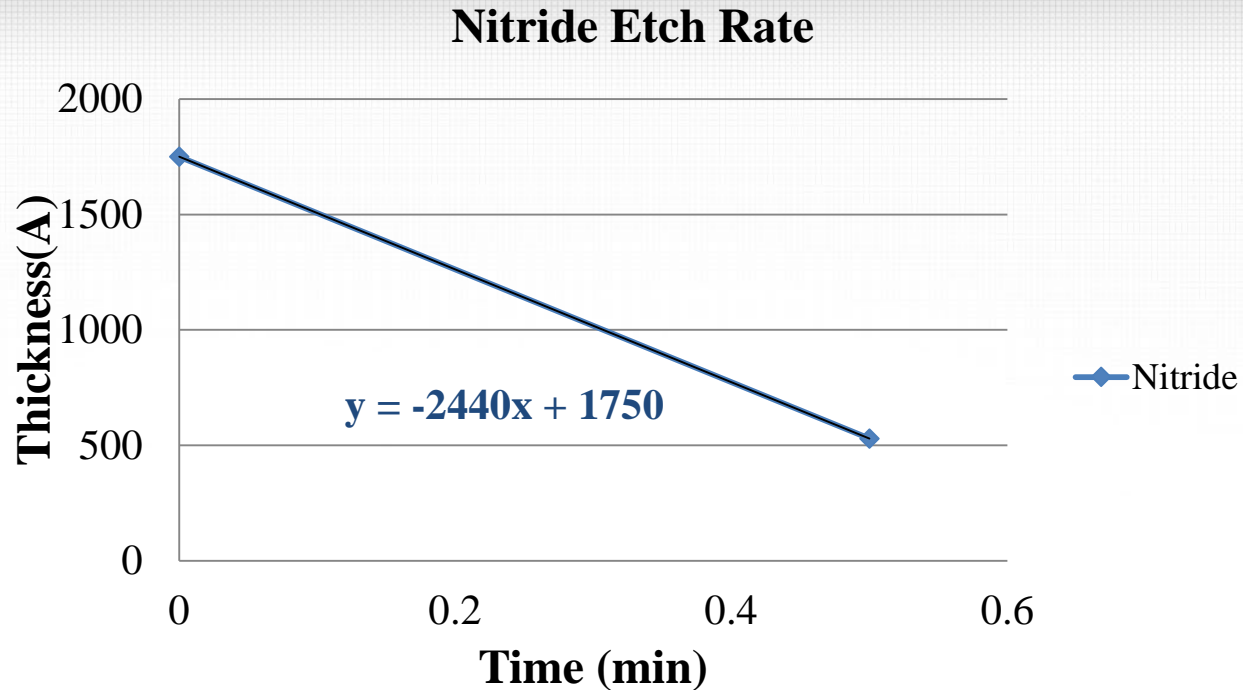
## Oxide lines on silicon



## Nitride deposition on oxide and silicon



# Nitride Etch



## Recipe:

Tool: Drytek Chamber 2.

Power : 250W.

Pressure: 40mT.

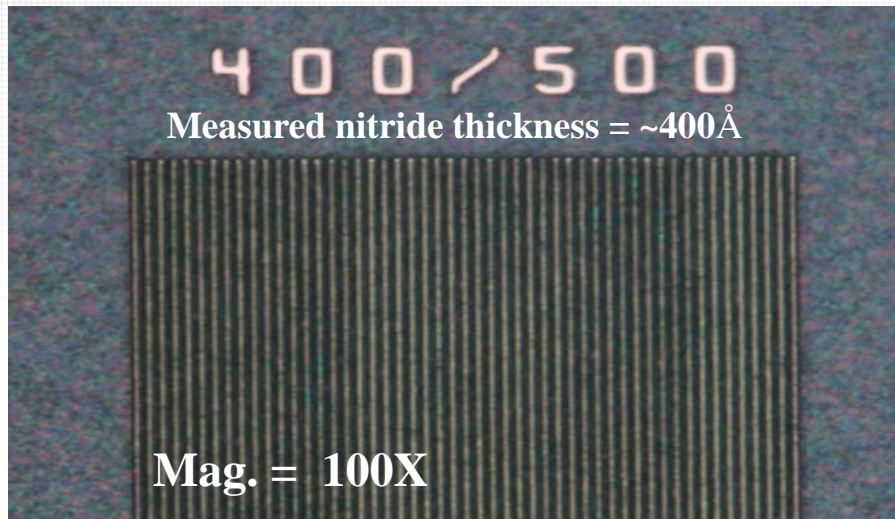
CHF3: 30 sccm.

SF6: 30 sccm.

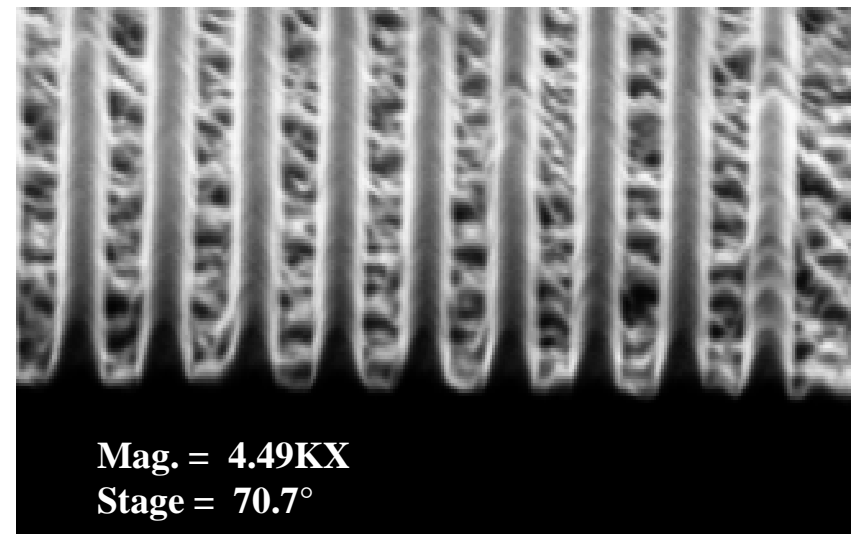
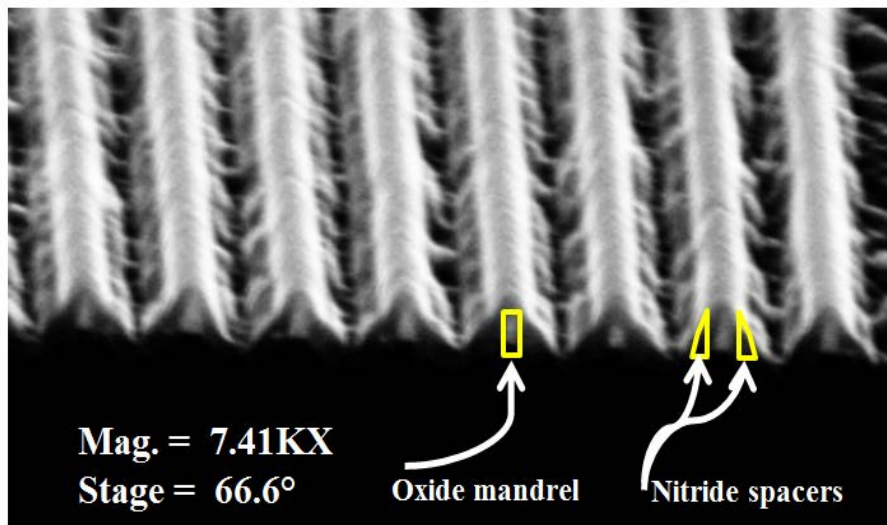
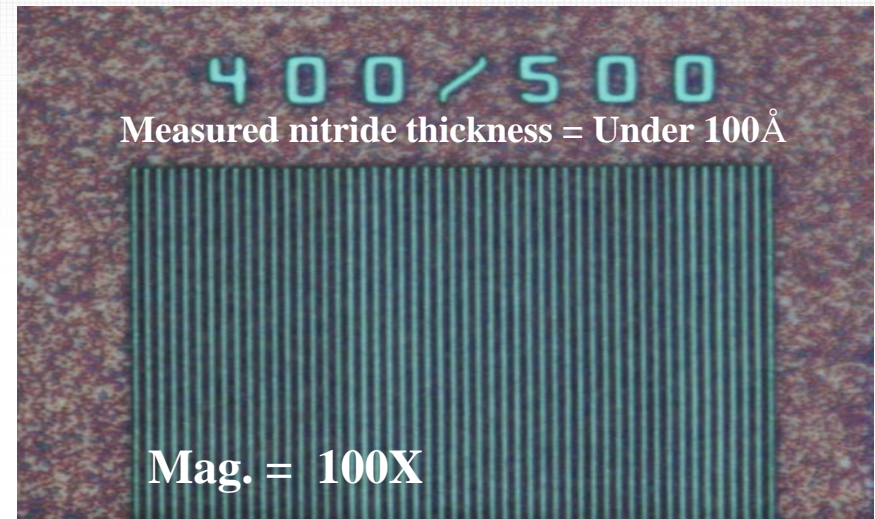
Etch rate:  $\sim 2440 \text{ \AA/min.}$

# Nitride Etch (Cont.)

30 seconds etch (Under etched)



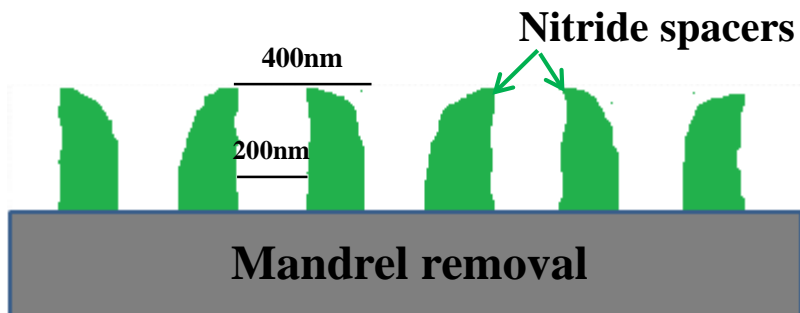
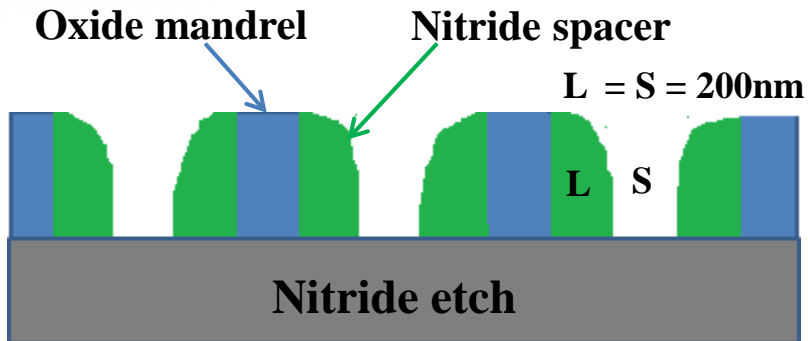
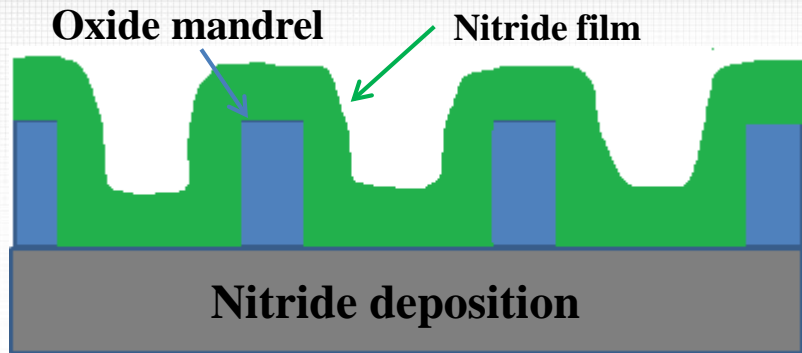
40 seconds etch (Over etched)



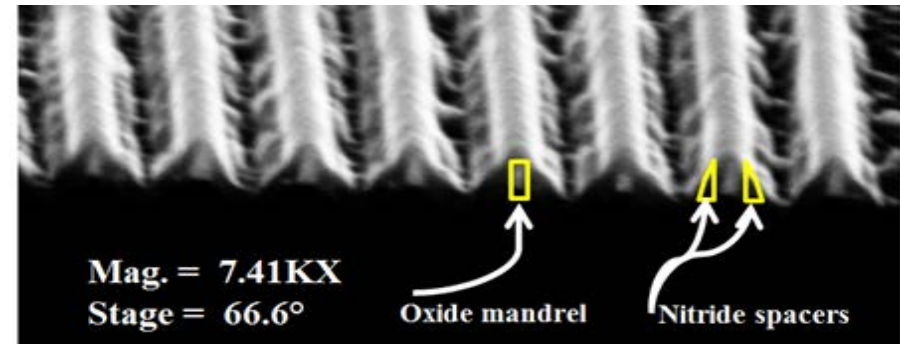
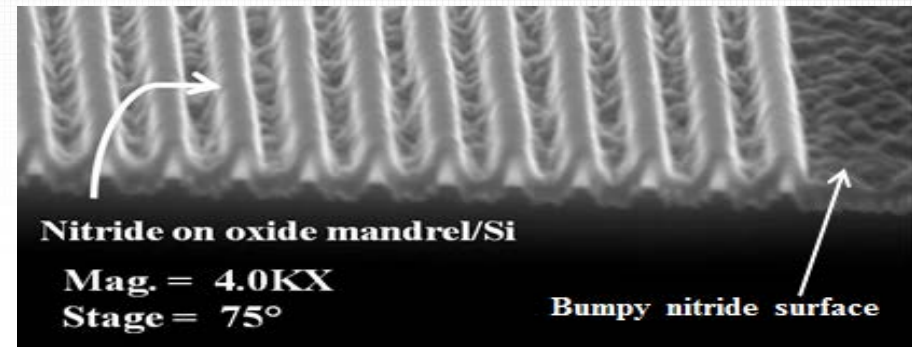


# Nitride Deposition & Etch (Proposed vs. Actual)

## Proposed



## Actual



?

# Summary

- Patterning through annular illumination is successful to image 280nm CD.
- Aluminum hard mask is excellent for oxide patterning with an anisotropic profile.
- Aluminum over-etch proved beneficial for achieving a 211nm mandrel CD .
- Nitride deposition shows a conformal yet textured profile over the oxide mandrel.
- Nitride etch resulted in non-uniform opening between nitride sidewall spacers due to the previous nitride deposition texture.
- DOE is required for the nitride deposition and etch for optimal sidewall profile.
- Due to the project constraints, the silicon etch process was not completed.

## Future Work

- Continue this investigation to develop a full fabrication process and electrically characterize finFET devices.
- Consider utilizing a hard mask under the nitride spacer to be transferred to the silicon.

## References

- [1]C. Shay, "CD Reduction through Annular Illumination and Sidewall Spacer Etch," ed. Rochester Institute of Technology, 2016.
- [2]Development and Simulation of Sublithographic Process for nm Scale Features, 1st ed. Rochester: Wallace Memorial Library, 2010, pp. 57 – 84.
- [3]E. Bowser, "Double Patterning Isolated and Dense Features With An ASML PAS 5500 i-Line Stepper," ed. Rochester Institute of Technology, 2013.