Development of a LFLE Double Pattern Process for TE Mode Photonic Devices

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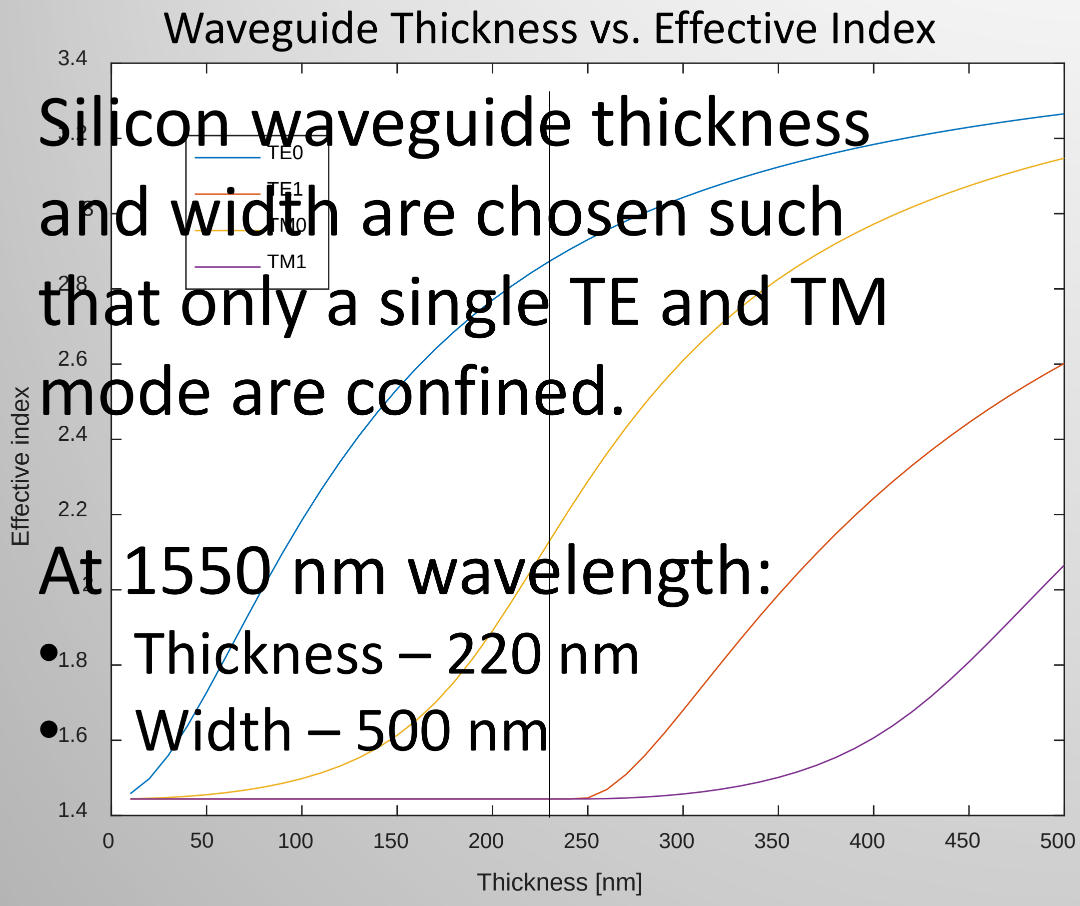
Introduction and Motivation

Silicon Photonics Geometry, TE vs TM, Double Pattern vs Single Pattern

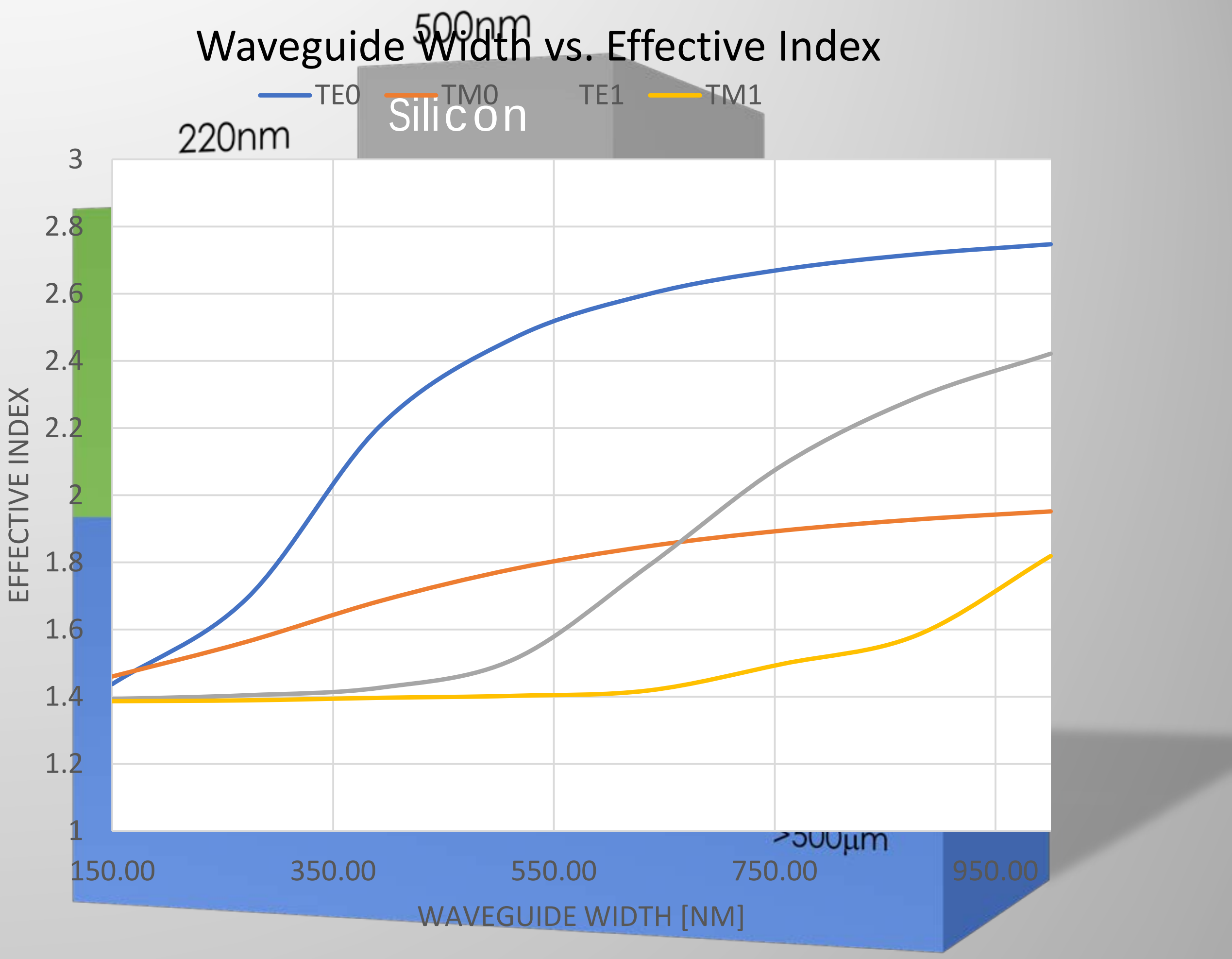
Silicon Photonics Geometry



Silicon waveguide thickness and width are chosen such that only a single TE and TM mode are confined.

At 1550 nm wavelength:

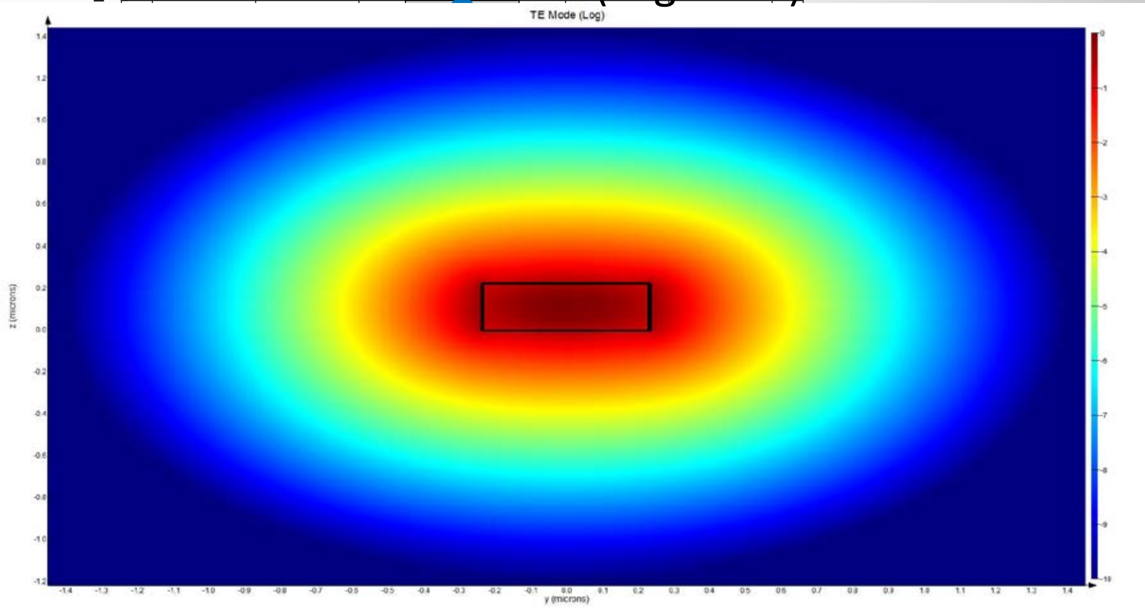
- Thickness – 220 nm
- Width – 500 nm



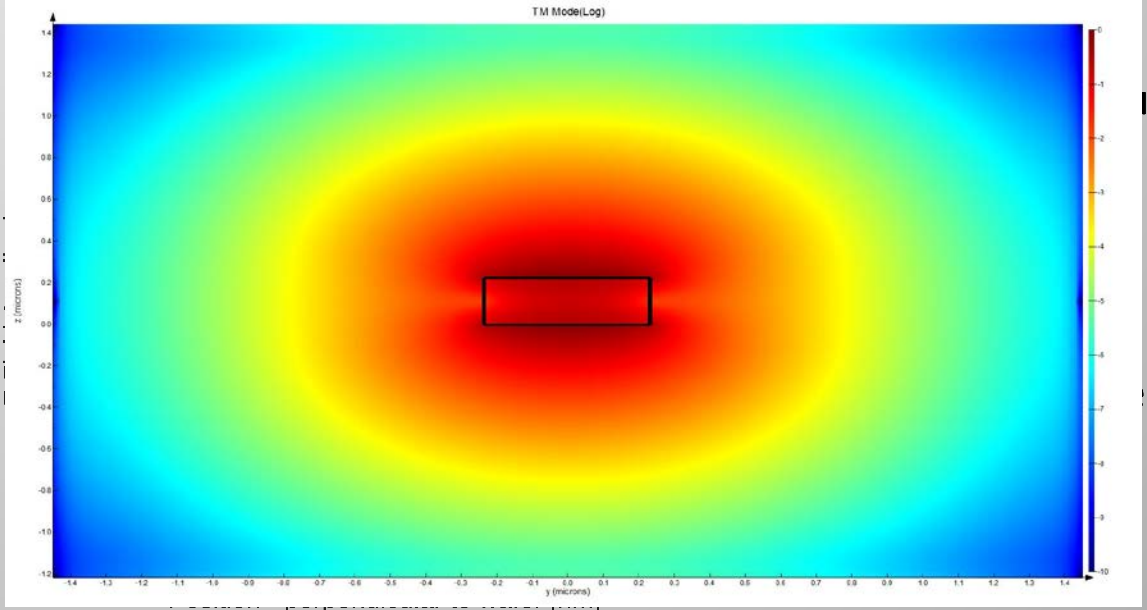
[1] S.Preble, “Waveguides: Silicon Waveguides”, MCEE-789/EEEE-789, Powerpoint, Spring 2165

TE Mode vs TM Mode

TE Mode E-Field (Log Scale)



TM Mode E-Field (Log Scale)



Photonic devices take advantage of optical tunneling of the evanescent field to couple energy from one waveguide to another.

TM Mode contains a larger amplitude evanescent field allowing coupling over larger distances

[1] S.Preble, “Waveguides: Silicon Waveguides”, MCEE-789/EEEE-789, Powerpoint, Spring 2165

Double Pattern vs Single Pattern (Using i-line Lithography)

Double Pattern

- Minimum feature size possible:
  - ~250 nm
- Minimum feature separation possible:
  - ~100 nm

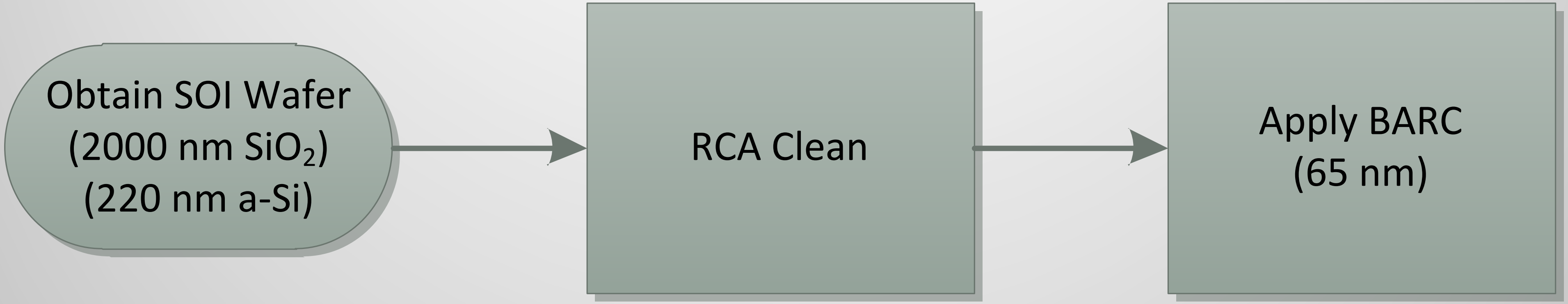
Single Pattern

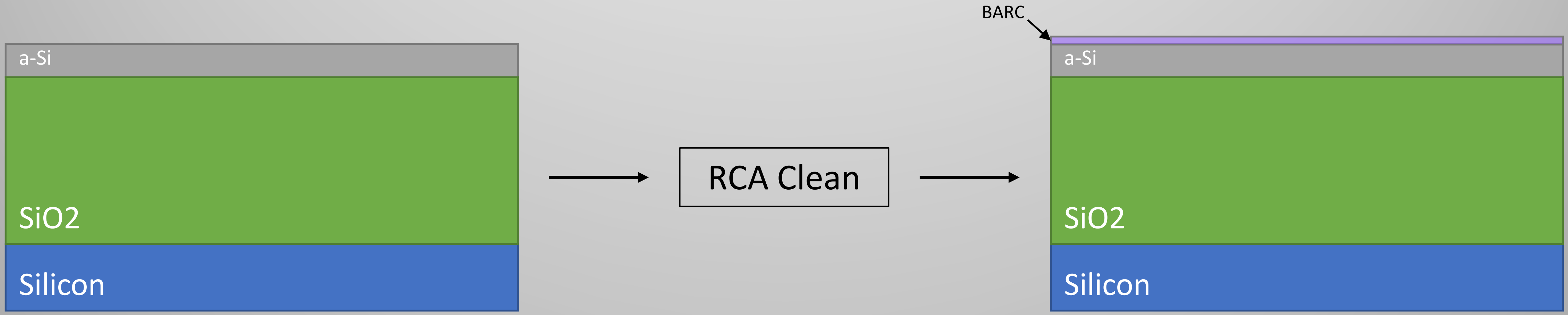
- Minimum feature size possible:
  - ~400 nm
- Minimum feature separation possible:
  - ~300 nm

Process Development

Proposed Litho-Freeze-Litho-Etch Process

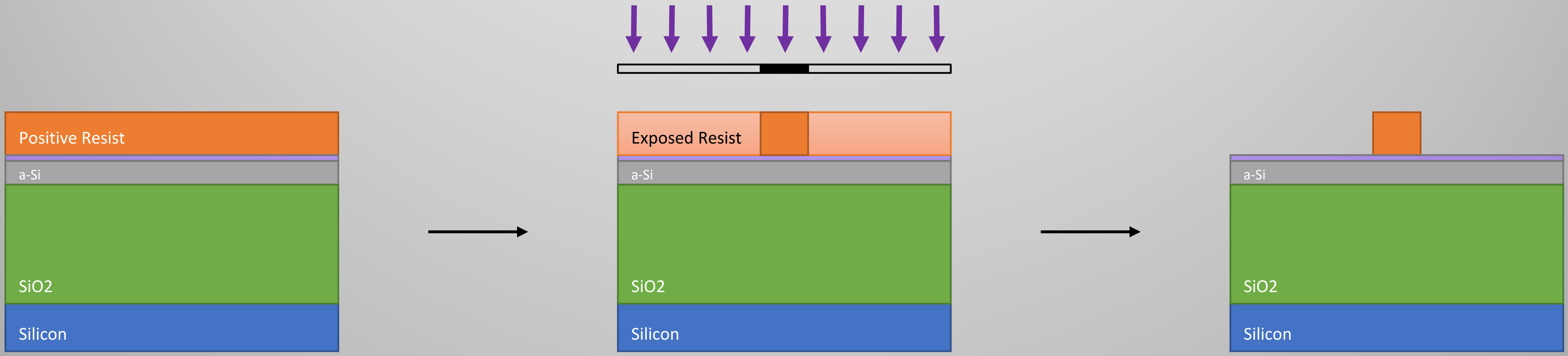
Wafer Pre-processing – Cleaning, BARC Application





Coat, Pattern, and Develop OiR-620 Positive Photoresist Image

Apply Positive Resist (300 nm) → Expose Resist → Develop Positive Resist

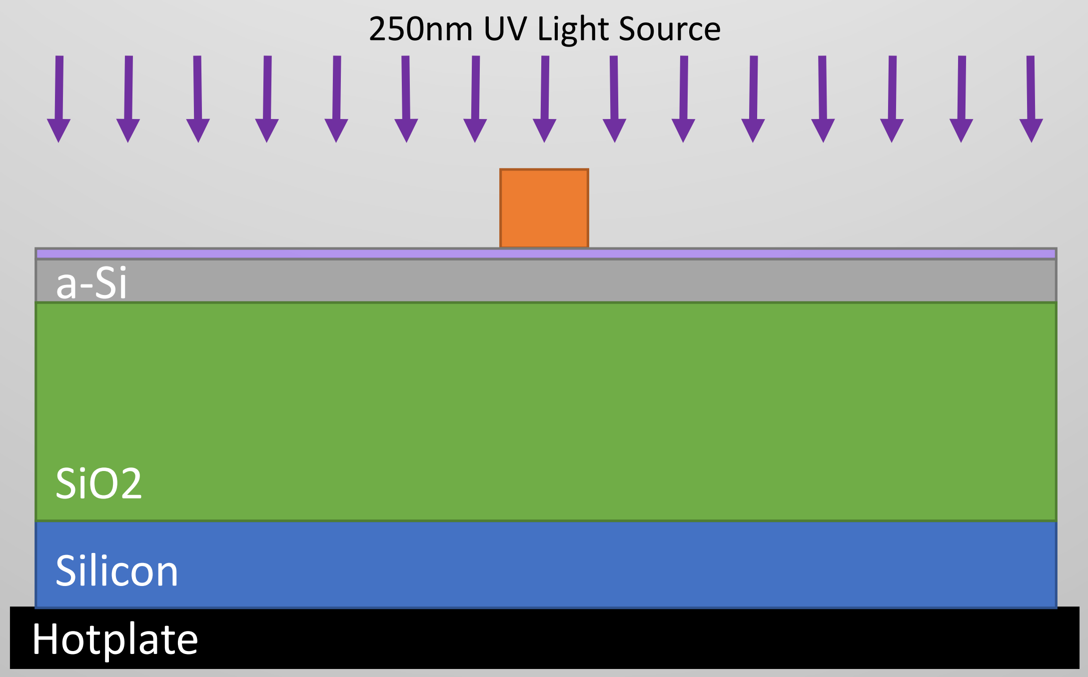


UV Cure of OiR-620 Positive Photoresist Image

UV Cure → Flood Expose

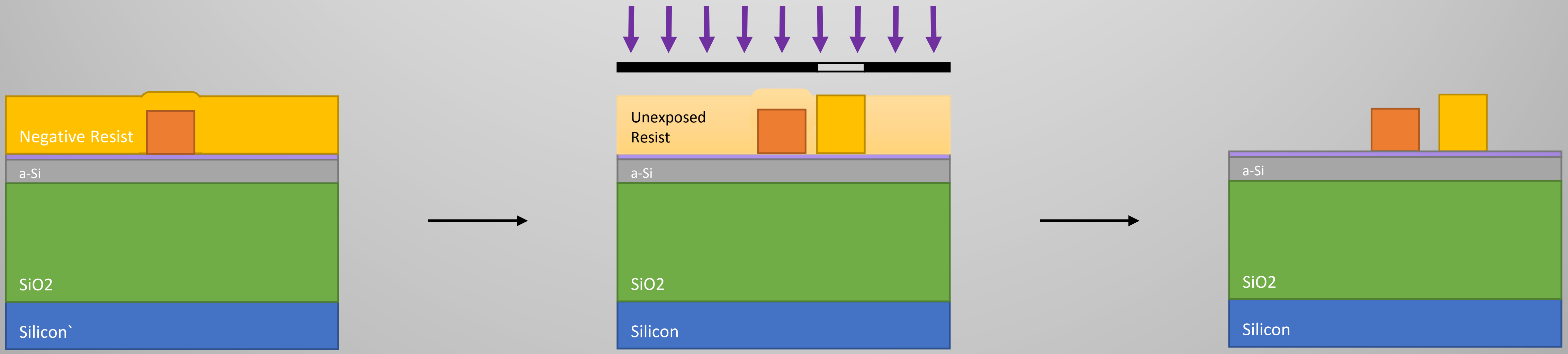
Flood Expose

- *250 nm Source*
- *140°C*
- *7 min*



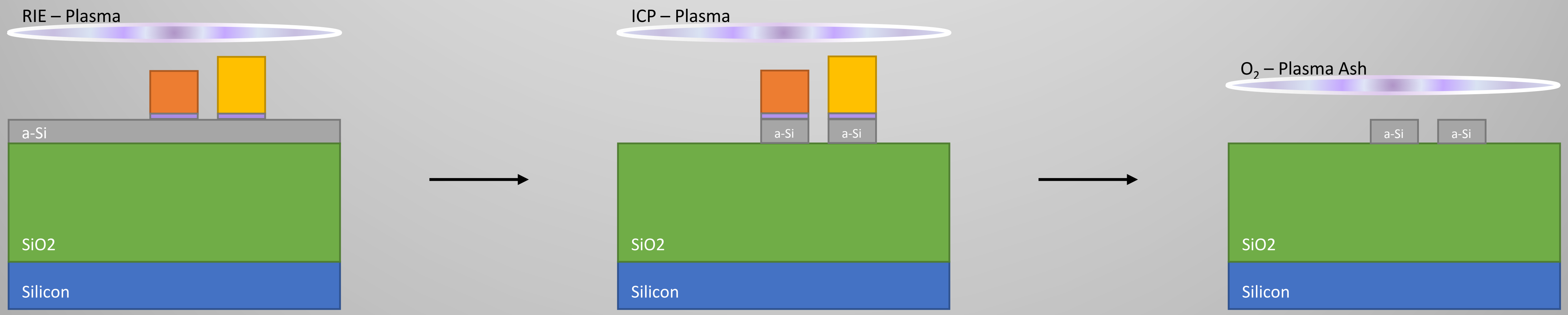
Coat, Pattern, and Develop NLOF-2020 Negative Photoresist Image

Apply Negative Resist (600 nm) → Expose Resist → Develop Negative Resist

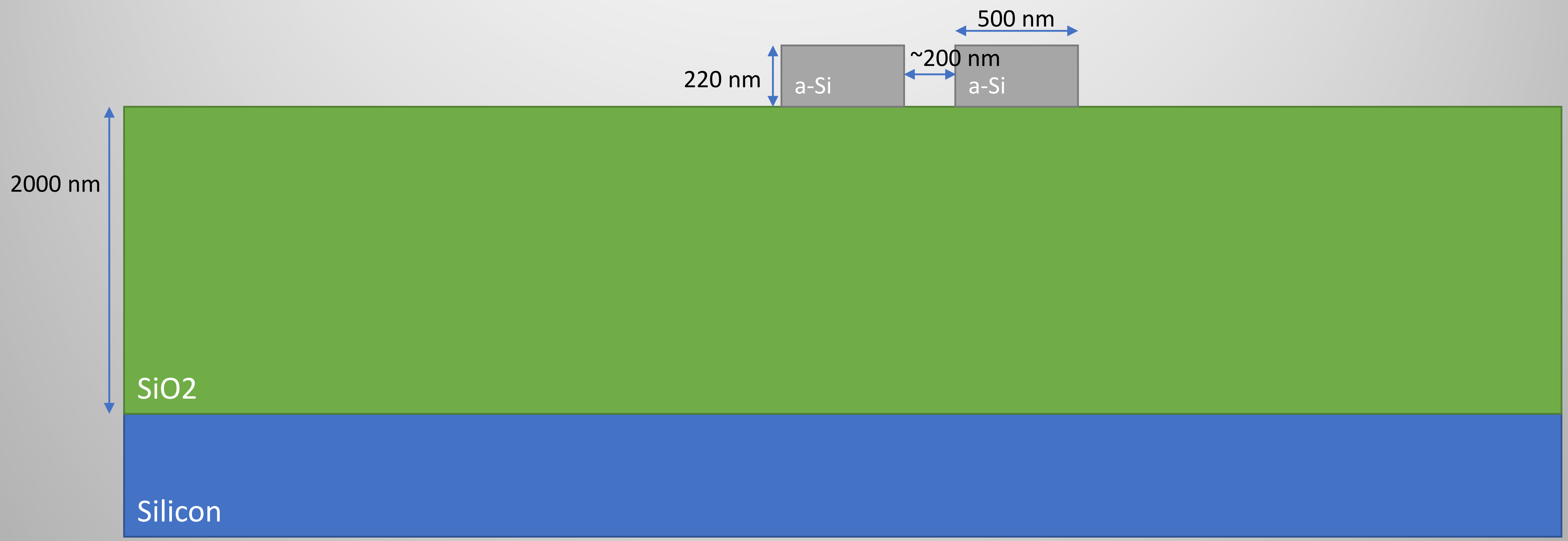


RIE Etch of BARC, ICP Etch of a-Si, Photoresist Strip

BARC Etch → a-Si Etch → Photoresist Strip



Final Device Profile – TE Mode Waveguide



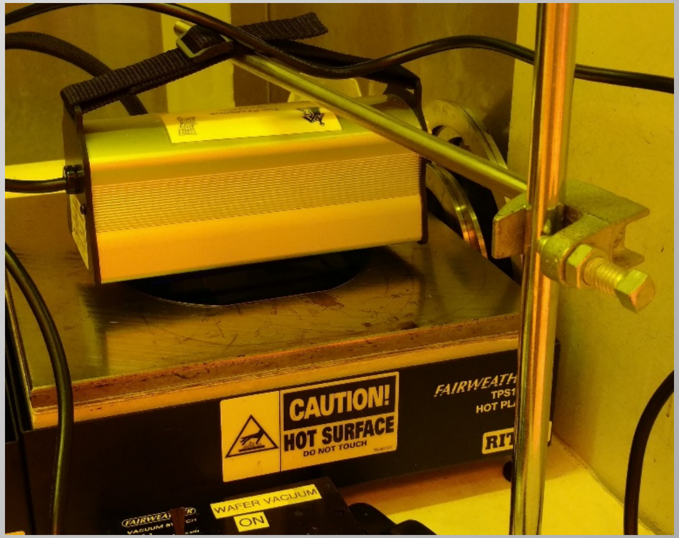
Process Development

UV Cure DOE – Impact of Exposure Time and Temperature on UV Cure Process

Experimental Setup

- Study the effects of exposure time, exposure temperature, room temperature, and humidity on the area of cured photoresist remaining after processing of the second layer of photoresist
- Apply and develop OiR-620 photoresist without exposure
- UV cure the first layer
- Apply and develop NLOF-2020 photoresist without exposure
- Measure area of remaining OiR-620 photoresist

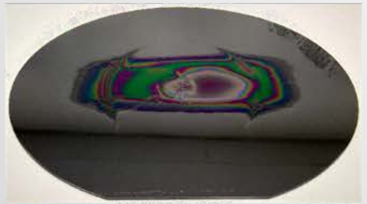
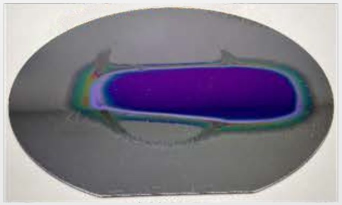
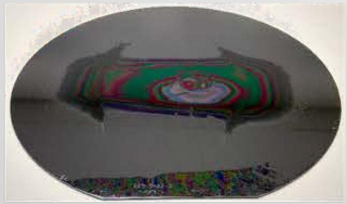
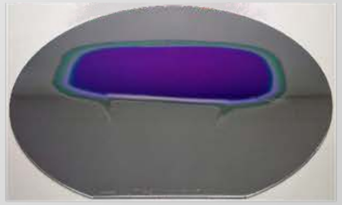
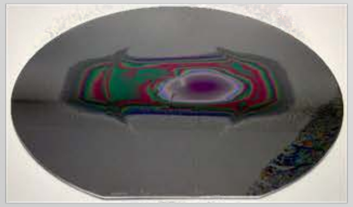
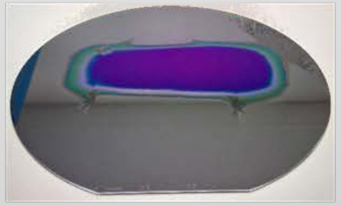
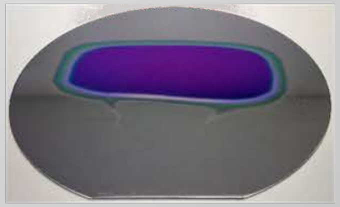
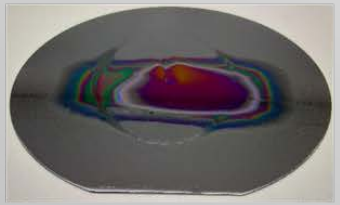
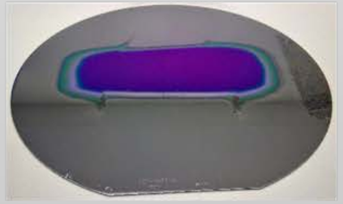
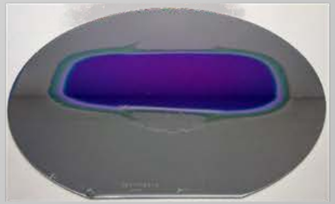
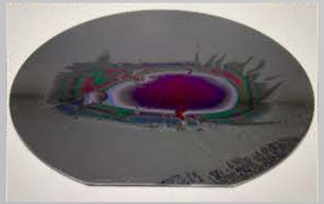
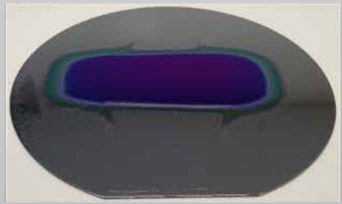
SVG 88 Track



UV Cure Setup

Design Matrix and Area of Cured Photoresist

Exposure Temperature

Exposure Time	130°C	Area (cm^2)	135°C	Area (cm^2)	140°C	Area (cm^2)
7 minutes		46.94		2876.6		3093.4
7.5 minutes		131.40		2519.4		3119.0
8 minutes		90.38		2506.6		3139.5
8.5 minutes		1148.10		2633.7		3598.6
9 minutes		993.80		3026.1		3198.1

Method of Analysis

- Least Squares Regression
- Examined three predictor variables:
  1. Exposure Temperature (Continuous)
  2. Exposure Time (Continuous)
  3. Humidity (Continuous)
- Using one response variable
  1. Area of cured photoresist in cm^2
- Regression Model:

$$Area = -1832 + 0.59*Time + 15.76*Temp - 901.64*Humidity$$

The REG Procedure
Model: MODEL1
Dependent Variable: area

Number of Observations Read	15
Number of Observations Used	15

Analysis of Variance					
Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Model	3	222578	74193	131.76	<.0001
Error	11	6194.17205	563.10655		
Corrected Total	14	228773			

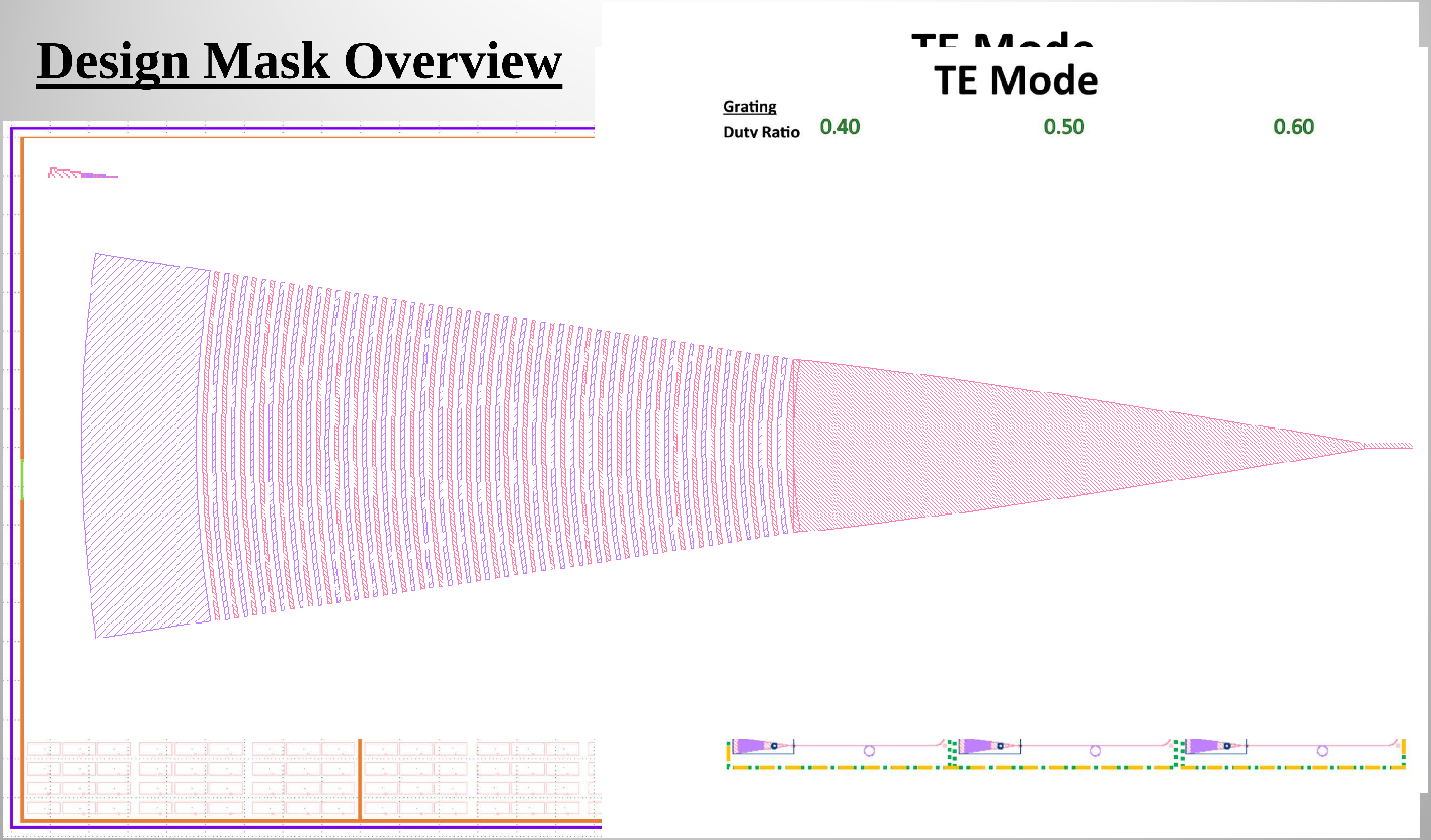
Root MSE	23.72987	R-Square	0.9729
Dependent Mean	214.14413	Adj R-Sq	0.9655
Coeff Var	11.08126		

Parameter Estimates							
Variable	DF	Parameter Estimate	Standard Error	t Value	Pr > |t|	95% Confidence Limits	
Intercept	1	-1832.13806	364.81531	-5.02	0.0004	-2635.09113	-1029.18499
time	1	0.58972	0.14442	4.08	0.0018	0.27187	0.90758
temp	1	15.75464	2.32719	6.77	<.0001	10.63253	20.87675
humidity	1	-901.64008	136.81456	-6.59	<.0001	-1202.76690	-600.51327

Process Development

Engineering Design Mask

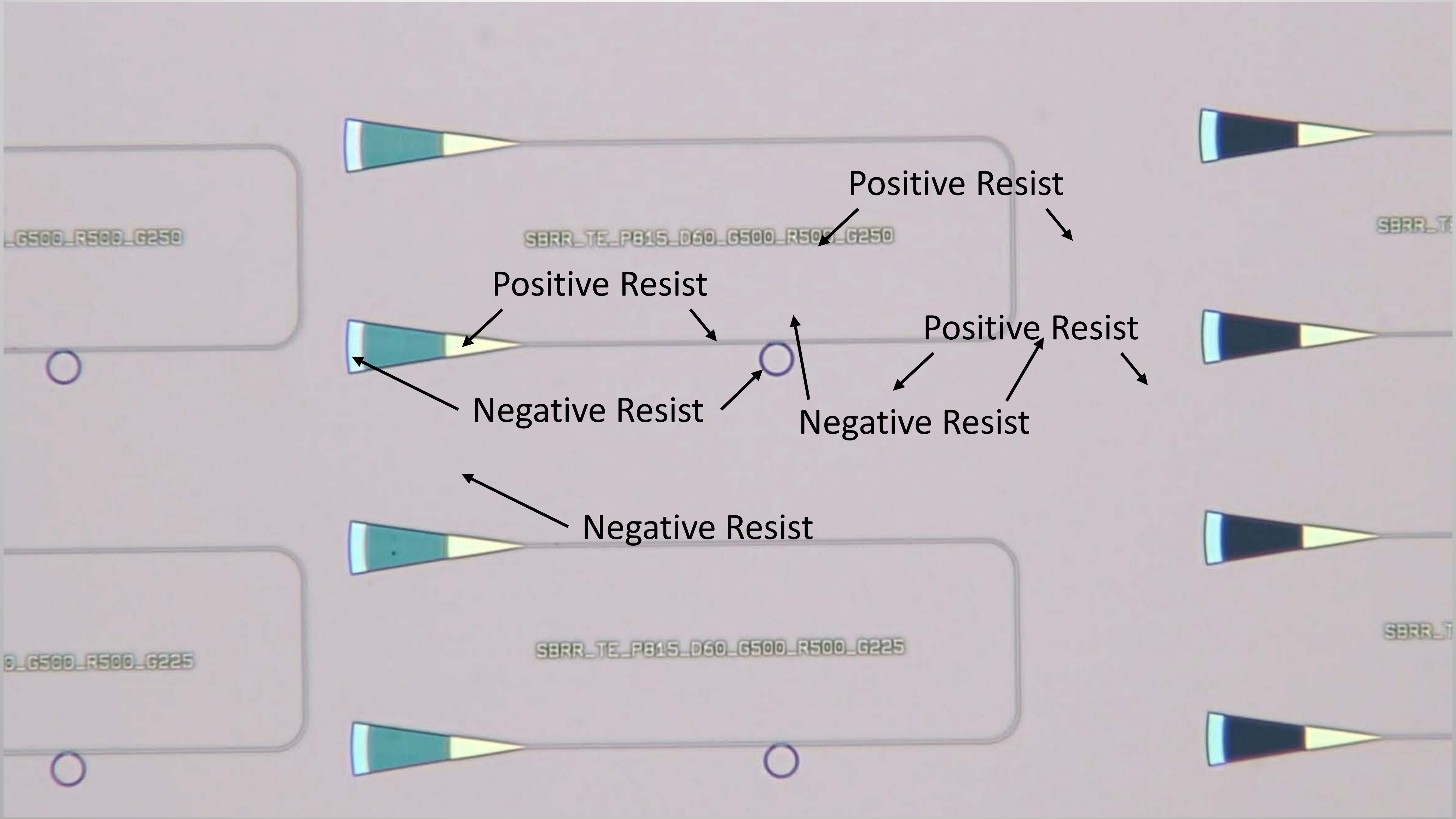
Design Mask Overview



Experimental Results

Initial Lithography Results

Compound Photoresist Image



Affect of Pitch and Duty Ratio on Photoresist Image

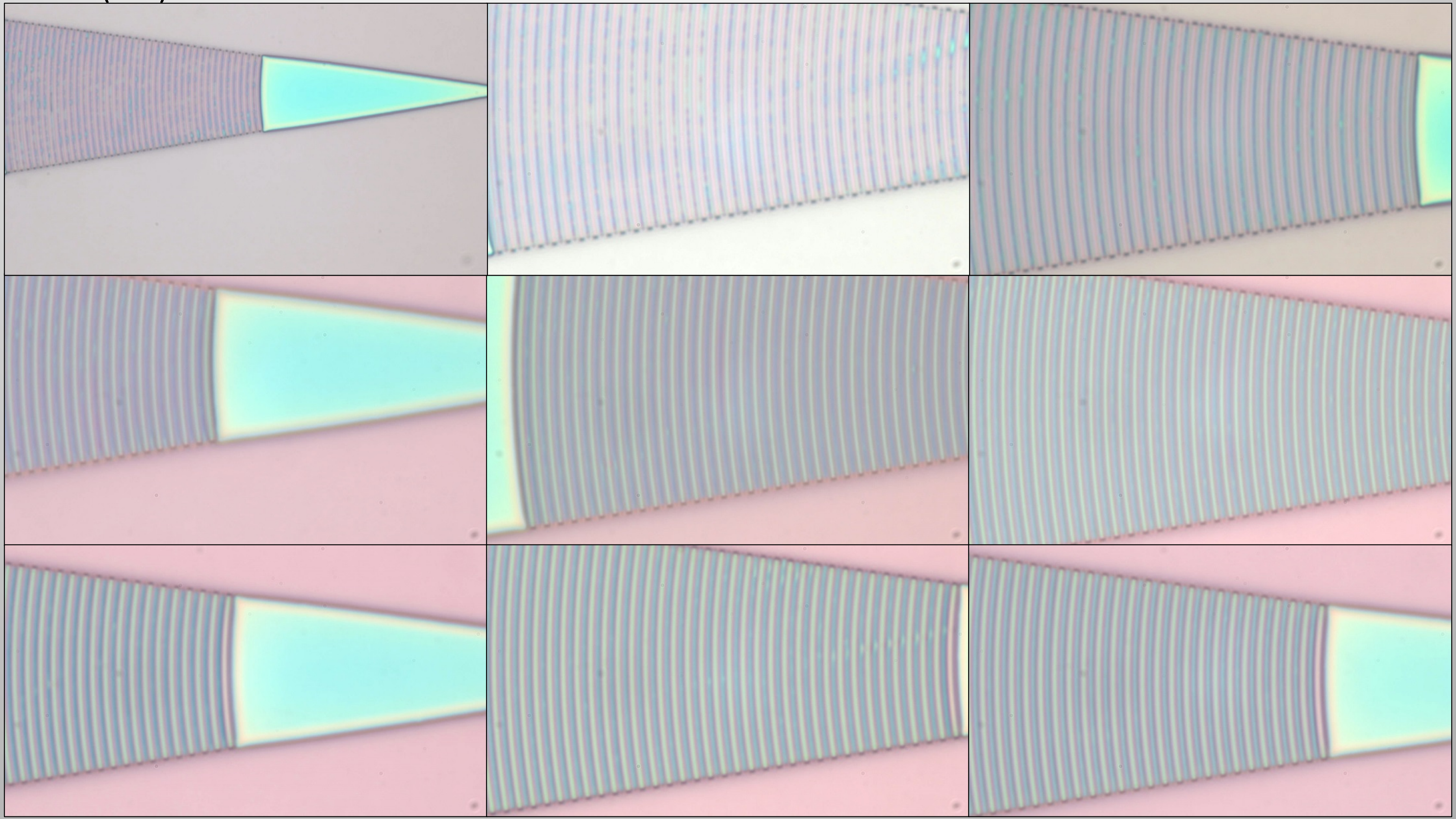
Pitch (nm) 640 675 710

Duty Ratio
(space:line)

0.40

0.50

0.60



Affect of Pitch and Duty Ratio on Photoresist Image

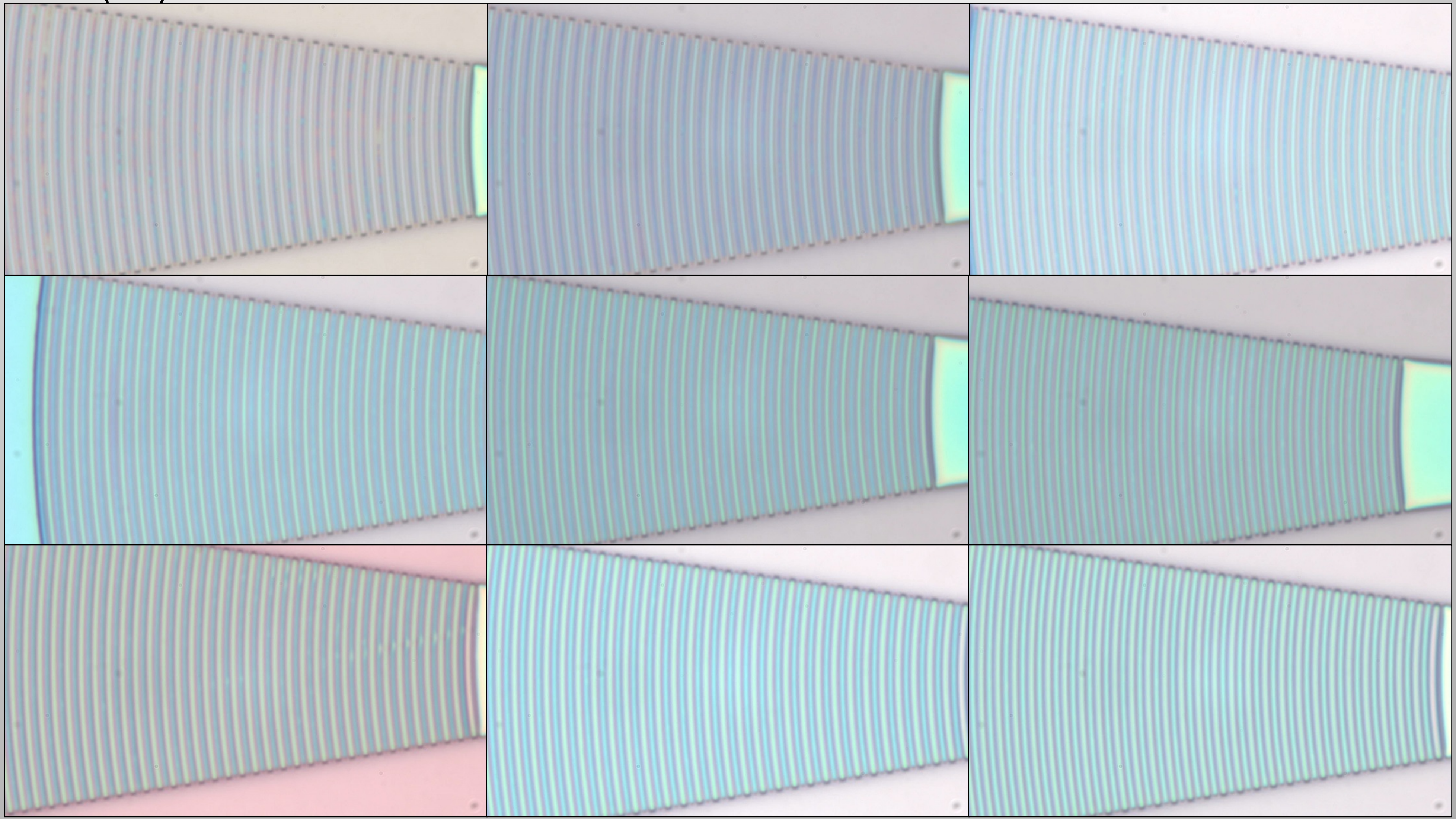
Pitch (nm) 745 780 815

Duty Ratio (space:line)

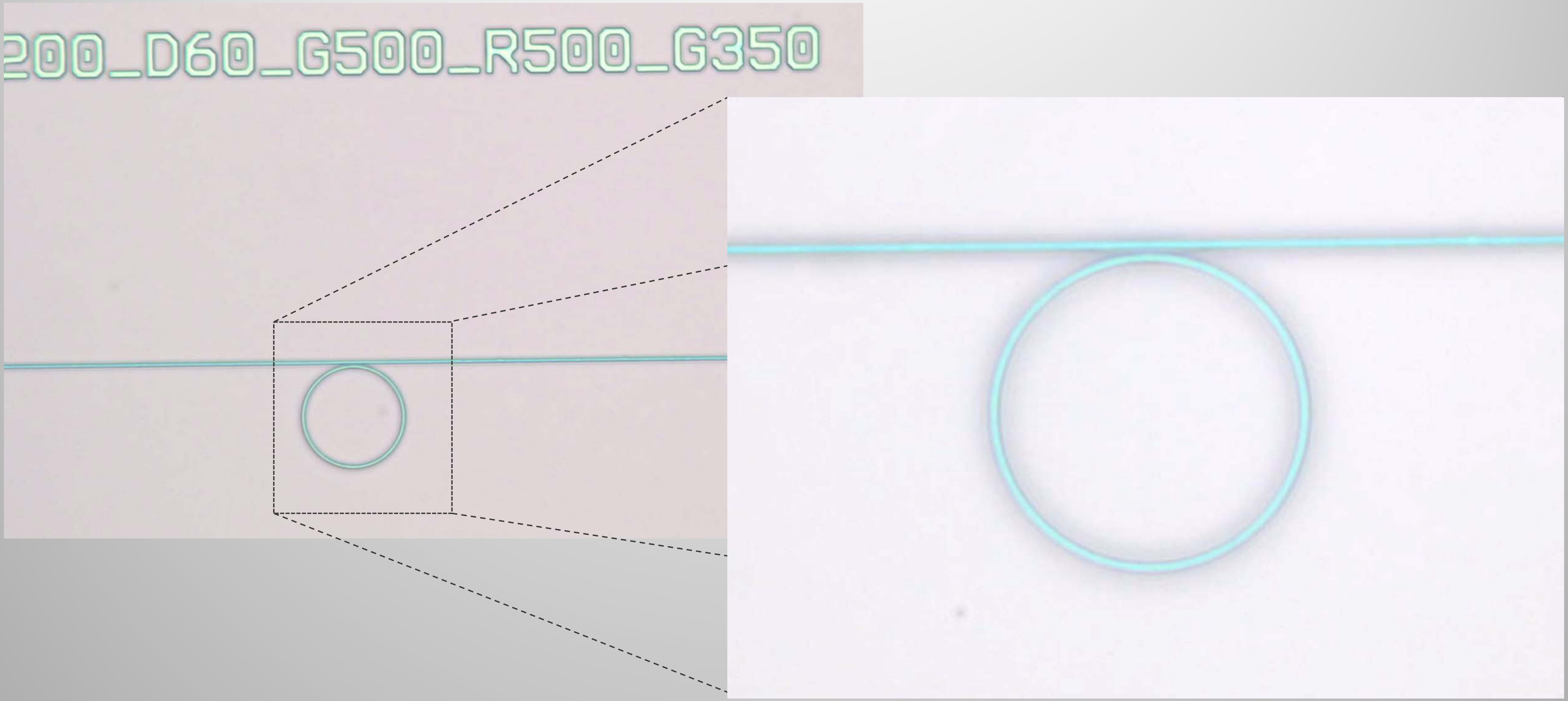
0.40

0.50

0.60



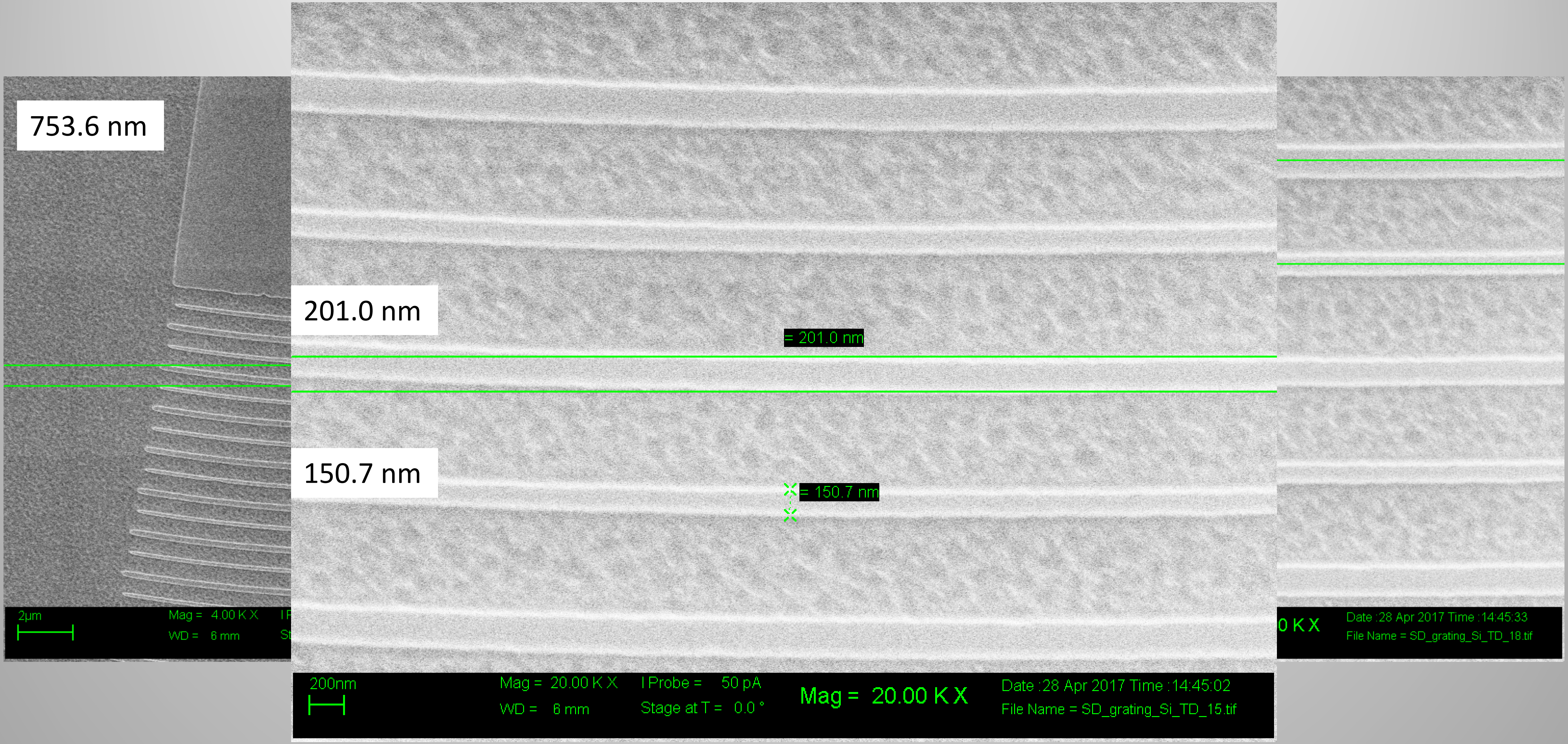
Ring Resonator



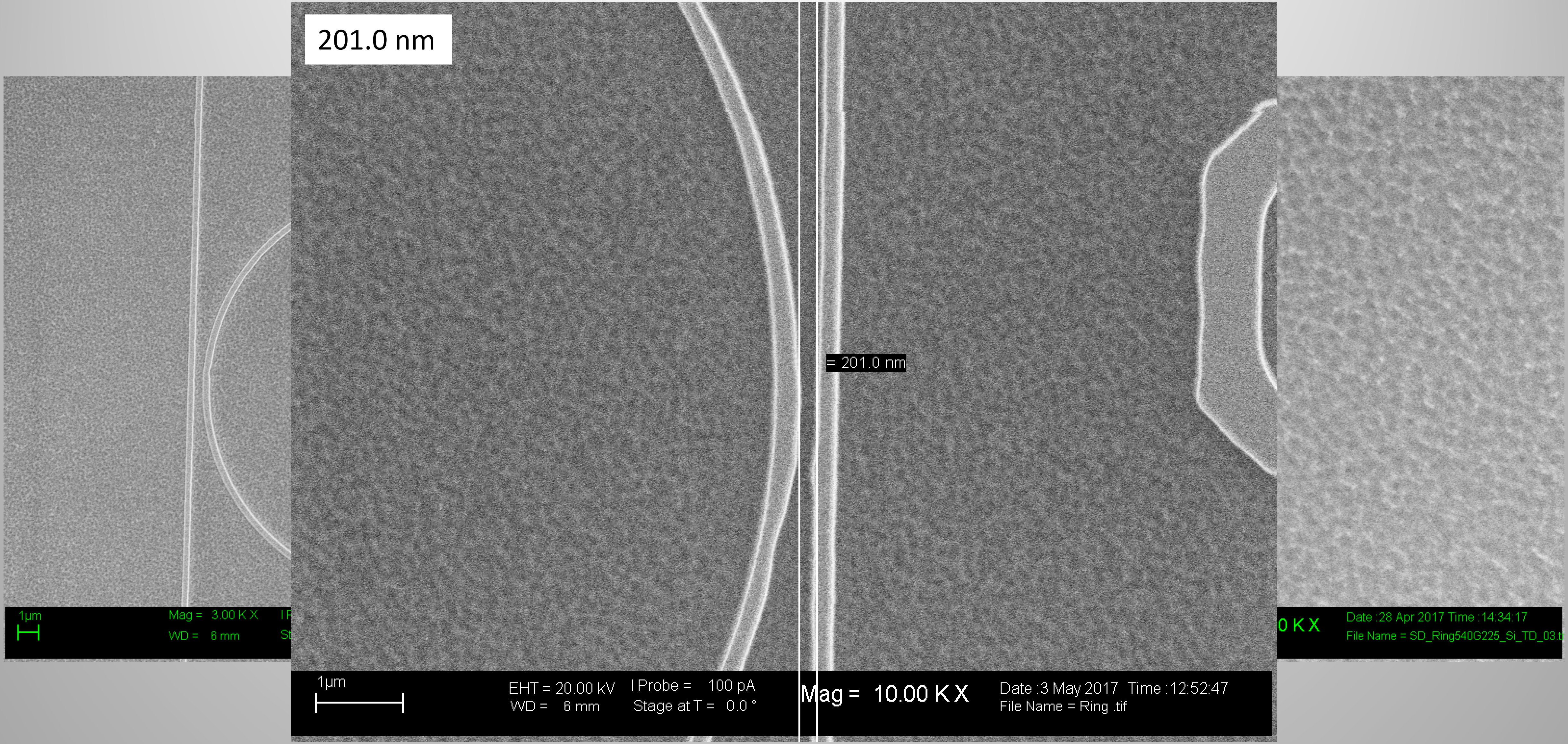
Experimental Results

Initial Etch Results

Grating Coupler – Post Etch SEM



Ring Resonator – Post Etch SEM



Conclusions

Conclusions Drawn from Final Results

Conclusions

- Obtained successful results from experimental process:
  - Minimum obtained feature size ~150 nm
  - Minimum obtained feature separation - ~100 nm
- Developed a working UV cure process using readily obtained positive and negative tone resists
- Developed a working LFLE process that can be refined to fabricate working TE mode photonic devices
- Created a two layer engineering design mask adequate for future work

Future Work

Outline of Possible Future Work

Outline of Possible Future Work

- Lithography optimization for SOI wafer
  - Account for changes in stack reflectivity
  - Separate optimization for positive and negative layers
- Optical Proximity Correction (OPC) mask design
  - Corrections for bulging in ring to wave guides gap
  - Corrections for fine pitch grating couplers
- Etch Recipe Optimization for compound resist image

References

Works Referenced

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- [1] S.Preble, “Waveguides: Silicon Waveguides”, MCEE-789/EEEE-789, Powerpoint, Spring 2165
- [2] M. Maenhoudt, “Alternative process schemes for double patterning that eliminate the intermediate etch step”, Proc. of SPIE Vol. 6924, 2008.
- [3] M. Hori, et al., “Sub-40nm Half-Pitch Double Patterning with Resist Freezing Process”, Proc. of SPIE Vol. 6923, 2008.
- [4] C. Shay, “CD Reduction through Annular Illumination and Sidewall Spacer Etch”, Senior Design, Rochester Institute of Technology, 2016.
- [5] P. Cadareanu, "Silicon Photonic Devices Manufactured Using Double-Patterned iLine Lithography“, Rochester Institute of Technology, 2016.