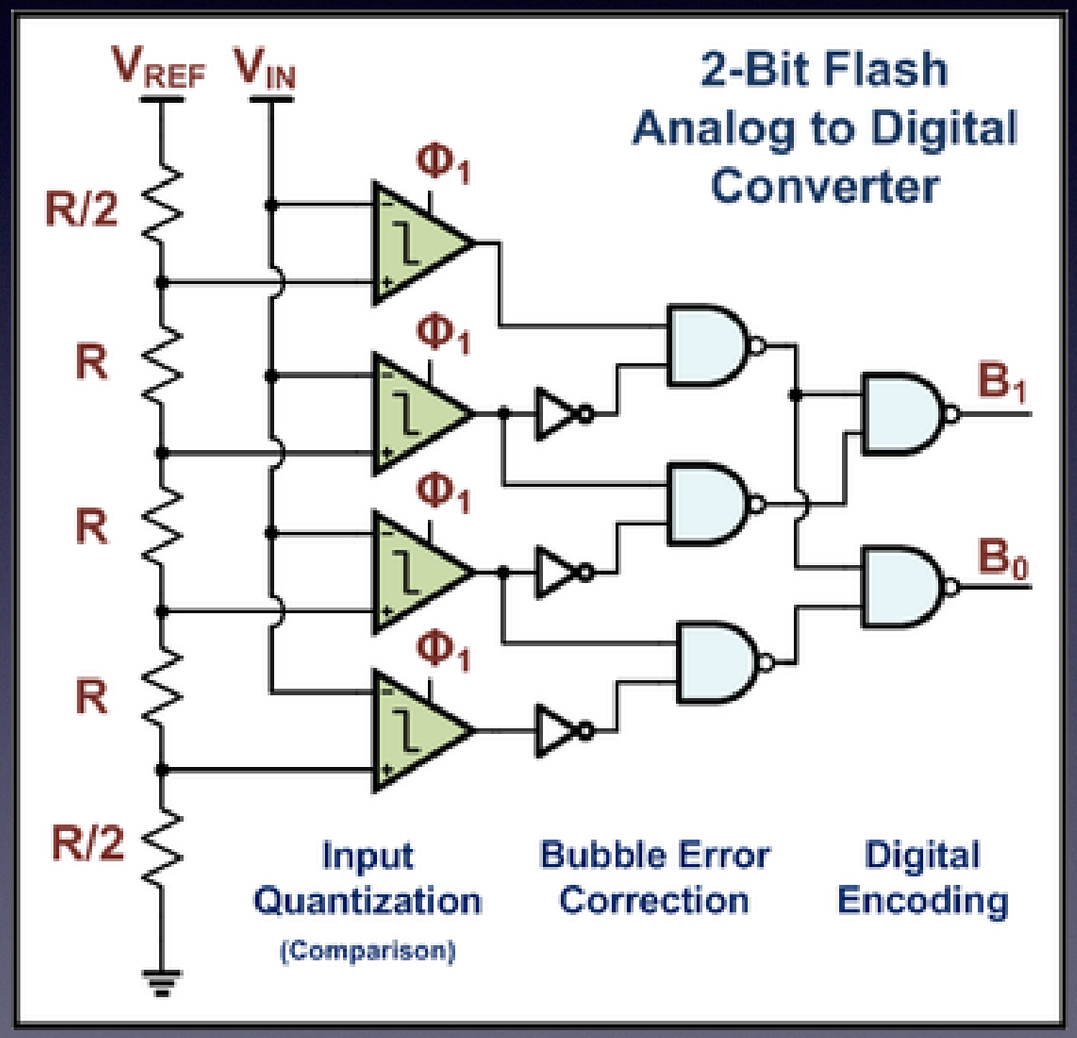
Stochastic ADC using Digital Standard Cells

Zach Baltzer

- State of the Industry
- Stochastic ADC Basis of Operation
- Layout Design
- Simulation

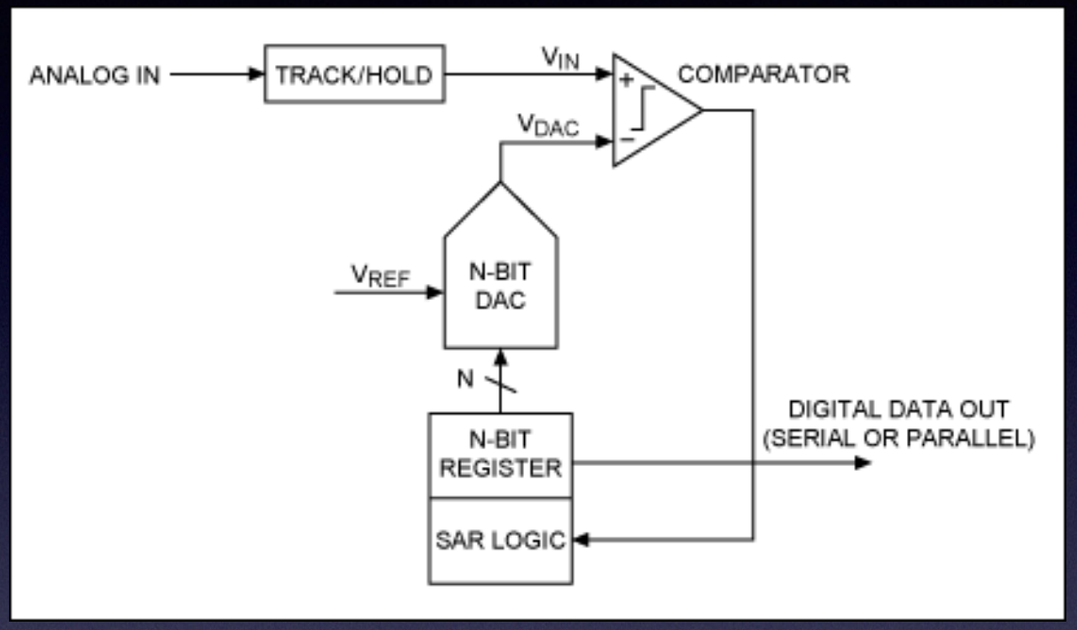
Traditional ADC - Flash

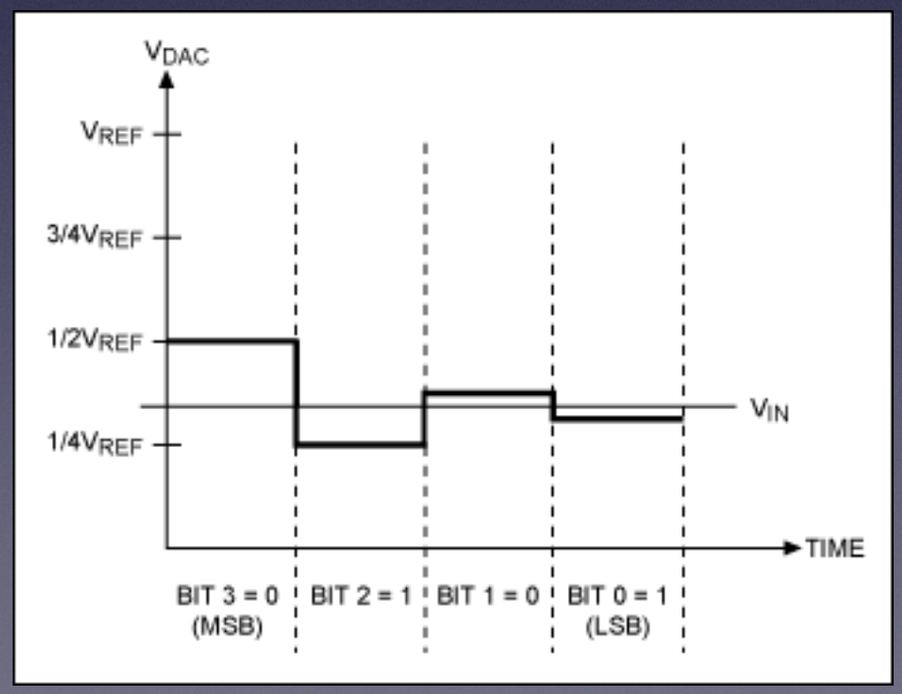
- Advantages:
  - Fast
  - Simple Design
- Disadvantages:
  - Error Correction
  - Resistor / Comparator Accuracy



Traditional ADC - SAR

- Advantages:
  - Simple Design
  - As Accurate as DAC Circuitry
- Disadvantages:
  - Large Capacitor Network
  - Slow





Statistical Variation

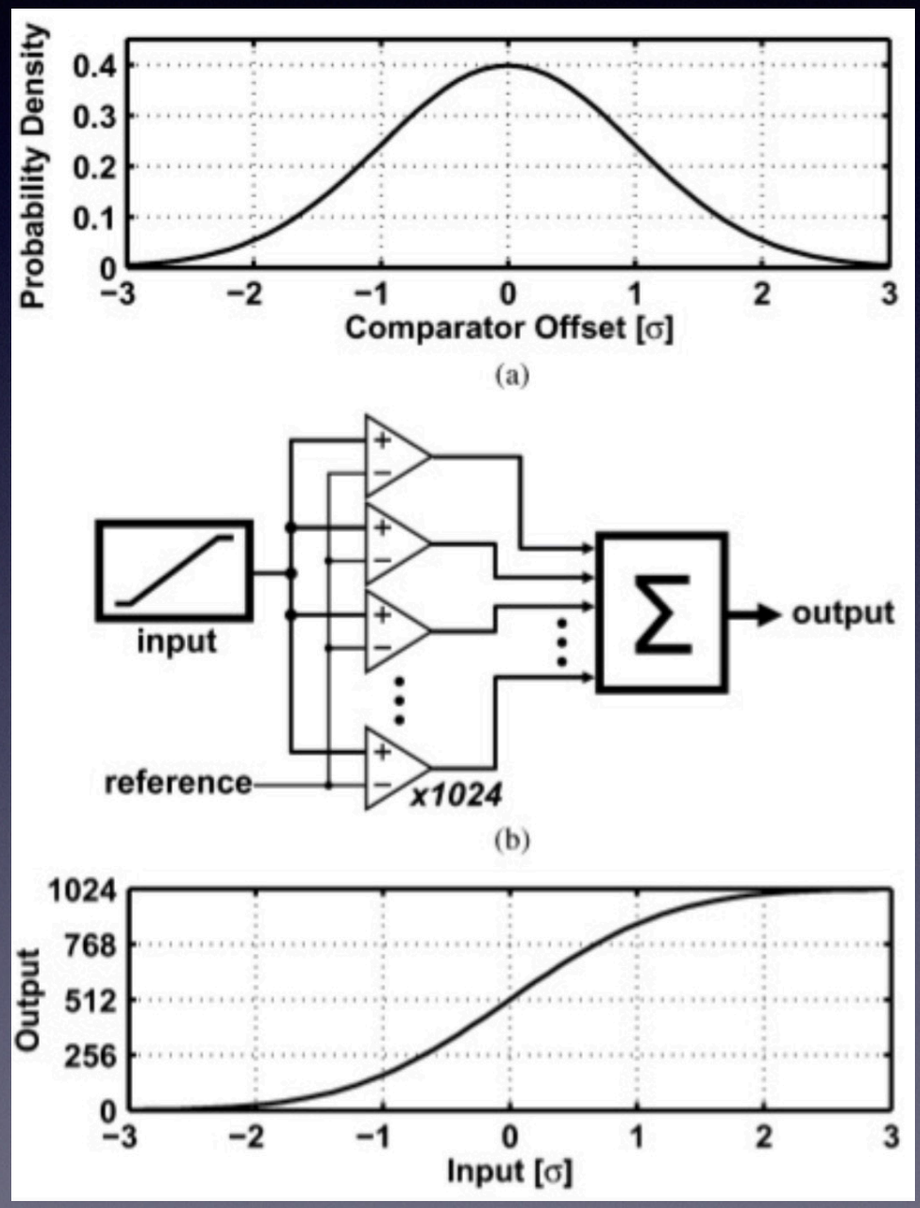
- No 2 transistors are equivalent.
- Latest SPICE models *include* this variation in the model itself. (Level 54)

TABLE I
LAYOUT AND SYSTEMATIC SOURCES OF VARIATION COVERED BY SPECIAL TEST STRUCTURES (PARTIAL LIST)

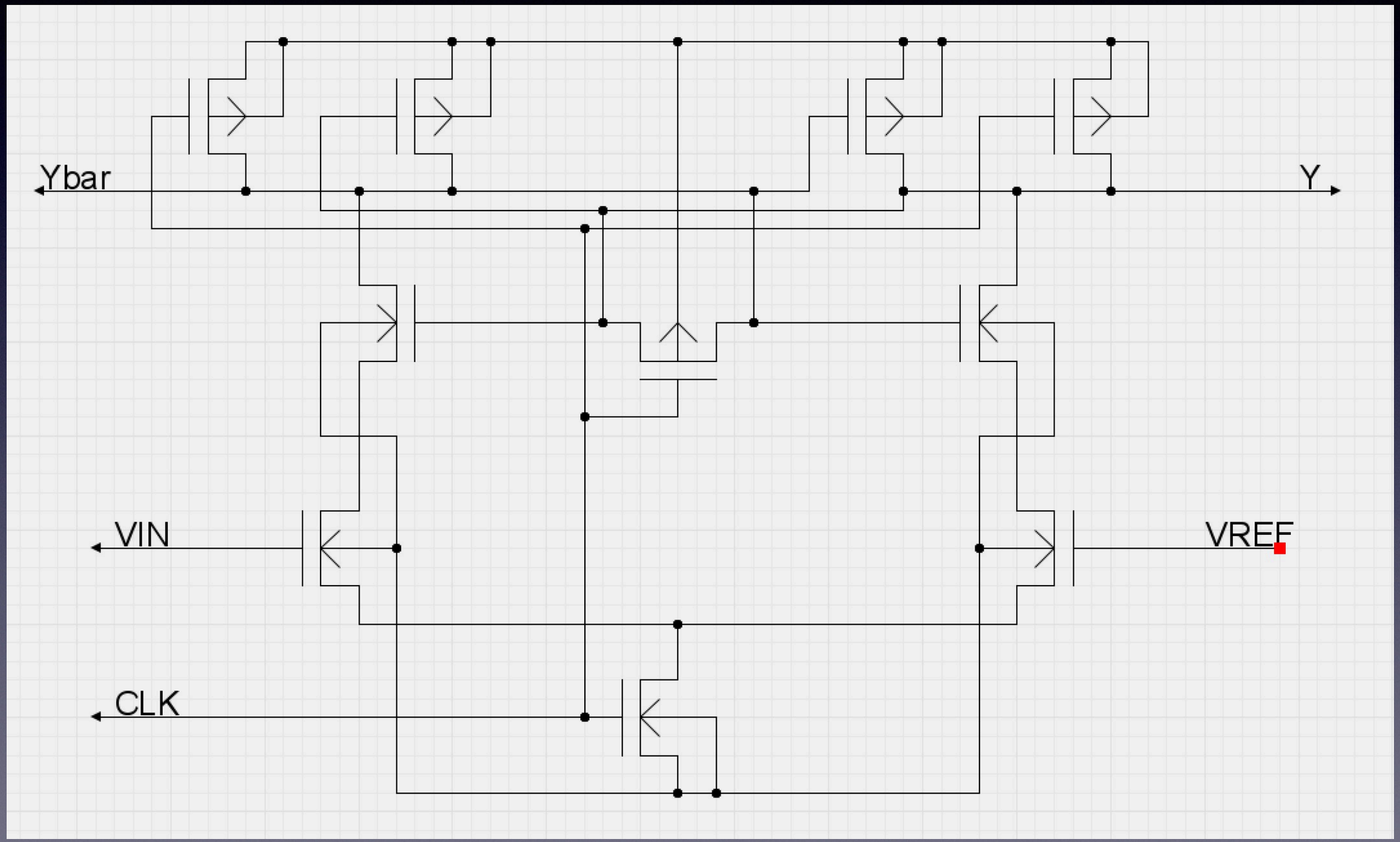
Systematic variation	Root causes
Gate poly orientation	Poly lithography, stress layers
Gate poly pitches	Poly OPC, lithography & stress
Poly corner rounding	Poly OPC and lithography
Transistor location in multi-gate transistor	Poly patterning impacted by local neighborhood differences
Active corner rounding	Active OPC and lithography
Un-modeled narrow width effects	Stress effects, poly step height
Gate to active edge	STI stress, e-SiGe stress
Well proximity	Implant scattering
Nwell-Pwell separation	Gate counterdoping and misalignment
Contact density and placement	Silicide sheet resistance and stress

Stochastic ADC

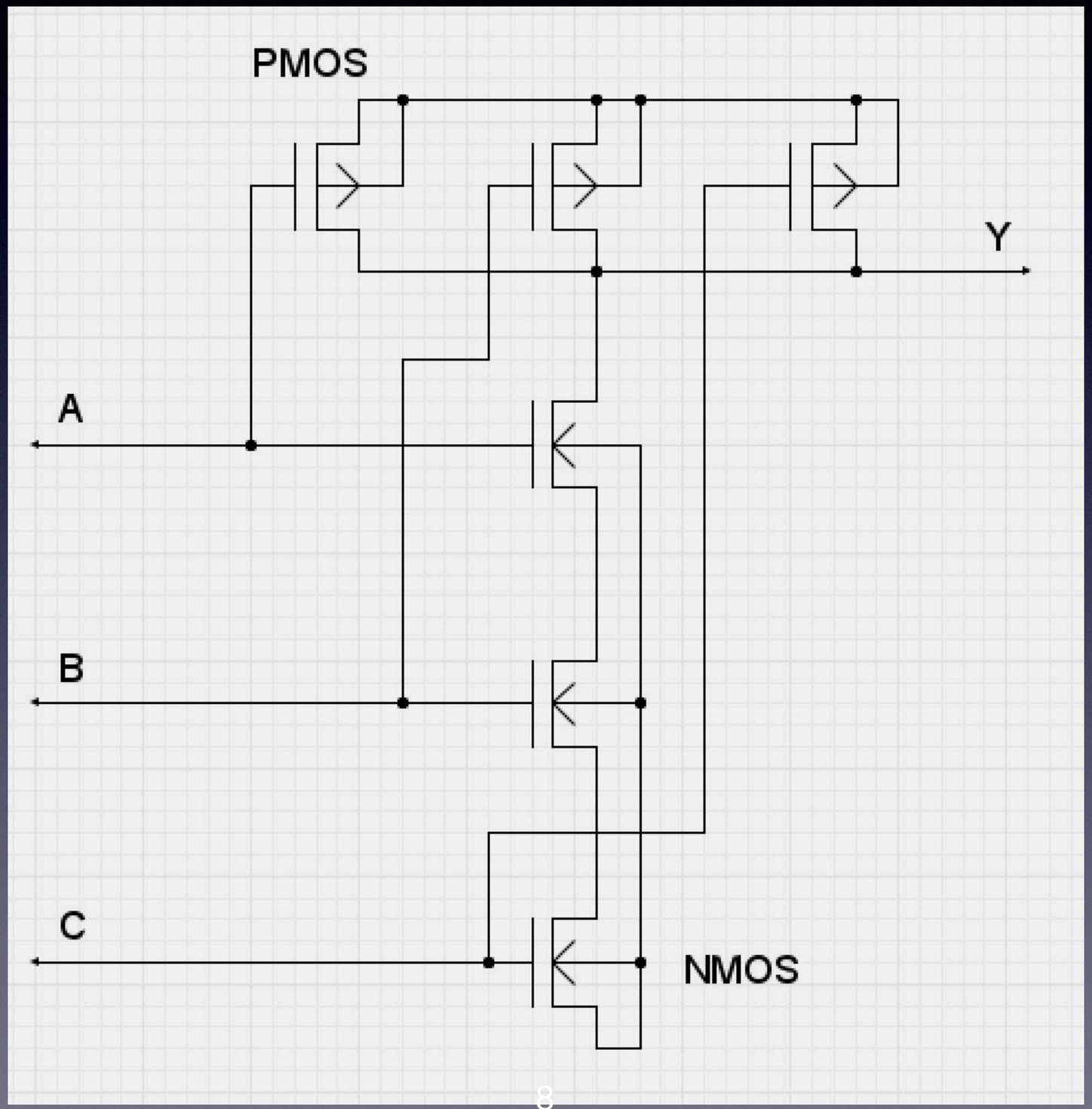
- Advantages:
  - Fast
  - Digital
  - Synthesizable Design
- Disadvantages:
  - Die Area
  - Process Dependent



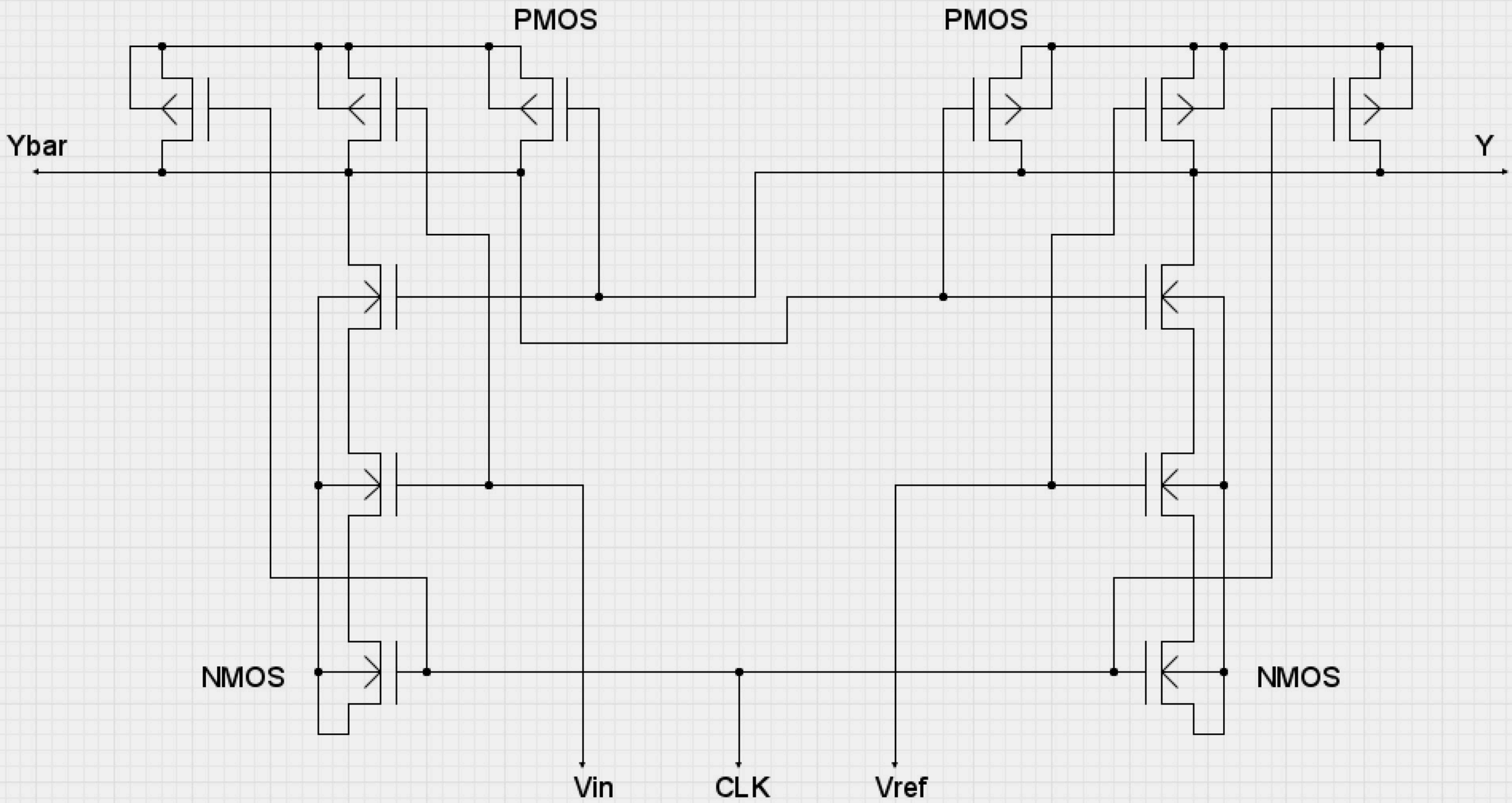
Basis of Operation



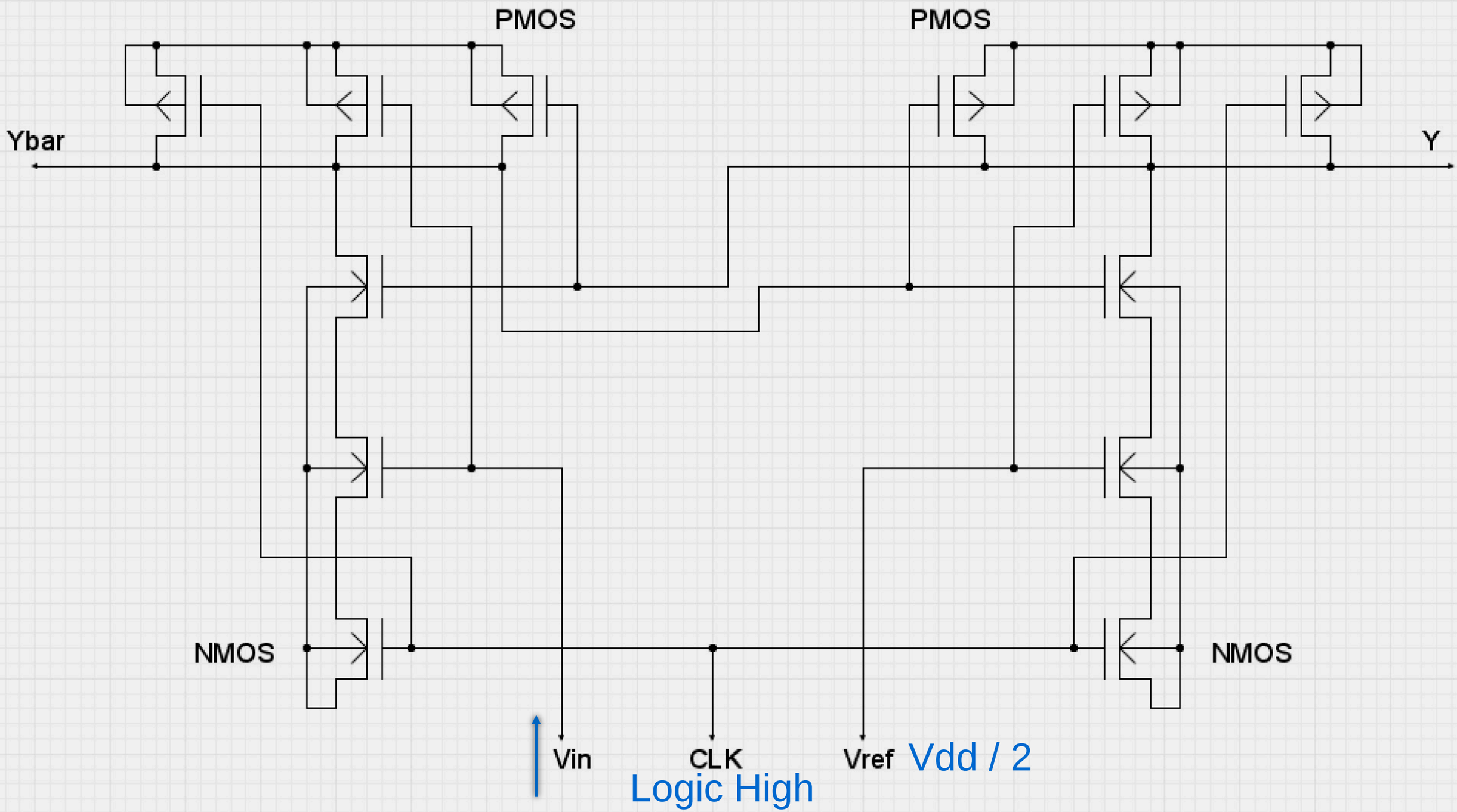
Stochastic ADC Operation



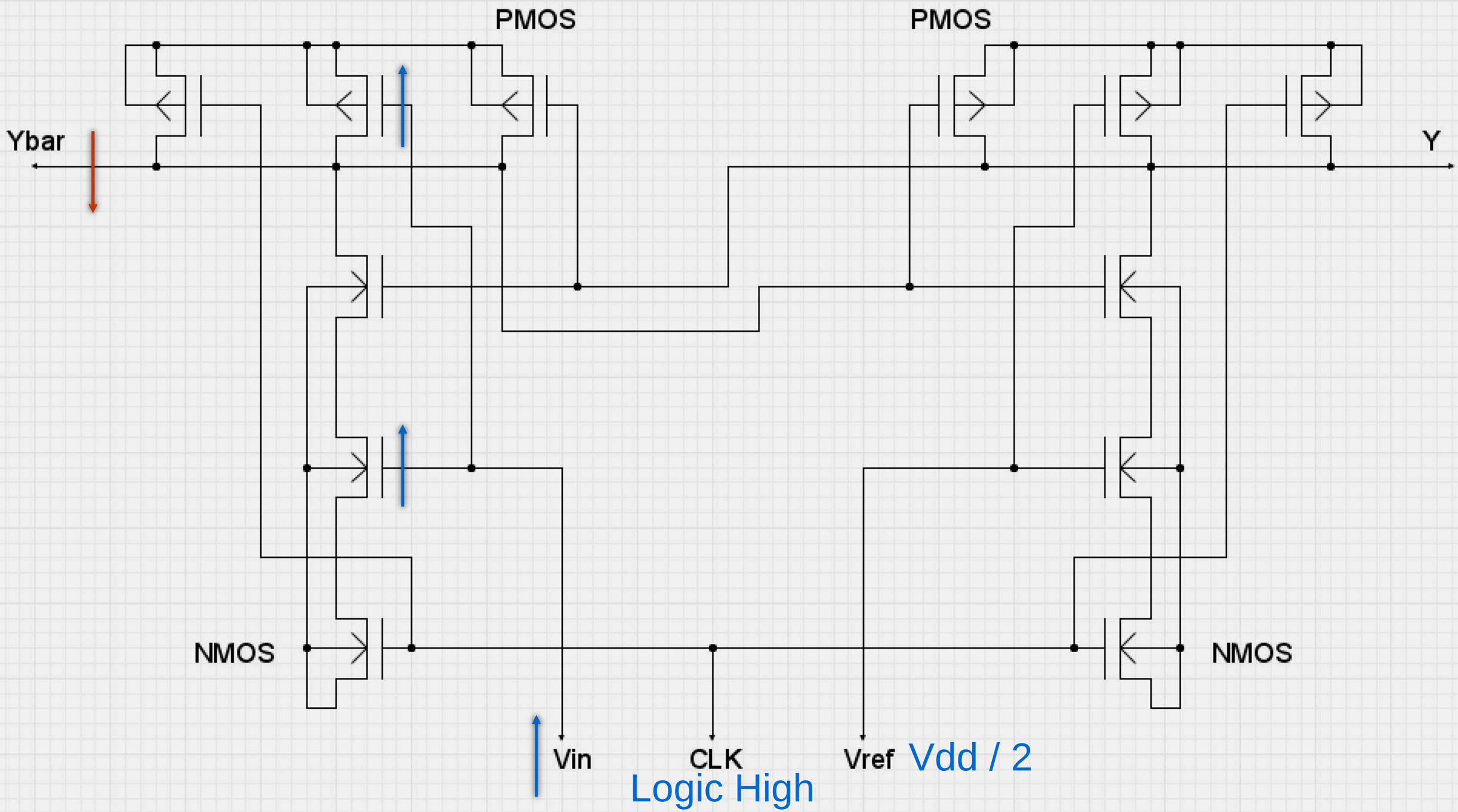
Stochastic ADC Operation



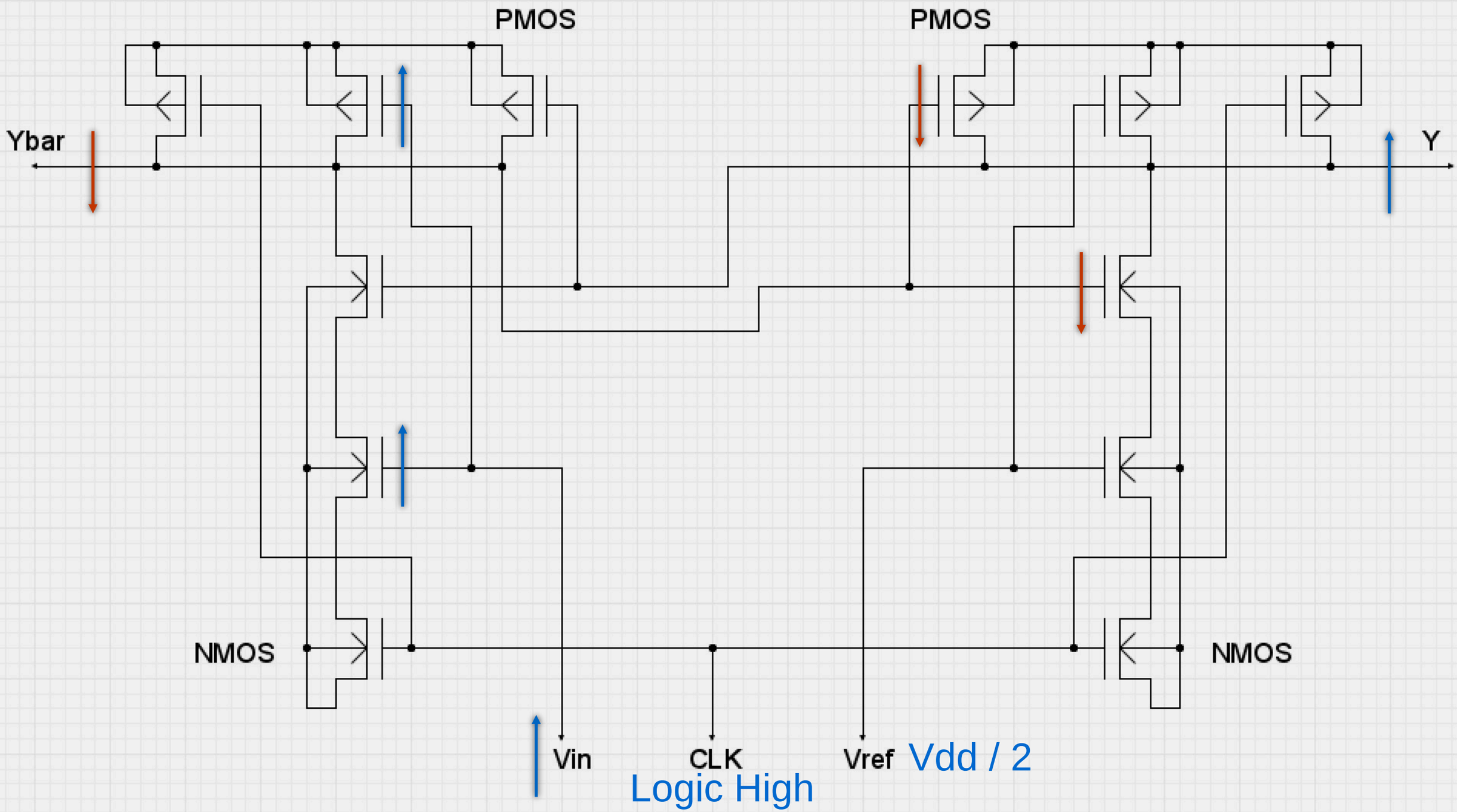
Stochastic ADC Operation



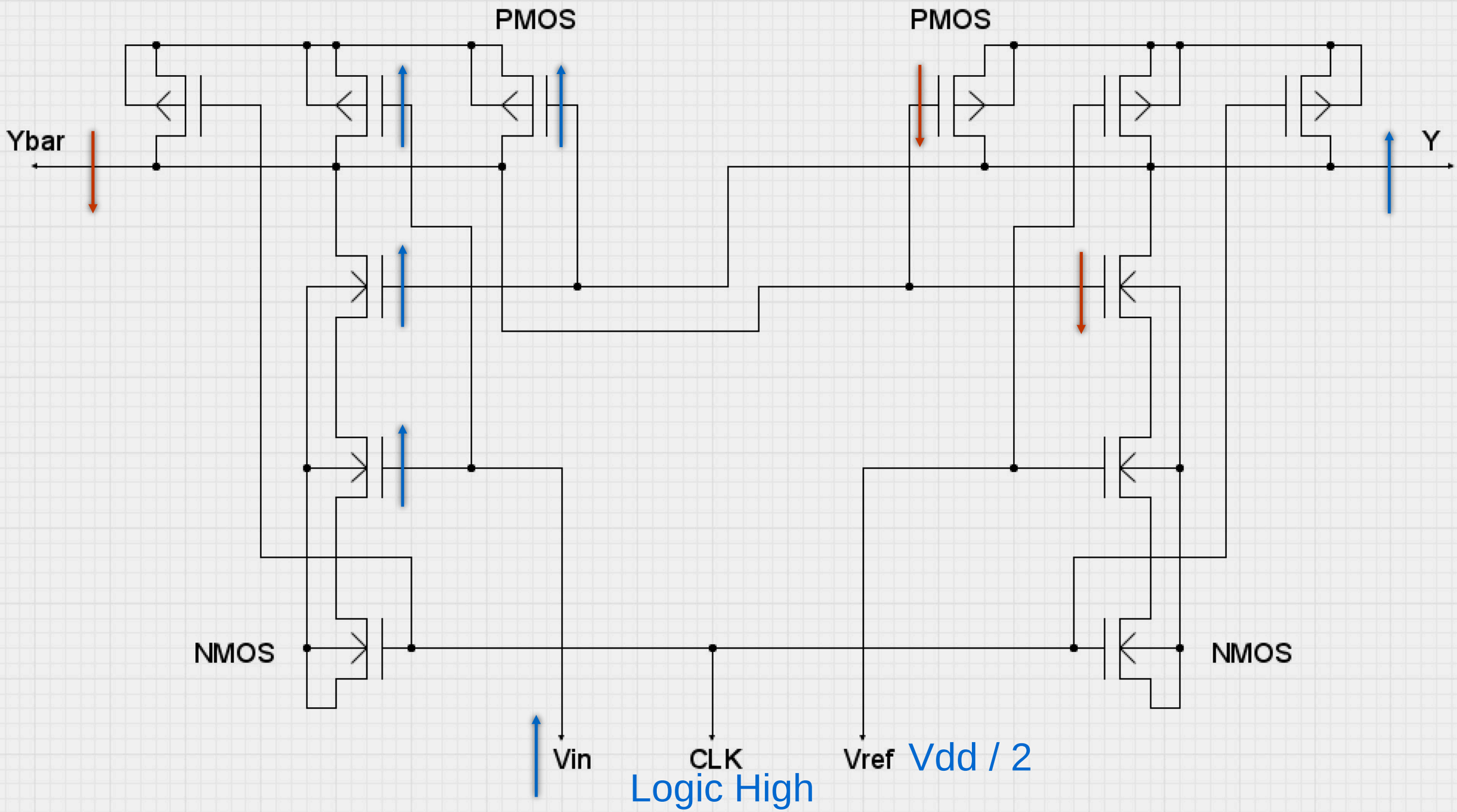
Stochastic ADC Operation



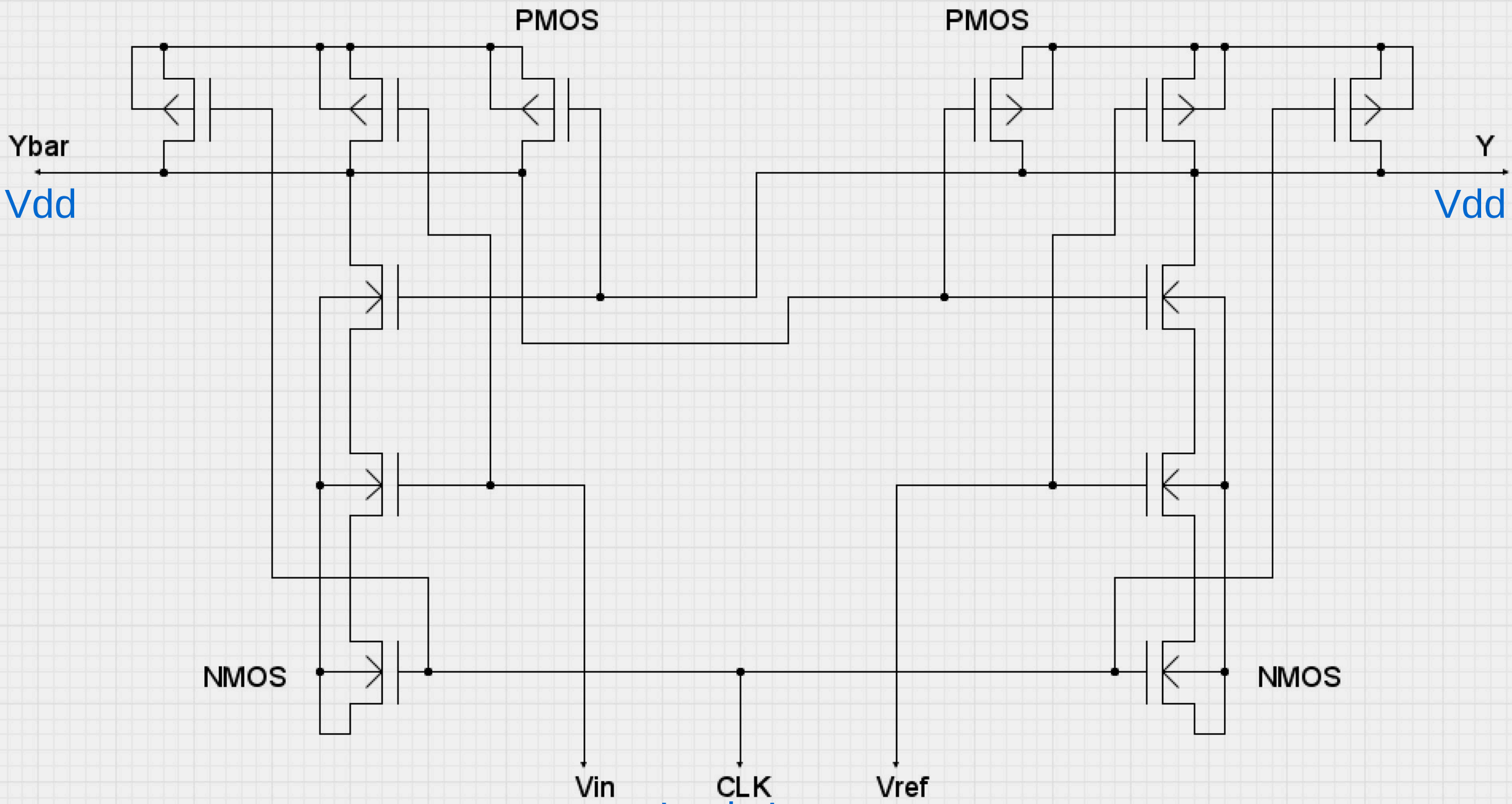
Stochastic ADC Operation



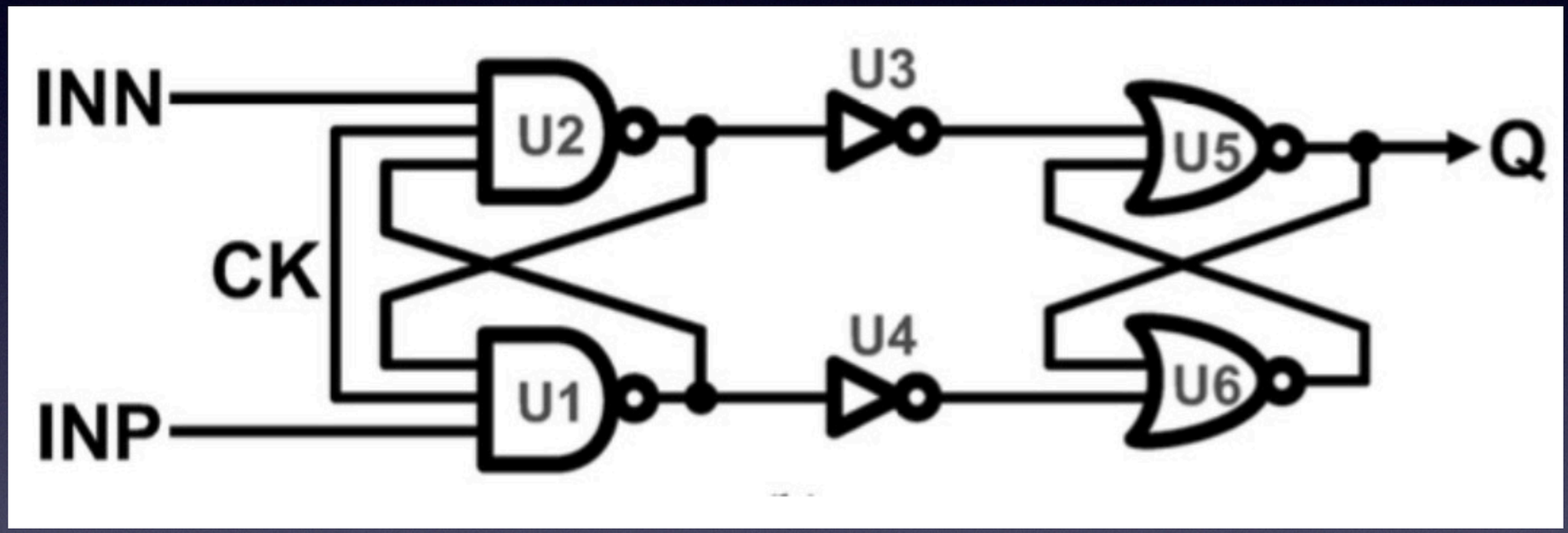
Stochastic ADC Operation



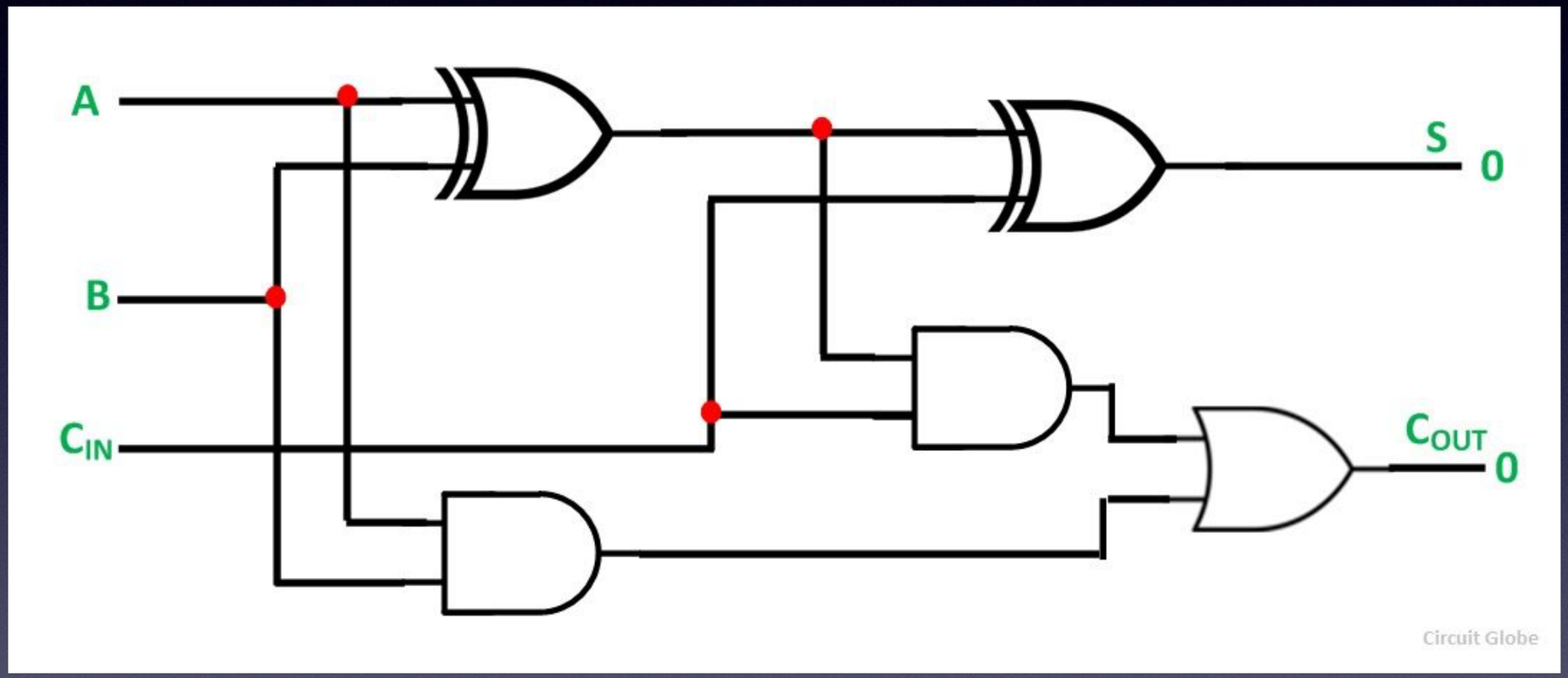
Stochastic ADC Operation



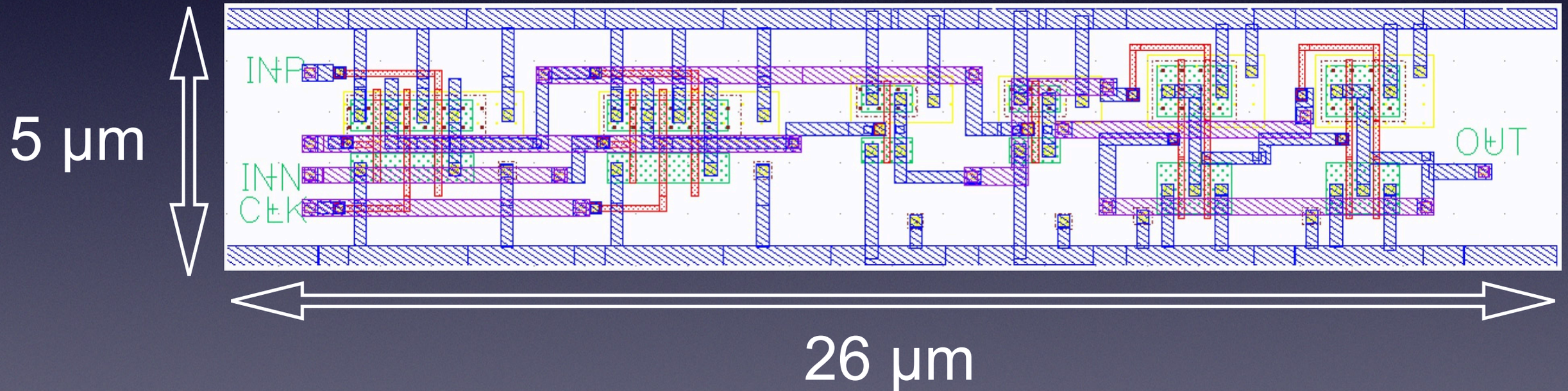
Clocked Comparator Schematic



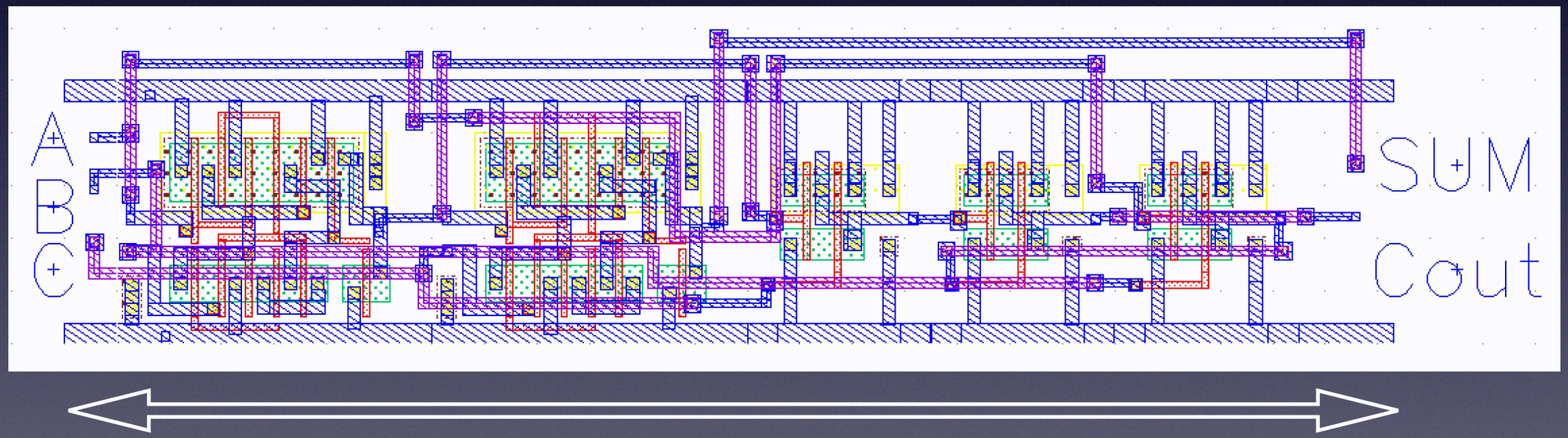
Full Adder Schematic



Clocked Comparator Design



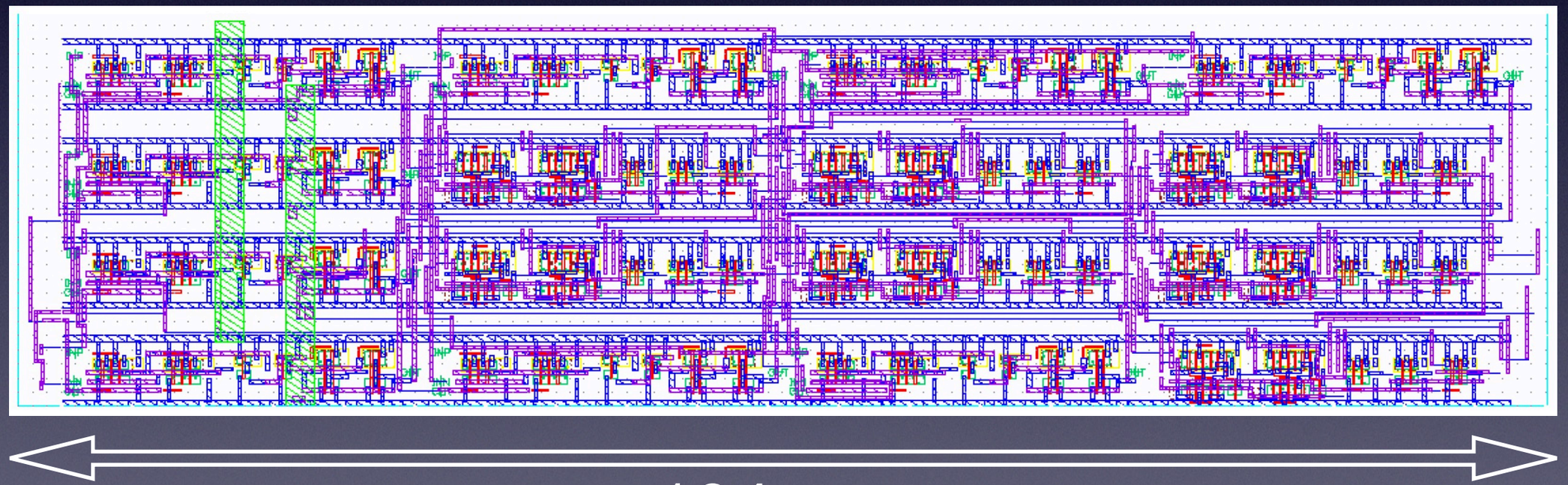
Full Adder Design



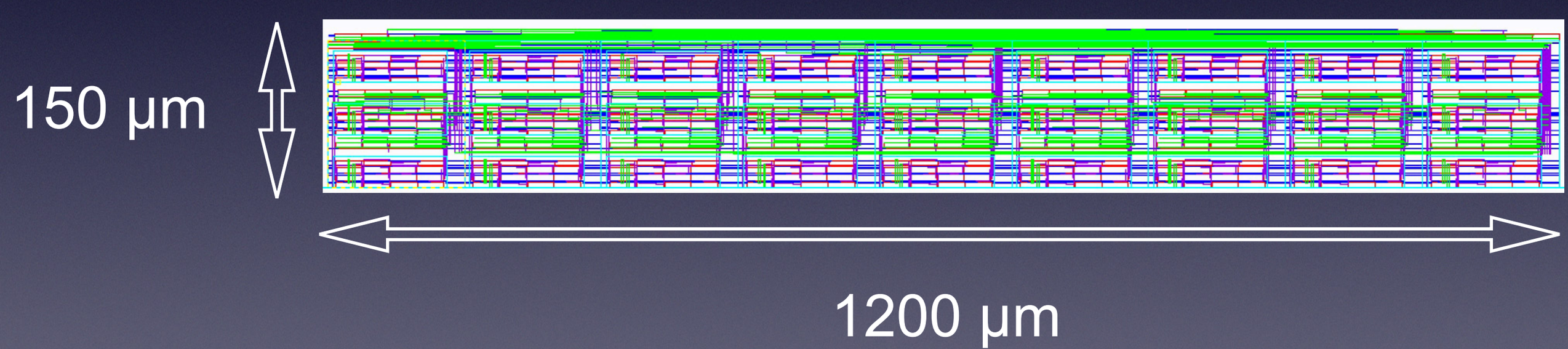
6 µm

26 µm

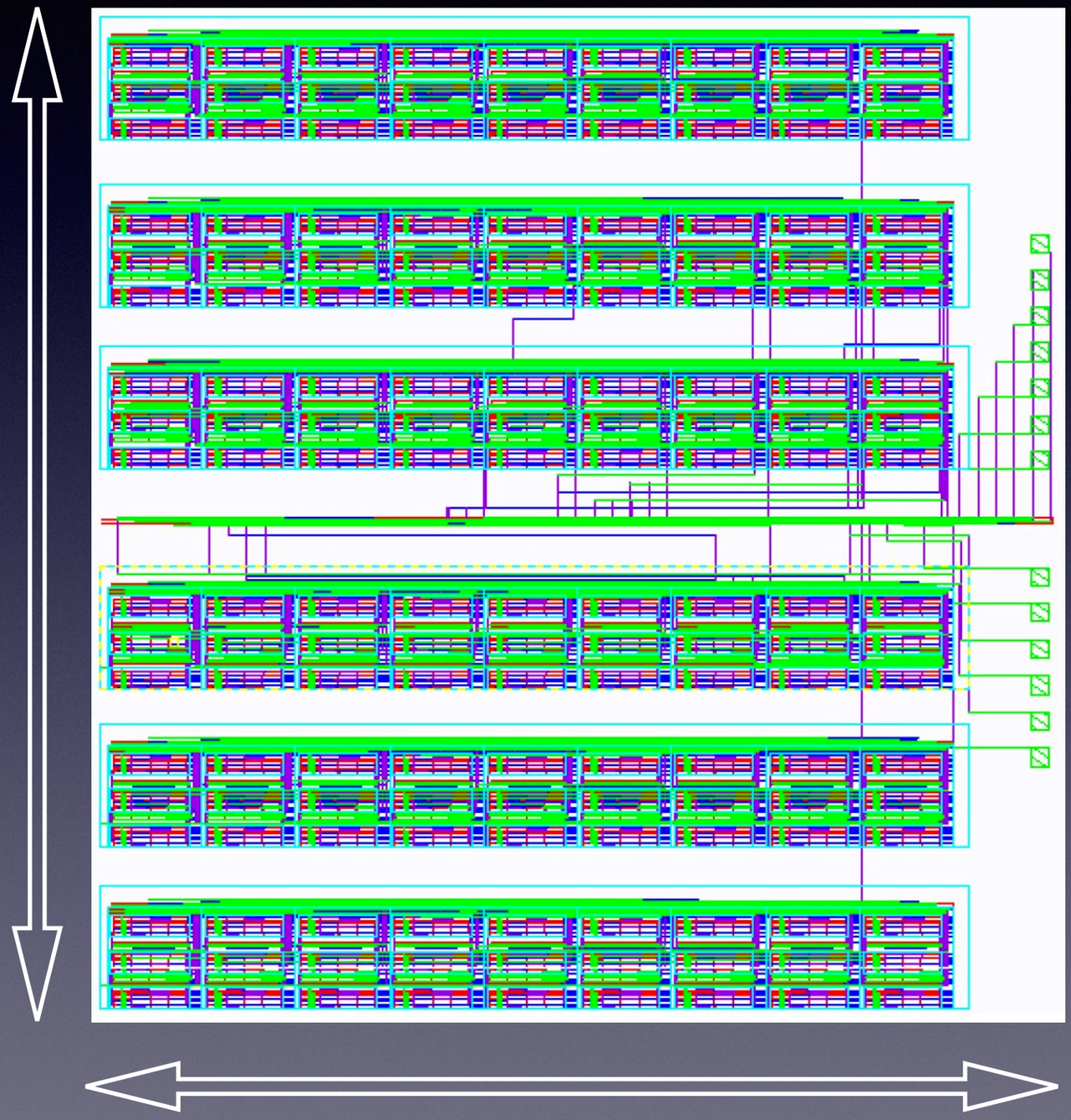
Compute Cell Design



Compute Row Design



Full Layout Design

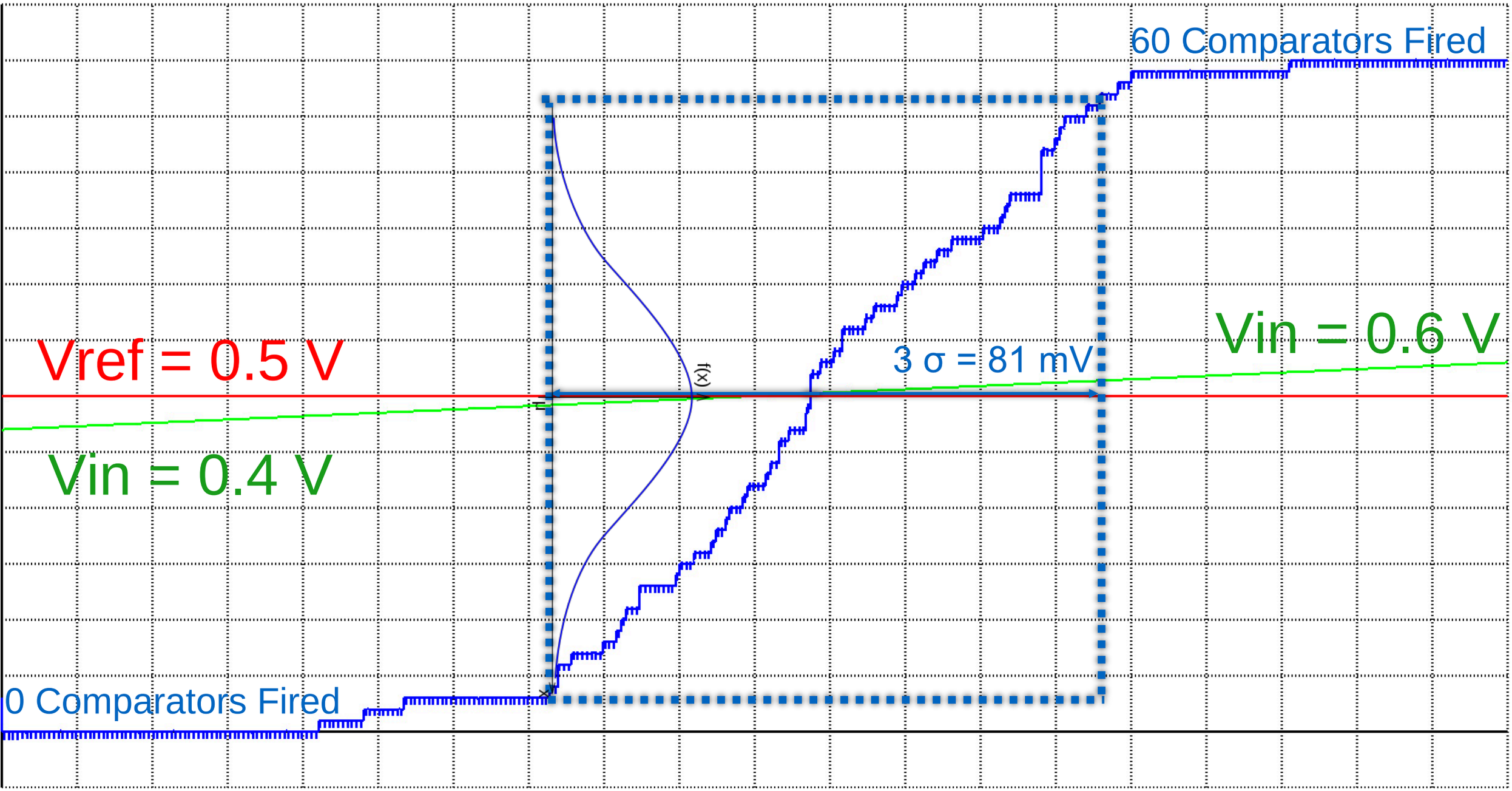


MOSIS

- MOS Implementation Service
  - Operated by the University of Southern California
  - Partners universities with fabs
  - Free for University Courses
- GlobalFoundries’ 130 nm CMOS

Simulation

- Subset of final design
  - 60 comparators (~ 3,000 Transistors)
    - σ_{vt} = 27 mV
- Simulated using:
  - 54 Intel Haswell Server Cores
  - 40 GB RAM
- Voltage ramp over 2 µs with a 10 ns clock and 10 ps step.
- VDD = 1V
- Vref = 0.5 V
- 0.4 V < Vramp < 0.6 V


60 Comparators Fired
Vref = 0.5 V
Vin = 0.6 V
3 σ = 81 mV
f(x)
Vin = 0.4 V
0 Comparators Fired

Conclusion

- A new ADC has been proposed taking advantage of the world of digitally synthesized designs.
- As more transistors fit onto a die - the stochastic ADC becomes viable over analog design work

References

- [1]S. Weaver, B. Hershberg and U. Moon, "Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 1, pp. 84-91, 2014.

- [2]S. Weaver, B. Hershberg, P. Kurahashi, D. Knierim and U. Moon “Stochastic Flash Analog-to-Digital Conversion“, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 11, pp. 2825-2833, 2010.