Development of a LFLE Double Pattern Process for TE Mode Photonic Devices

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I. Project Objectives

Goal: Develop a Litho-Freeze-Litho-Etch(LFLE) process that can be utilized to create TE mode photonic devices.

- Develop a LFLE process that can achieve a minimum feature separation of ~100nm
- Create a two level engineering design mask with aligned positive tone and negative tone images
- Develop a UV cure process to produce a compound resist profile on SOI wafer
- Demonstrate a working TE mode ring resonator device to prove validity of the developed process

II. Motivation

Current SMFL equipment and processes limit photonic device fabrication to TM mode devices.

- TE mode photonic devices require minimum feature separation of ~100nm
- Using a single patterned i-line lithography process can only yield minimum feature separation of ~300nm
- A double patterned LFLE process
  - Can potentially improve efficiency over a more standard LELE process
  - Can potentially achieve minimum feature separation of ~100nm
- Development of a LFLE process will allow creation of TE, TM and mixed mode devices on the same chip

III. Process Development

Proposed LFLE process:

1. Coat, pattern, and develop OiR-620 positive photoresist image
2. Crosslink positive image with a UV Cure process
3. Coat, pattern, and develop NLOF-2020 negative photoresist image
4. Etch a-Si layer to create photonic devices

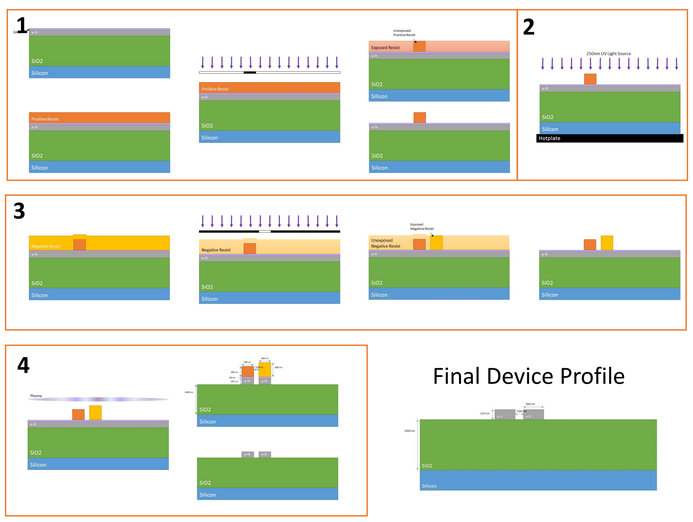

Figure 1. Process Flow Diagram

III. Process Development (Con't)

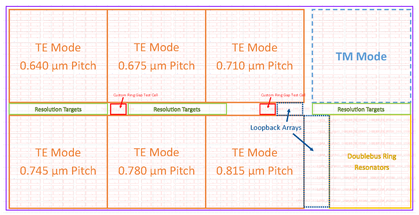

Figure 2. Mask Overview

Mask Design:

- Photonic Device Variations
  - Pitch and duty ratio of grating couplers
  - Waveguide width (500nm-530nm)
  - Feature gap (100nm-375nm)
- Loopback Arrays
- Resolution Targets
- Custom Test Structures

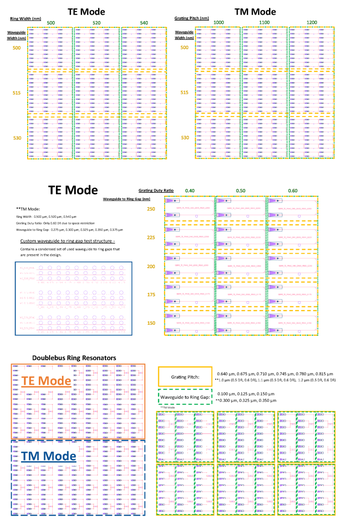

Figure 3. Design Variations

UV Cure Process:

- DOE performed for exposure time and exposure temperature
- Optimum process window determined
  - Optimum exposure time: 7 minutes - 9 minutes
  - Optimum exposure temperature: 130°C - 135 °C
- 250 nm source lamp

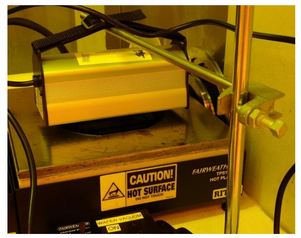

Figure 4. UV Cure Setup

IV. Experimental Results

Initial Lithography Results:

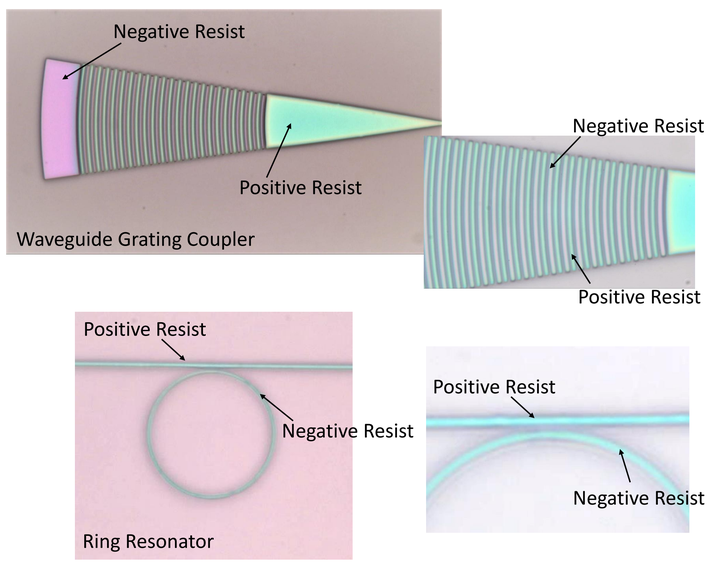

Figure 5. Compound Photoresist Image

IV. Experimental Results (Con't)

Initial Etch Results:

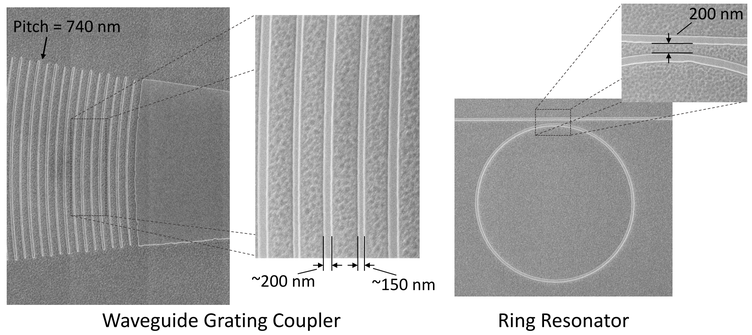

Figure 6. Image Etched in Silicon

V. Conclusions

- Obtained successful results from experimental process:
  - Minimum obtained feature size ~150 nm
  - Minimum obtained feature separation - ~100 nm
- Developed a working UV cure process using readily obtained positive and negative tone resists
- Developed a working LFLE process that can be refined to fabricate working TE mode photonic devices
- Created a two layer engineering design mask adequate for future work

Future Work:

- Lithography optimization for SOI wafer
  - Account for changes in stack reflectivity
  - Separate optimization for positive and negative layers
- Optical Proximity Correction (OPC) mask design
  - Corrections for bulging in ring to wave guides gap
  - Corrections for fine pitch grating couplers
- Etch Recipe Optimization for compound resist image

References:

[1] M. Maenhoudt, "Alternative process schemes for double patterning that eliminate the intermediate etch step", Proc. of SPIE Vol. 6924, 2008.
[2] M. Hori, et al., "Sub-40nm Half-Pitch Double Patterning with Resist Freezing Process", Proc. of SPIE Vol. 6923, 2008.
[2] C. Shay, "CD Reduction through Annular Illumination and Sidewall Spacer Etch", Senior Design, Rochester Institute of Technology, 2016.
[3] P. Cadareanu, "Silicon Photonic Devices Manufactured Using DoublePatterned iLine Lithography", Rochester Institute of Technology, 2016.

Acknowledgements

- Advisors: Dr. Stephen Preble, Dr. Dale Ewbank, Dr. Robert Pearson
- Sanjna Lakshminarayanamurthy
- Cornell University who allowed us to fabricate a mask
- Special thanks to all the SMFL Staff