Stochastic Analog to Digital Converter Using Standard Cells

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I. Project Objectives

Goal: Create an ADC without an analog front end using only standard cells and automated digital IC design tools

- Provide a means to bring analog IC design into the modern, automated, digital world
- Fabricate an IC using MOSIS (Metal Oxide Semiconductor Implementation Service)
- Design tutorials for future endeavors

II. Motivation

Analog design is virtually impossible to automate and difficult to scale. Capacitors and resistors used in typical Flash or SAR ADCs do not scale linearly with process technology, and these ADC designs require special layout considerations due to their analog and noise-prone nature.

An ADC based on a digital stochastic design requires a large number of transistors (~90,000 for a 5-bit design). However, future scaling benefits will result in better, faster, and cheaper ADCs due to automated design synthesis and reduced R&D costs.

III. Basis of Operation

- No two transistors are identical
- On GlobalFoundries 130 nm CMOS process, threshold voltage variation can exceed 100 mV
- As a result, comparators will trigger with an offset directly related to the severity of the threshold variation
- The number of comparators triggered is directly related to input voltage
- A 3-input NAND latch creates a race condition down the NMOS branches, whichever sets first (has higher current drive), latches the system.
- Adder circuitry (Wallace Tree Adder) and linearization logic is needed to condense the comparator outputs to a readable, reliable digital code (Fig 6.)

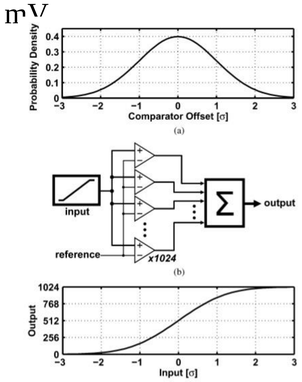

Figure 1. Comparator Offset can be modeled as a probability function, giving rise to an output related to the strength of the input

IV. Experimental Results

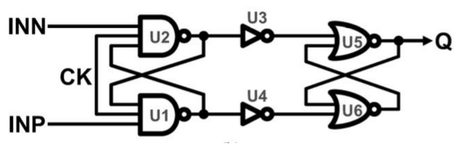

Figure 2. Comparator using standard cells

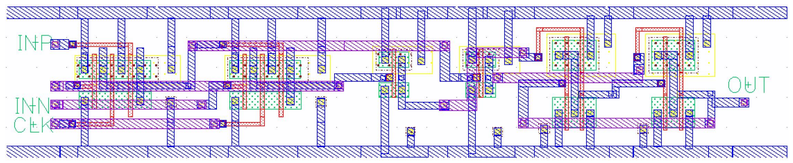

Figure 3. Layout of Figure 2 using GlobalFoundries 130nm CMOS technology

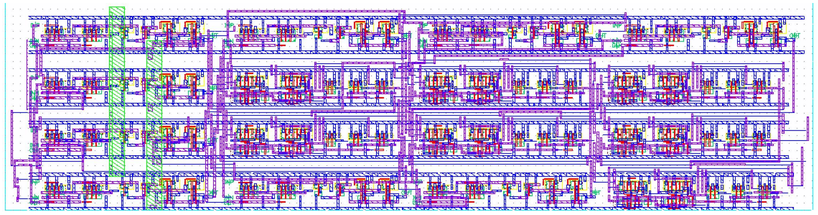

Figure 4. 'Compute Cell' Consisting of 9 comparators and 7 full adders

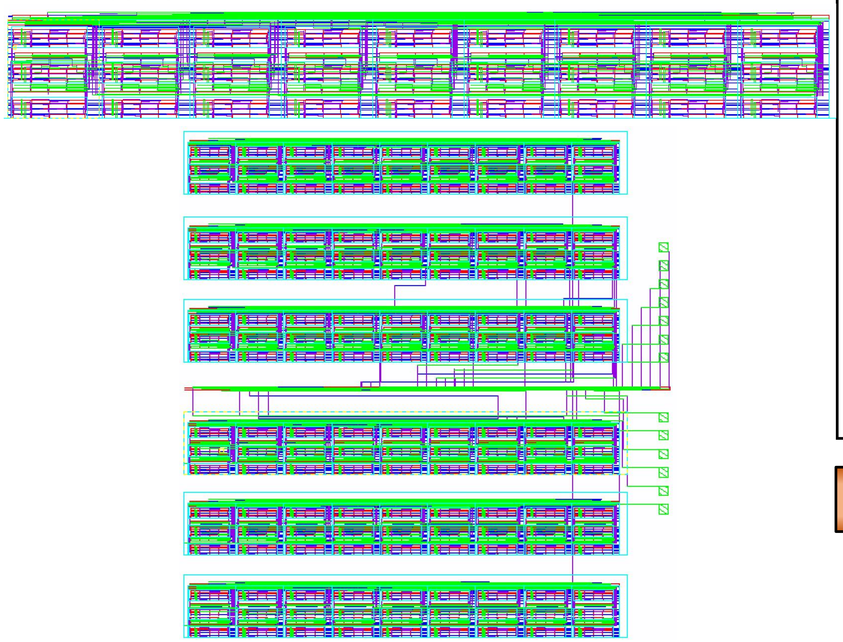

Figure 5. (top) A Compute row consisting of 27 Compute Cells; (bottom) 6 Compute Rows (1,452 comparators) routed in a 1.4 mm X 1.3 mm die to produce a 5-bit ADC.

Results (con't)

$$f(v) = \begin{cases} 2v + v/2 - 1049 & : & 775 > & v \\ v + v/2 - 274 & : & 549 < & v & \leq 775 \\ v & : & -549 \leq & v & \leq 549 \\ v + v/2 + 274 & : & -775 \leq & v & < -549 \\ 2v + v/2 + 1049 & : & & v & < -775 \end{cases}$$

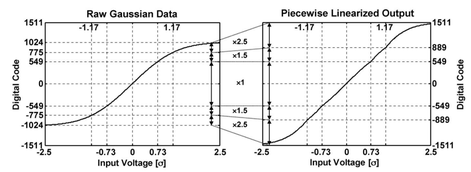

Figure 6. Linearization computation needed for linear best fit

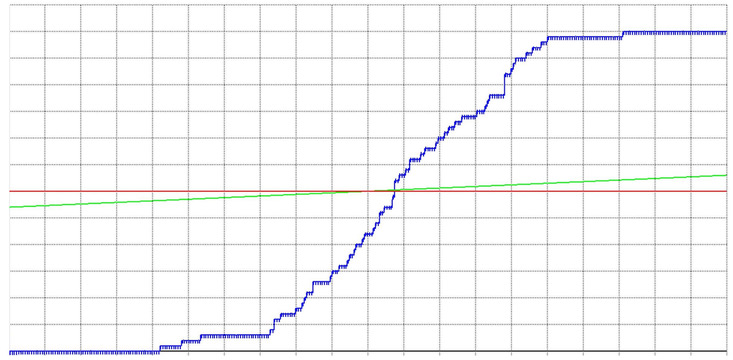

Figure 7. Digital output from a simulation of 60 comparators with a reference voltage of 500 mV (red), and an input ramp from 400 mV to 600 mV (green). The output (blue), shows the random comparator offset variation.

V. Conclusions

Through theory and simulation, the device functions as a useful alternative to traditional analog front end ADCs

Future Work

- Perform DRC and LVS
- Fabricate through MOSIS
- Test characteristics

References

[1]S. Weaver, B. Hershberg and U. Moon, "Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 1, pp. 84-91, 2014.

[2]S. Weaver, B. Hershberg, P. Kurahashi, D. Knierim and U. Moon "Stochastic Flash Analog-to-Digital Conversion", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 11, pp. 2825-2833, 2010.

Acknowledgements

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- Dr. Fuller