Ferroelectric HfO_2 Thin Films

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JACKSON ANDERSON

ELECTRICAL AND MICROELECTRONIC ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

Outline

Introduction
- Background
- Project Objectives

Experimental Results
- Deposition of Doped HfO_2 Thin Films
- CV Measurements
- Hysteresis Measurements

Conclusions and Future Research

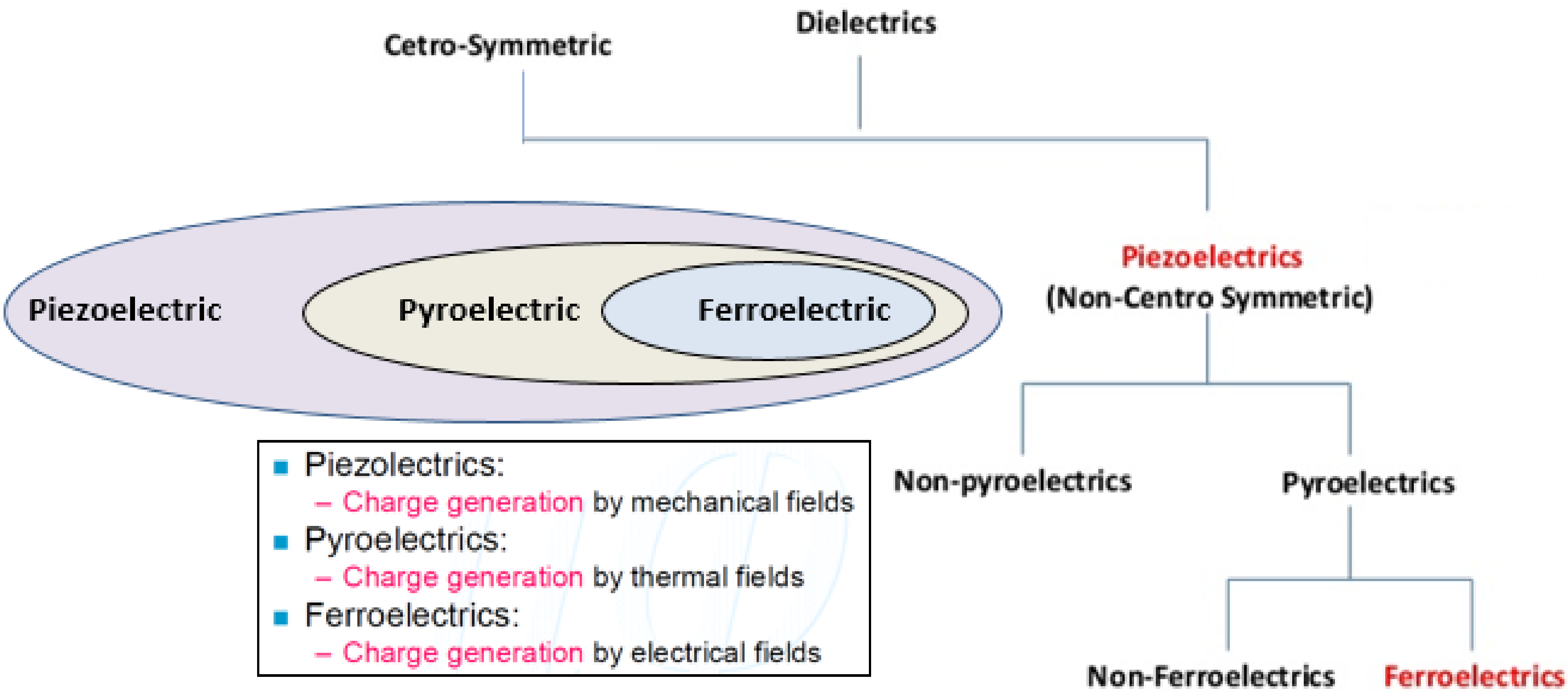
Outline

Introduction

Experimental Results

Conclusions and Future Research

What is Ferroelectricity?



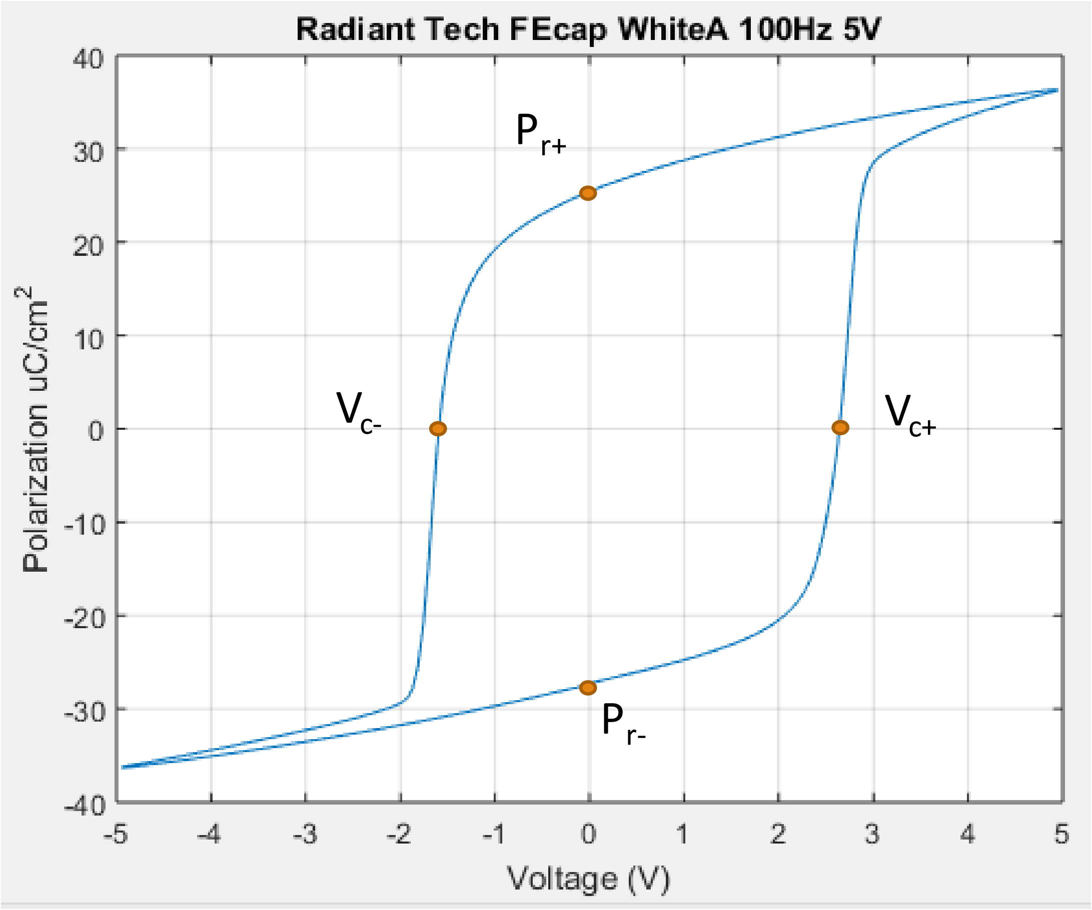
Measurements of Ferroelectricity

Remnant Polarization:

- Polarization in ferroelectric material when no bias applied

Coercive Voltage/Field:

- Voltage/E-field when no polarization is present



Benefits of Ferroelectric Memory (FeFET)

Sub-100ns read/write times (Yurchuk, 2014)

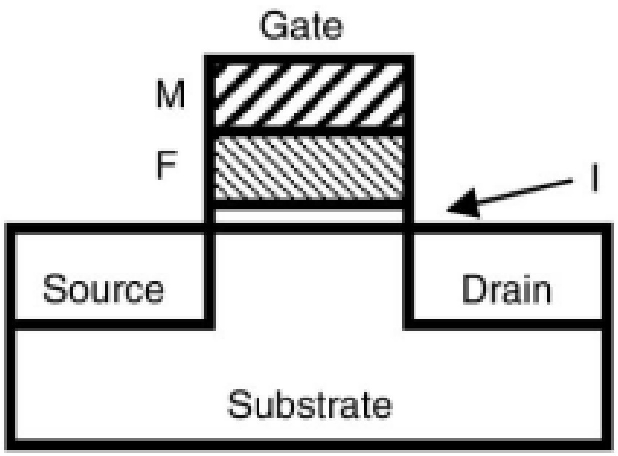
Smaller footprint than DRAM

- 1T vs 1T1C

Potential for use in non-volatile applications

- Memory window of over 1V shown after 10 days (HfO_2) (Yurchuk, 2014)
  - 10 year memory window projected for HfO_2 and traditional materials (ITRS, 2013)
- Lower write voltages than floating gate or charge-trap memories
  - 4-6 V vs 10-15 V required for floating gate (Yurchuk, 2014)

Non-charge based



Arimoto, 2004

Challenges with Traditional Ferroelectric Materials

Lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT) most common ferroelectric films

These films likely not scalable beyond 22 nm node

- Low coercive field requires thick ferroelectric layer to obtain useful memory window
- Thick buffer layer required between ferroelectric gate and channel to limit inter-diffusion
- Depolarization field caused by buffer layer decreases retention time

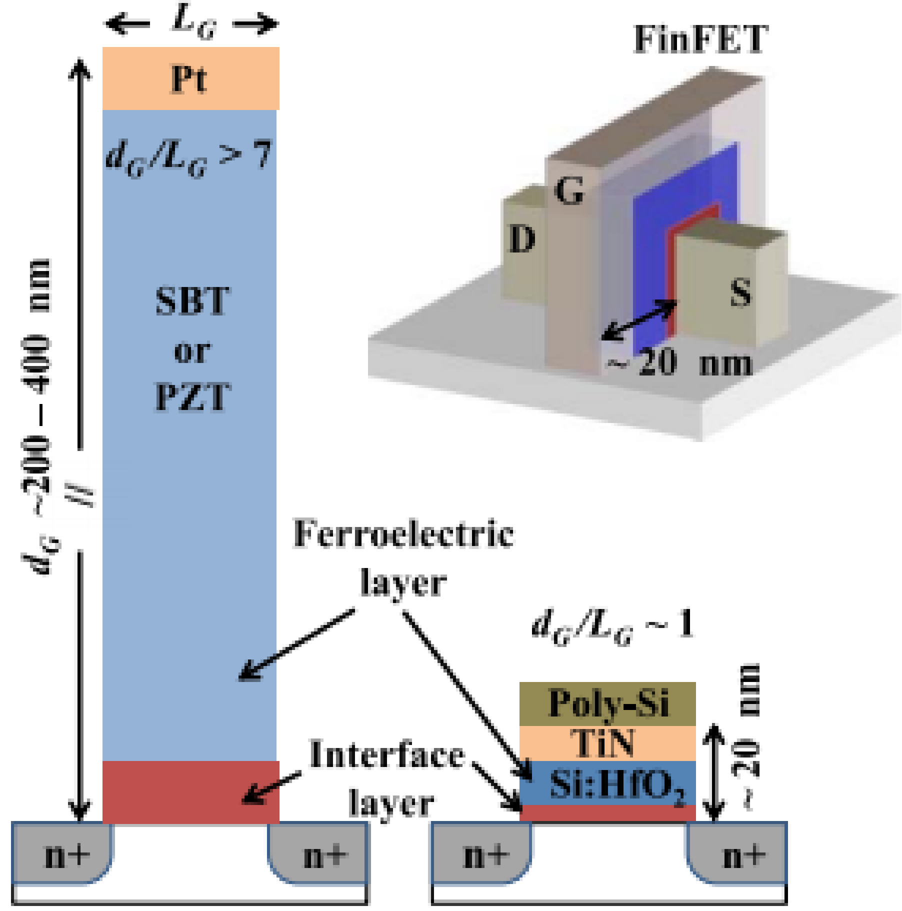
ITRS, 2013

Why HfO_2?

Higher coercive field allows for thin ferroelectric layer, enabling continued scaling of FeFETs

Doesn't require thick buffer layer – decreases depolarization field, increasing theoretical retention time

Familiar material – can leverage high-k metal gate (HKMG) process knowledge



Yurchuk et al, 2014.

Ferroelectricity Reported in a Variety of HfO_2 Films

Ferroelectric HfO_2 first reported in 2011 (Si, 4% mol, ALD) (Boesck, 2011)

- Observed with other dopants such as Al and Y (Schroeder, 2013)

Ferroelectric behavior also seen in sputtered Y-doped HfO_2 (Schroeder, 2013)

Year	Dopant	mol %	P_r (µC/cm²)	E_c (MV/cm)
2011	Si	3.8	10	1
2013	Al	5 - 7	16	1.3
2013	Y (ALD)	2.5 - 5.5	24	1.2
2013	Y (sputtered)	2.5 - 5.5	10	1.5
2013	Si	3.5 - 4.5	14-24	1

Project Objectives

1. Develop a process for fabrication of ferroelectric HfO_2 devices using tools available in the RIT Semiconductor and Microsystems Fabrication Laboratory (SMFL)
   - Sputtered HfO_2 film (no Atomic Layer Deposition)

2. Enable in-house characterization of ferroelectric films through the installation and qualification of a newly purchased ferroelectric test system

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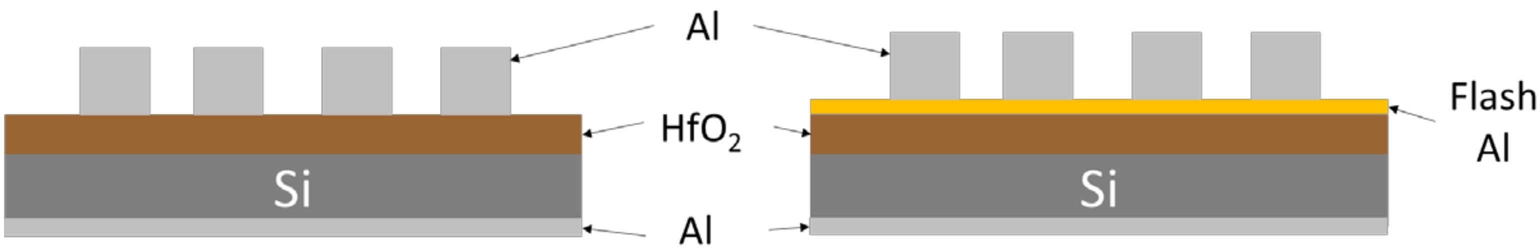
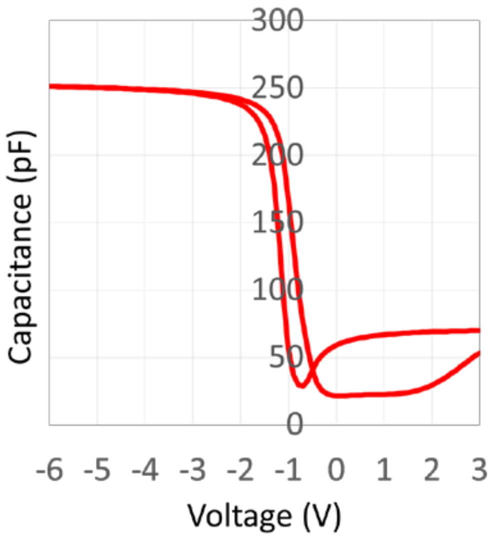
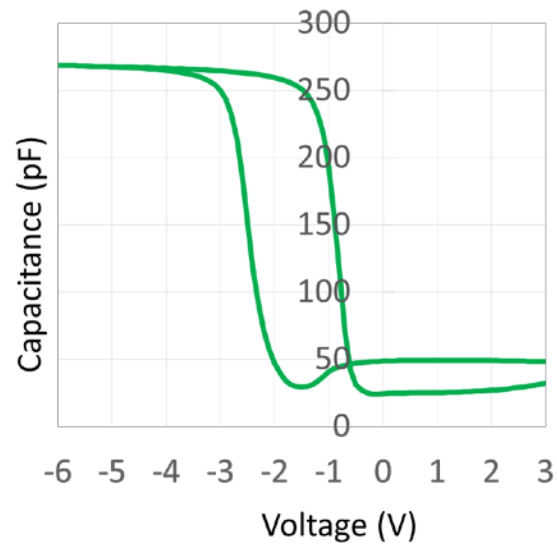
Previous RIT Work



Sample 1: MIS Al/HfO$_2$/Si

Sample 2: MIS Al/Al:HfO$_2$/Si



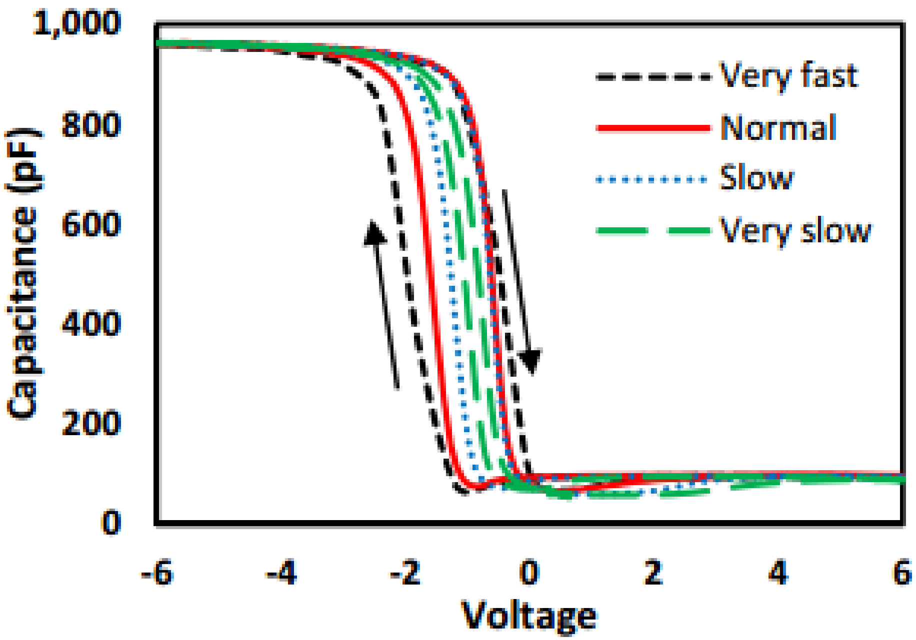


M. Witulski, Senior Design 2014.

CV Window Changes with Sweep Speed

Window in CV likely caused by charges rather than ferroelectricity

Speed	Speed measurement	Sweep step (V)	Delay (s)
Fast	Fast	0.5	0.5
Normal	Normal	0.1	1
Slow	Slow	0.04	3
Very slow	Slow	0.02	10

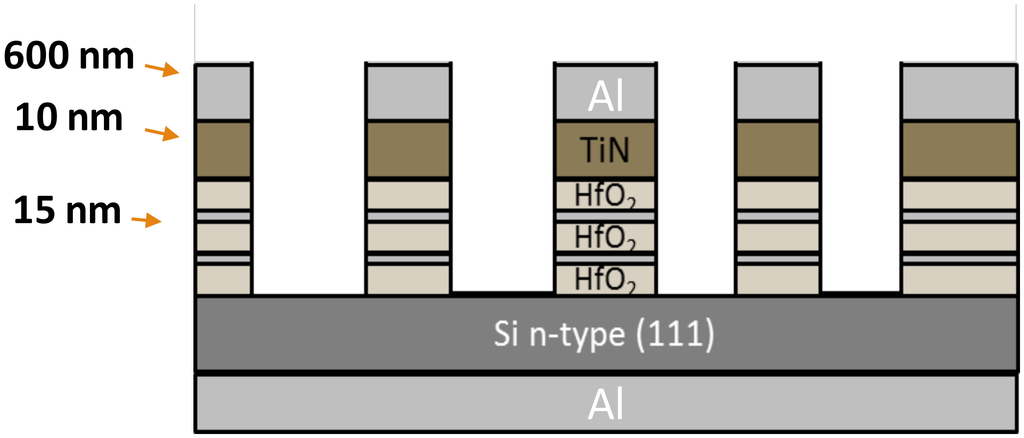


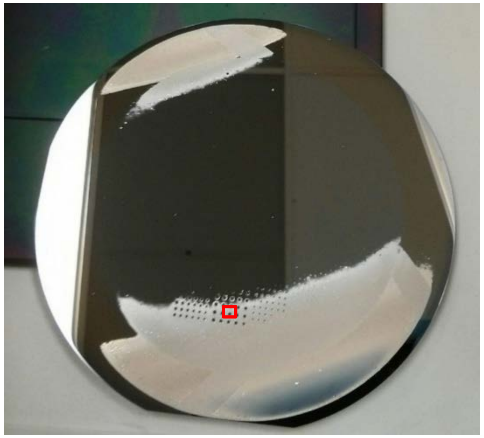
HfO_2/Al Sandwich Approach for More Uniform Doping

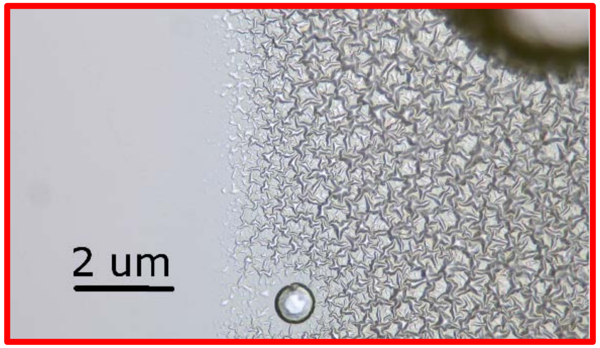
HfO_2/Al deposited via alternating sputter without breaking vacuum

Some devices exhibited mechanical failure of film stack after anneal

- Additional layers added stress to the system
- Additional interfaces provided more points for failure







Al Solid Source Doping Revisited

10 nm TiN Reactive Sputter (D1,D2)

15 nm HfO_2 Reactive Sputter (all wafers)

5 nm Aluminum Layer

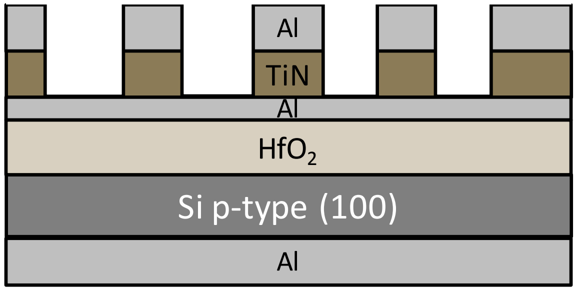
- Evaporation (D1, D4)
- Sputtering (D2, D3)

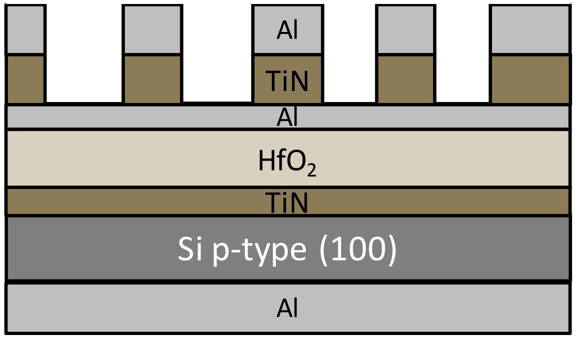
Sputter & Lift-off Top 10 nm TiN (half of each wafer)

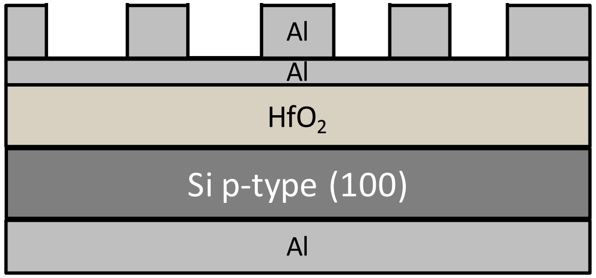
Anneal – RTA or Furnace

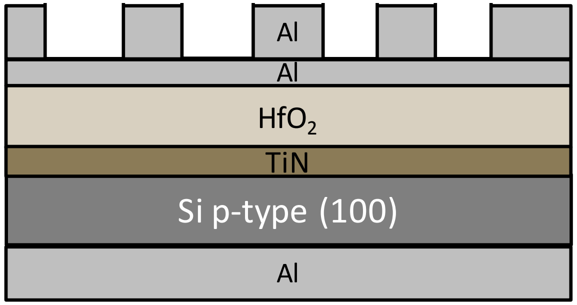
Evaporate & Lift-off Top Al (600 nm)

Evaporate Back Al (600 nm)









Experimental Matrix

Device Wafers				
Label	Bottom TiN	Al Dep Method	Top TiN	Anneal
D1A	Yes	evaporation	Yes	RTA
D1B	Yes	evaporation	Yes	Furnace
D1C	Yes	evaporation	No	RTA
D1D	Yes	evaporation	No	Furnace
D2A	Yes	sputter	Yes	RTA
D2B	Yes	sputter	Yes	Furnace
D2C	Yes	sputter	No	RTA
D2D	Yes	sputter	No	Furnace
D3A	No	evaporation	Yes	RTA
D3B	No	evaporation	Yes	Furnace
D3C	No	evaporation	No	RTA
D3D	No	evaporation	No	Furnace
D4A	No	sputter	Yes	RTA
D4B	No	sputter	Yes	Furnace
D4C	No	sputter	No	RTA
D4D	No	sputter	No	Furnace

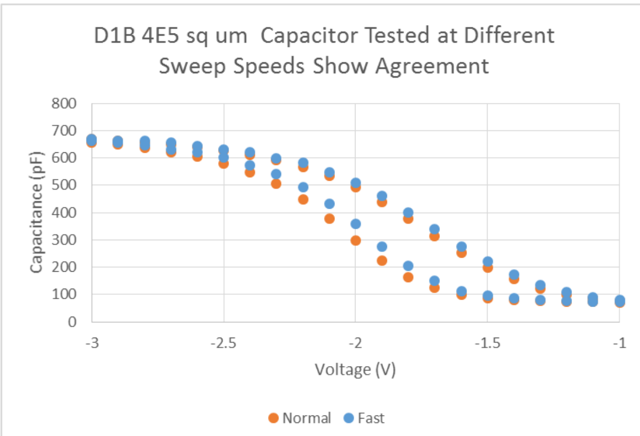
Al Developed Away

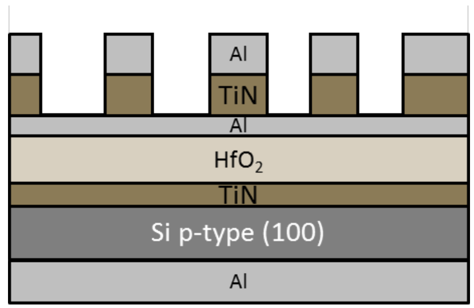
Al Developed Away

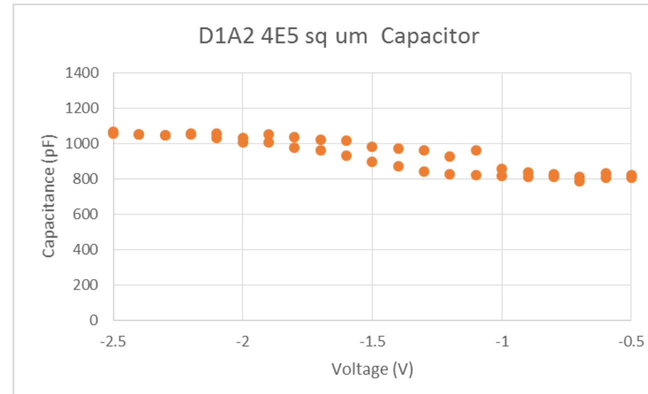
Promising Results Seen in Samples with TiN Cap

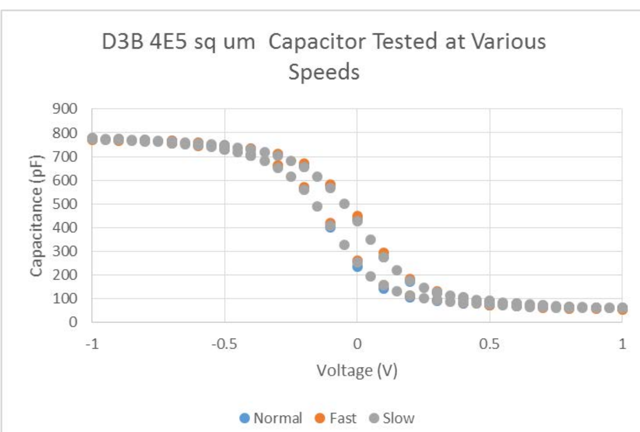
Furnace - 1hr 600°C

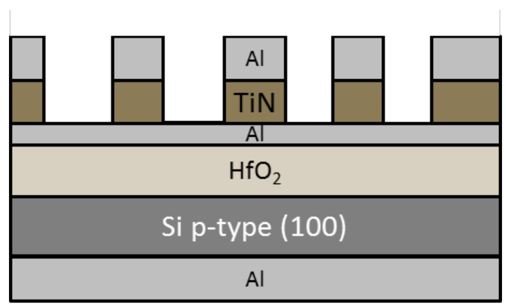
RTA - 20s 850°C

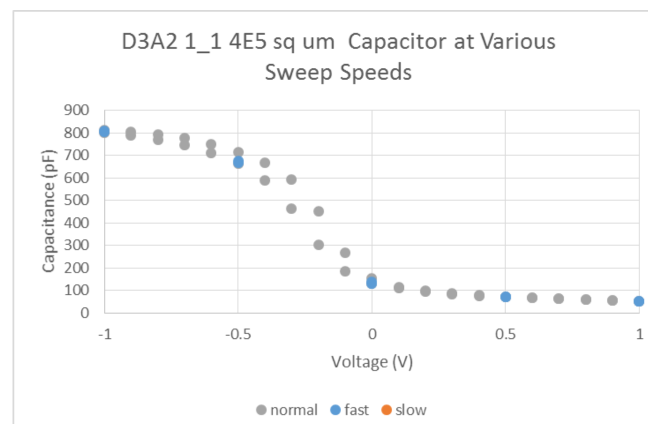








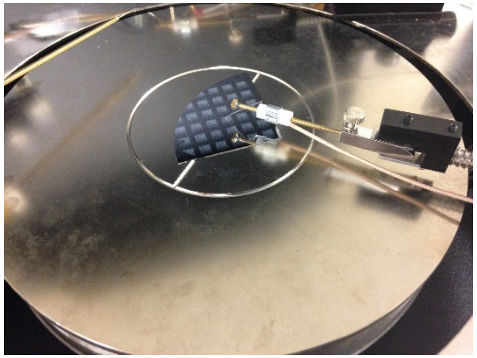


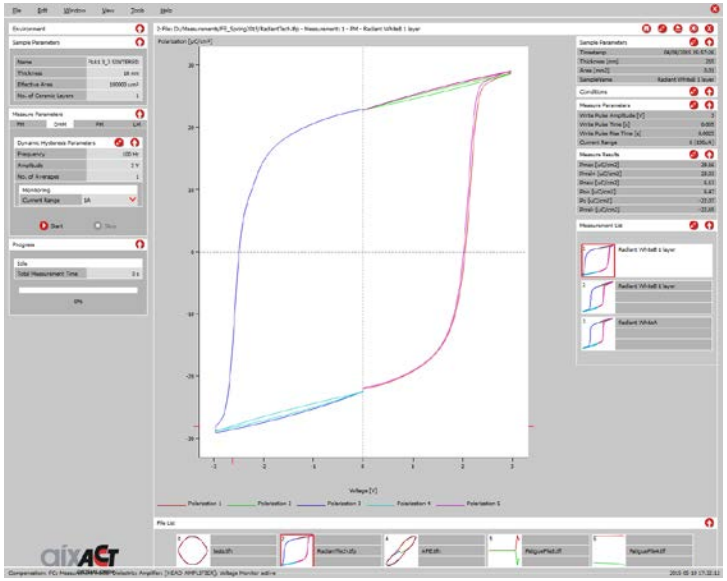


New Ferroelectric Test System Installed

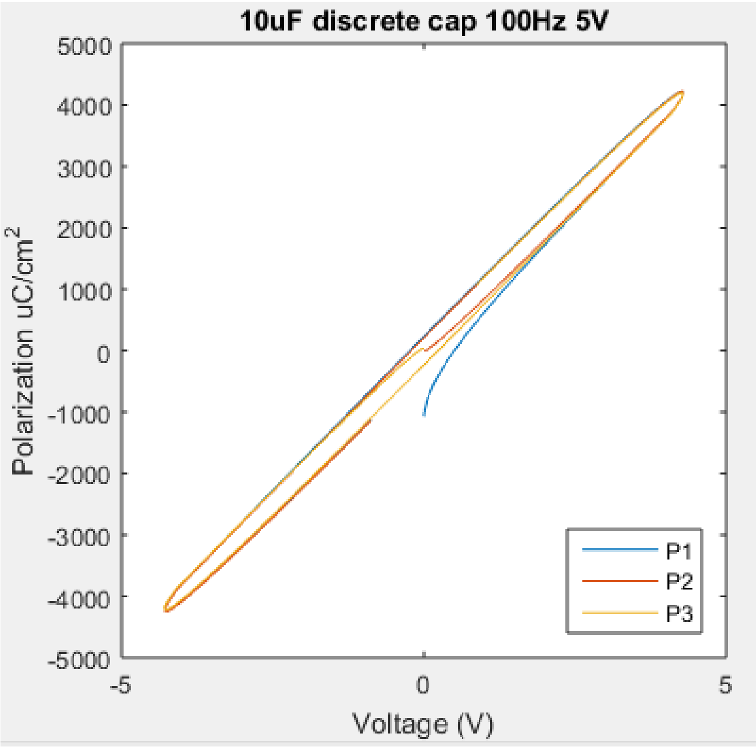
Advanced Customized Characterization Technologies TF Analyzer 1000 (TF 1000) allows for:

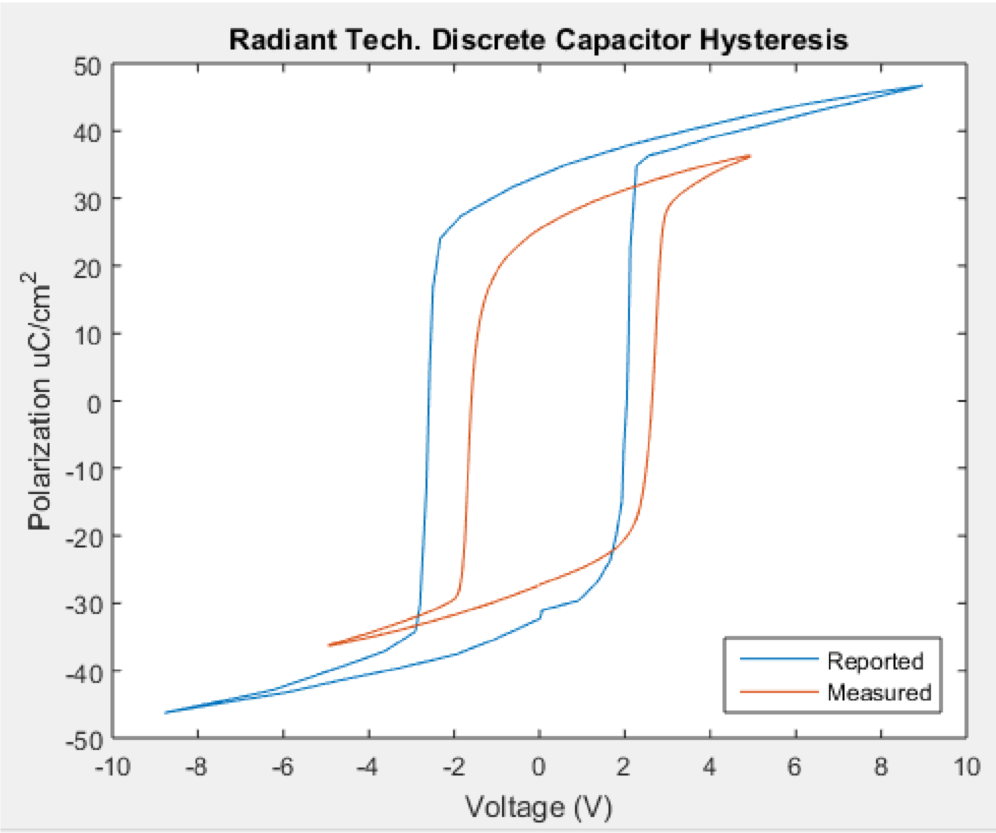
- Hysteresis measurement
- PUND testing
- Leakage current measurement
- Fatigue measurement





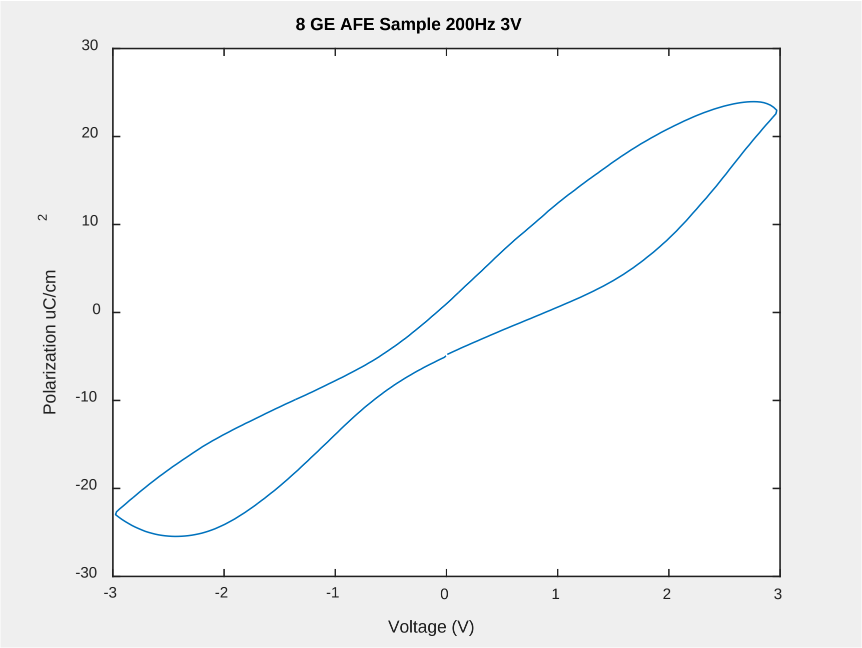
Discrete Component Measurement

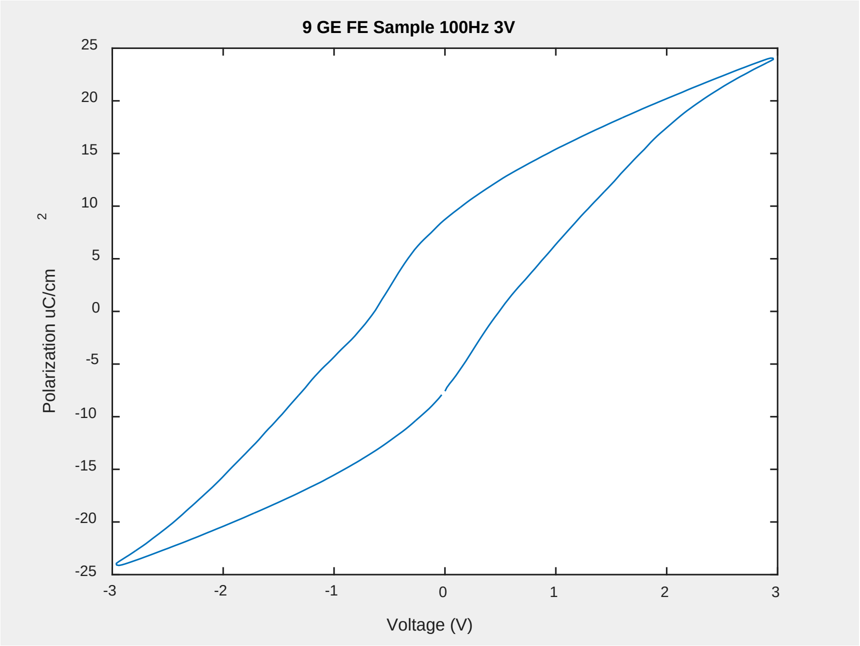


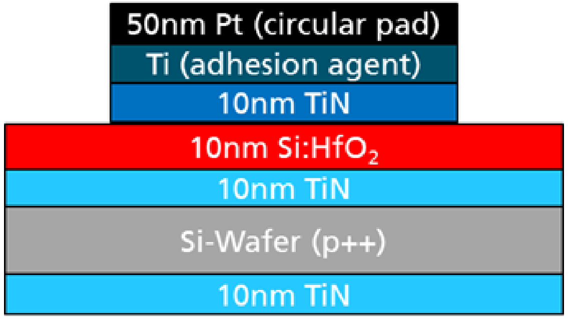


Evans, 2008

NaMLab Ferroelectric and Antiferroelectric HfO_2







Conclusions and Future Research

Conclusions:

- A top TiN layer along with a low-temperature anneal are key in coercing sputtered Al:HfO_2 into a ferroelectric phase
- RIT is prepared to characterize fabricated ferroelectric devices
  - aixACCT TF Analyzer 1000 proven on both discrete PZT and ferroelectric HfO_2 samples
- Doped HfO_2 is a strong contender for enabling scalable FeFETs
  - Comparable memory window to PZT can be achieved with a film 10x thinner

Future Areas of Research:

- Materials analysis to investigate effects of Al solid-source diffusion and anneal method on ferroelectric phase formation in HfO_2
- Fabrication of MIM capacitors to allow easy hysteresis measurement
- Modeling of the impact of depletion capacitance on the hysteresis measurement to allow characterization of MIS capacitors
- Fabrication and testing of FeFETs using a modified RIT CMOS process

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The entire SMFL Staff

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References

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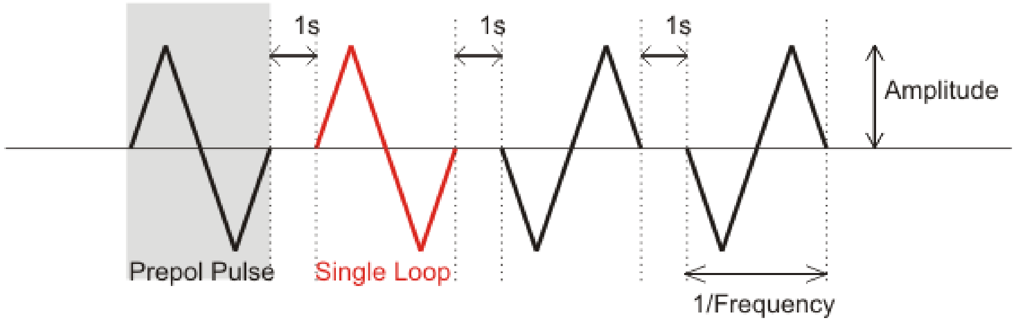
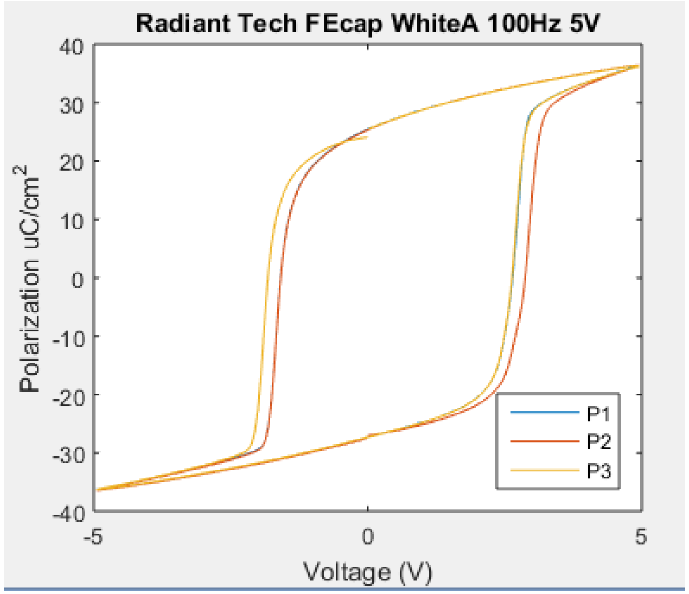
Thank You.

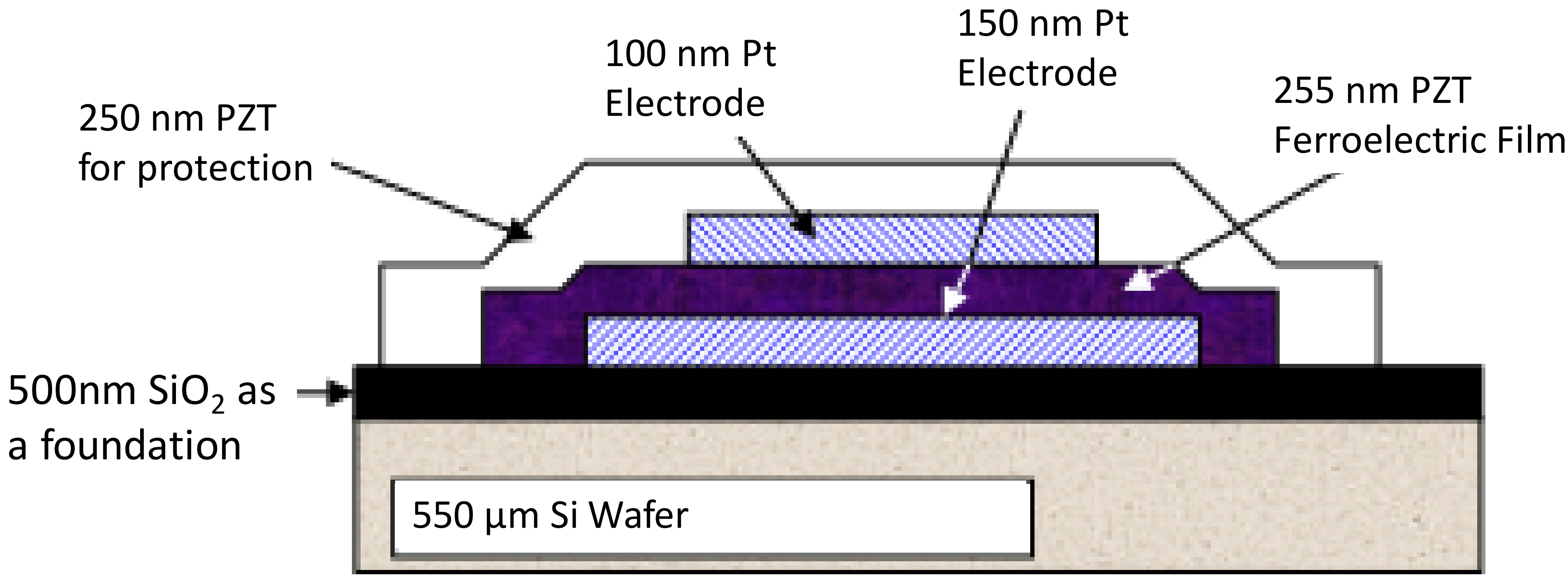
Backup

Dynamic Hysteresis Measurement (DHM)



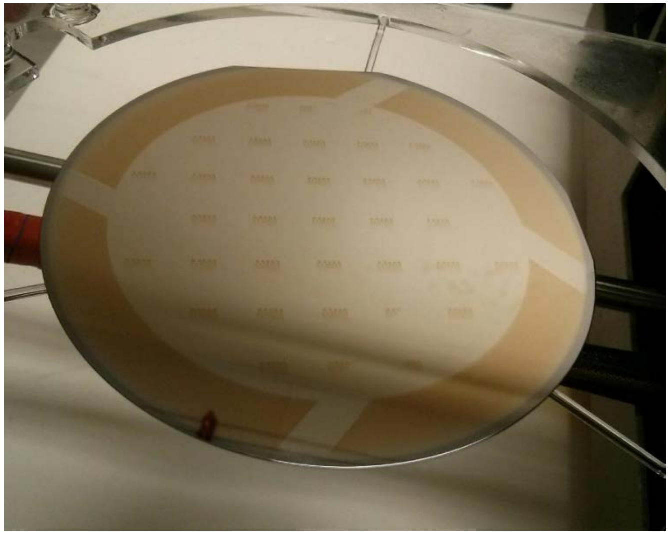


Discrete Ferroelectric Capacitor Structure



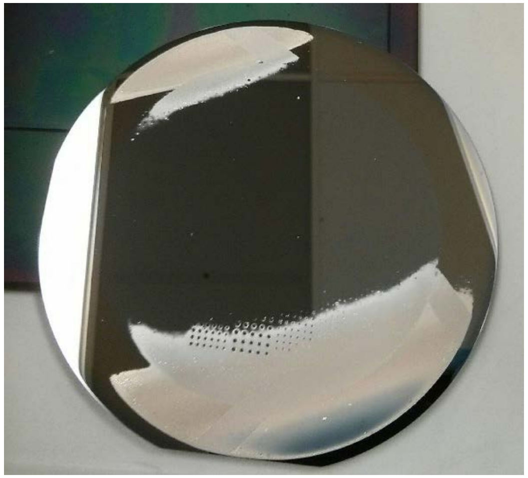
Evans, 2008

Doped Capacitors After Anneal



850°C 20s

1000°C 20s

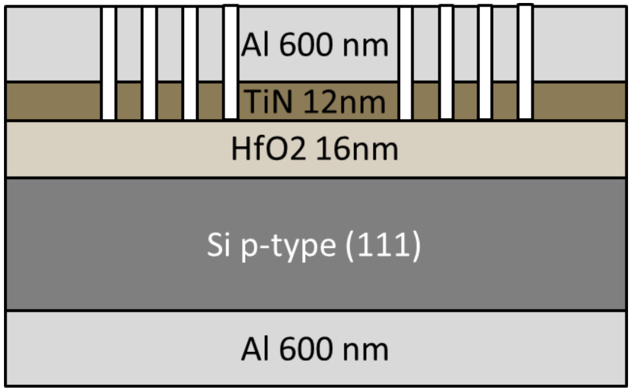


Undoped Shadow Mask Reference Capacitors

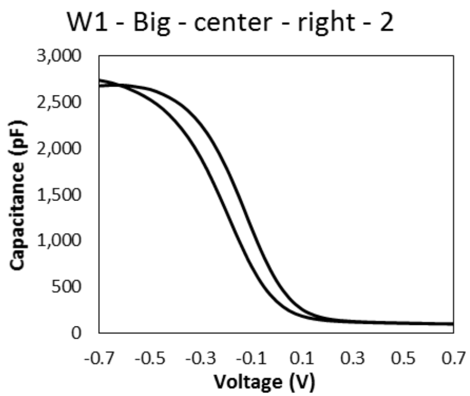
P-type 111 wafers

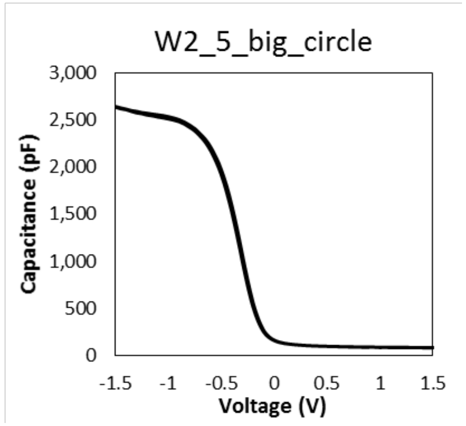
Anneal

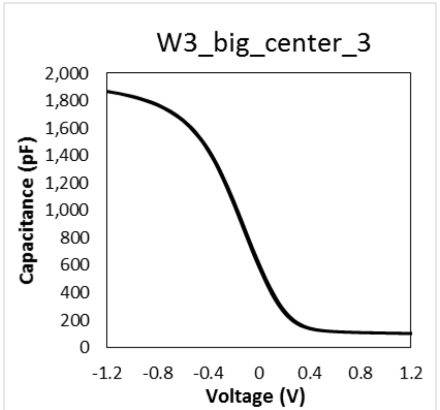
- Wafer 1: 1000 C
- Wafer 2: 870 C (850 target)
- Wafer 3: 740 C (700 target)

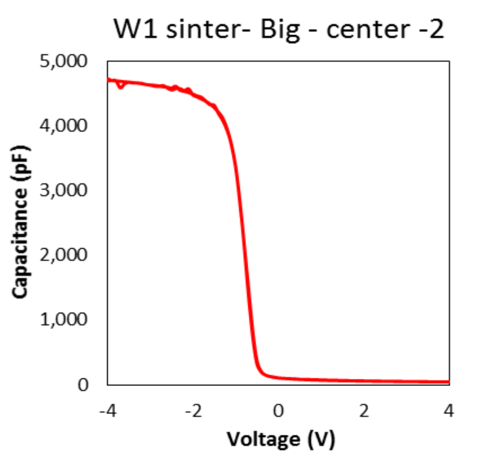


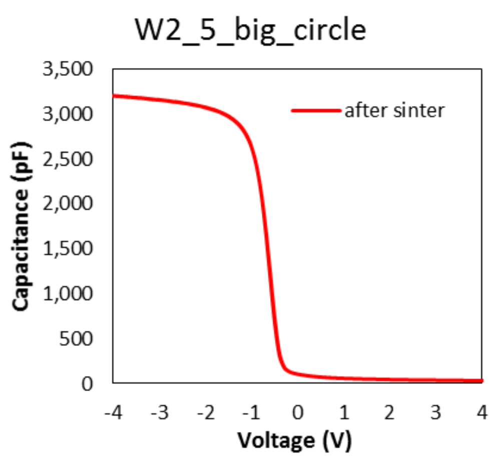
Reference Capacitors (Fabricated without Doping)

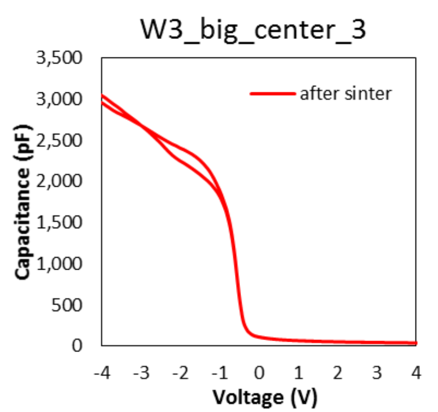






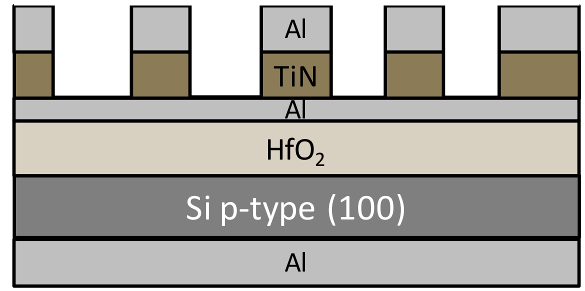


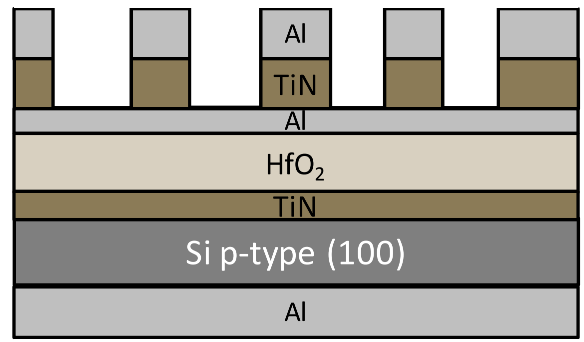


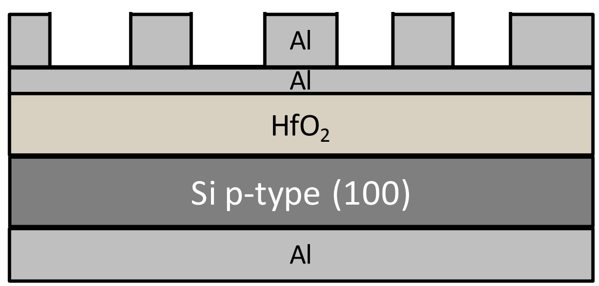


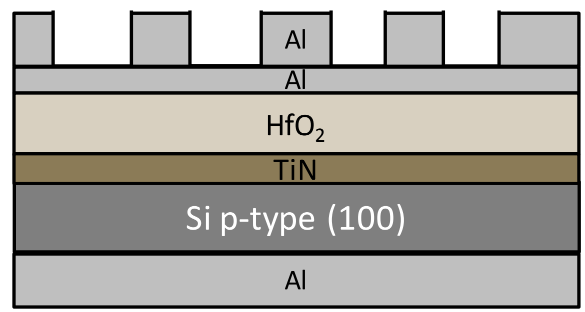
Al Solid Source Doping Revisited

- 10 nm TiN Reactive Sputter (D1,D2)
- 15 nm HfO_2 Reactive Sputter (all wafers)
- 5 nm Aluminum Layer
  - Evaporation (D1, D4)
  - Sputtering (D2, D3)
- Sputter & Lift-off Top 10 nm TiN (half of each wafer)
- Anneal – RTA or Furnace
- Evaporate & Lift-off Top Al (600 nm)
- Evaporate Back Al (600 nm)

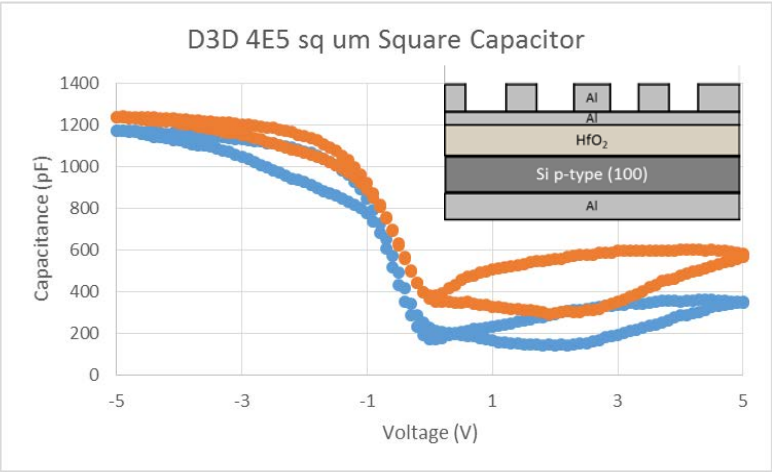




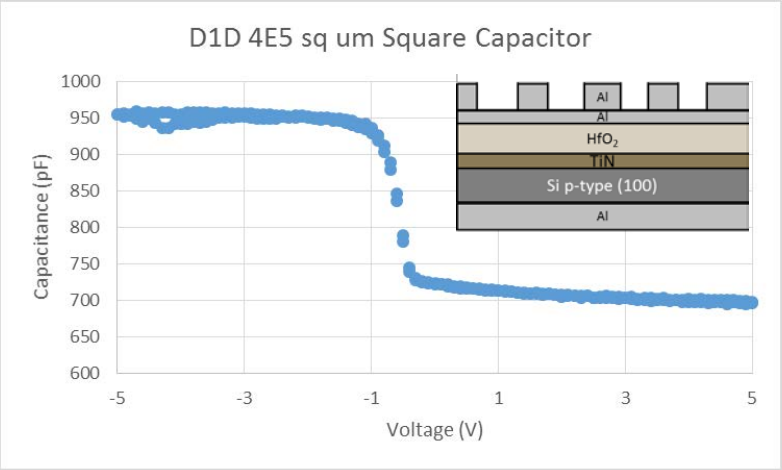




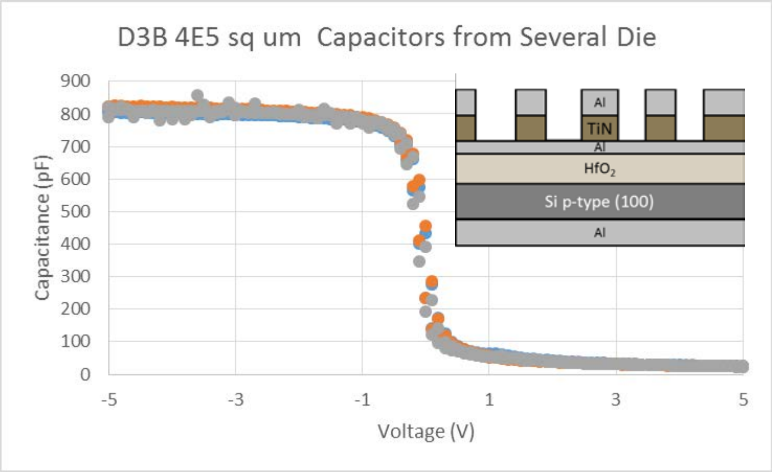
CV Results



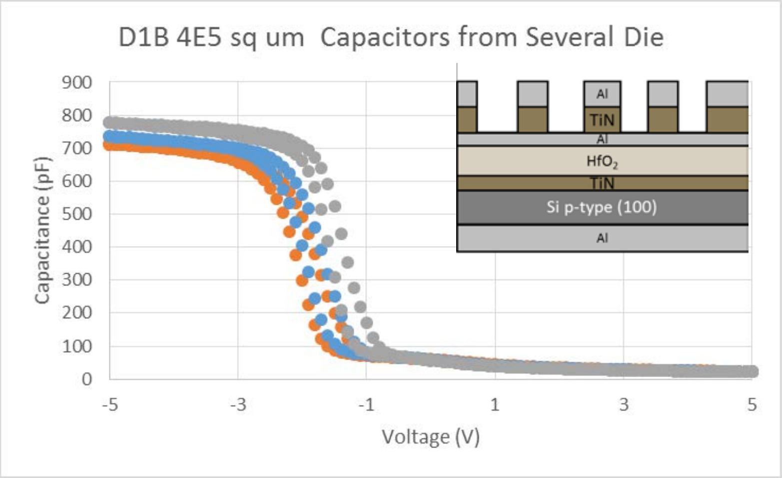
D3D 4E5 sq um Square Capacitor
Capacitance (pF)
Voltage (V)
1400
1200
1000
800
600
400
200
0
-5
-3
-1
1
3
5
Al
Al
HfO2
Si p-type (100)
Al



D1D 4E5 sq um Square Capacitor
Capacitance (pF)
Voltage (V)
1000
950
900
850
800
750
700
650
600
-5
-3
-1
1
3
5
Al
Al
HfO2
TiN
Si p-type (100)
Al



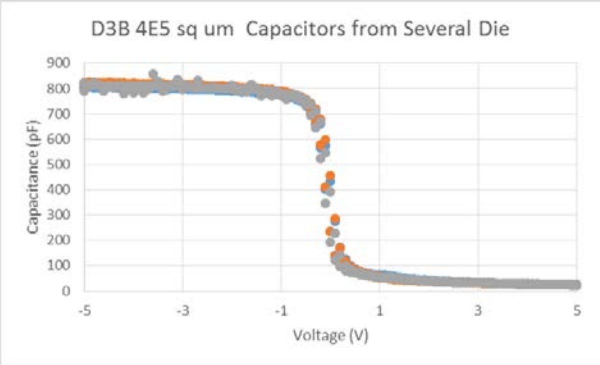
D3B 4E5 sq um Capacitors from Several Die
Capacitance (pF)
Voltage (V)
900
800
700
600
500
400
300
200
100
0
-5
-3
-1
1
3
5
Al
TiN
Al
HfO2
Si p-type (100)
Al

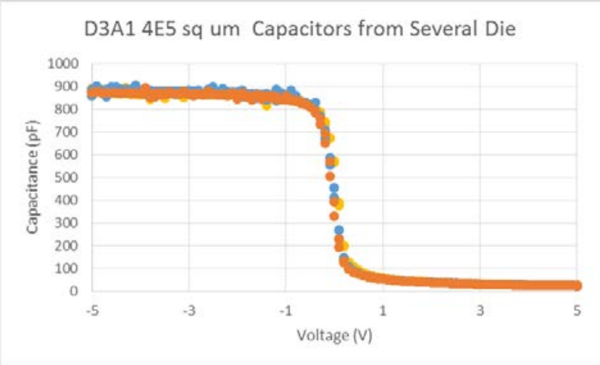


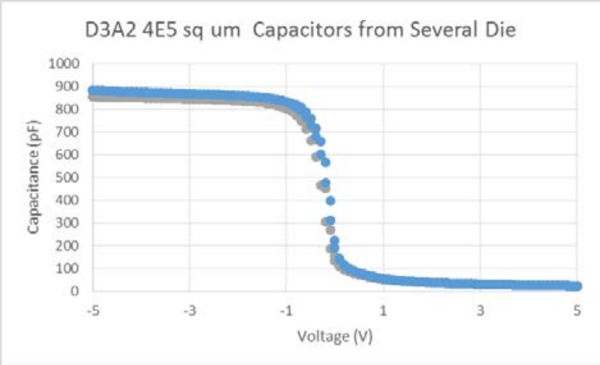
D1B 4E5 sq um Capacitors from Several Die
Capacitance (pF)
Voltage (V)
900
800
700
600
500
400
300
200
100
0
-5
-3
-1
1
3
5
Al
TiN
Al
HfO2
TiN
Si p-type (100)
Al

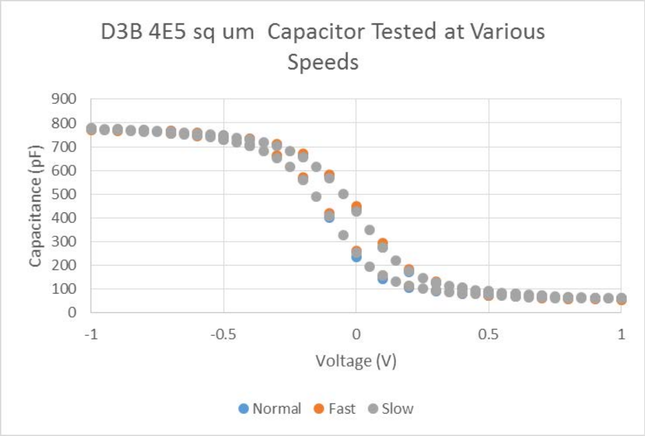
Top TiN Only

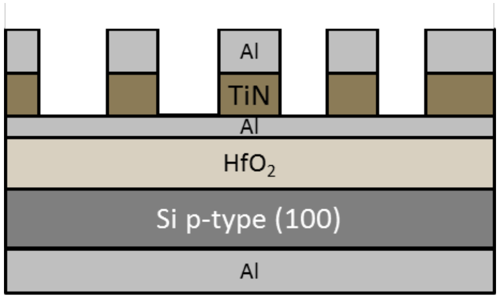
Furnace - 1hr 600°C	RTA - 1s 1000°C	RTA - 20s 850°C

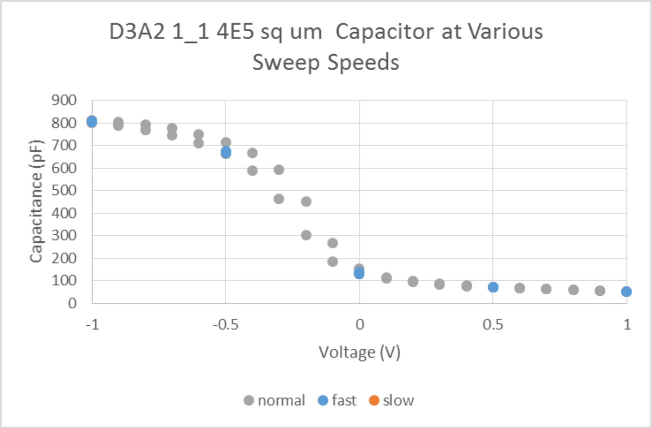






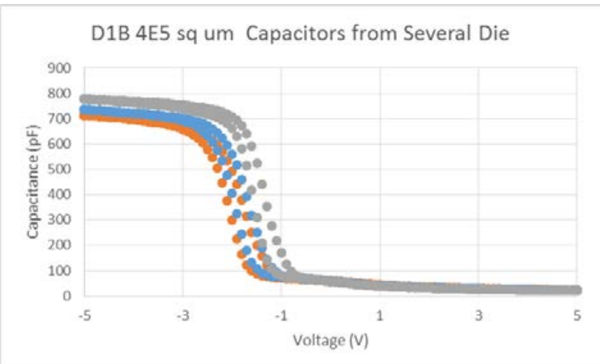




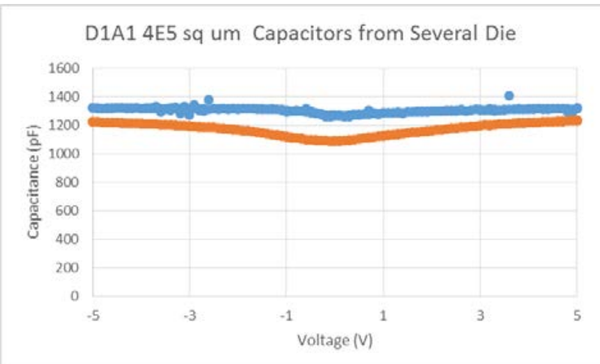


Top and Bottom TiN

Furnace - 1hr 600°C



RTA - 1s 1000°C



RTA - 20s 850°C