Touch and Display Driver Integration (TDDI) Architecture Considerations for System Level ESD

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I. Project Objectives

Goal: Evaluate component level design constraints to assist in system level electrostatic discharge (ESD) requirements for Touch and Display Driver Integration (TDDI) ICs. Optimize ESD protection scheme to provide better protection against system level tests.

II. Motivation

- Standard component level ESD testing is insufficient to predict the outcome of system level ESD performance in the case of TDDI ICs.
- A TDDI IC that meets JEDEC specifications will not necessarily meet system level IEC specifications due to the unique constraints of an assembled TDDI liquid crystal display.

III. ESD Overview

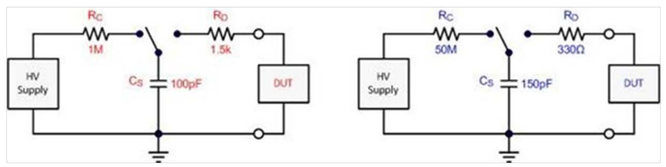
ESD Testing

Component Level Testing

- Simulated discharge through skin of an inadequately grounded person
- Intended to protect a component during manufacturing processes
- Typical Component level testing is done to JEDEC Human Body Model (HBM) and Charged Device Model (CDM)

System Level Testing

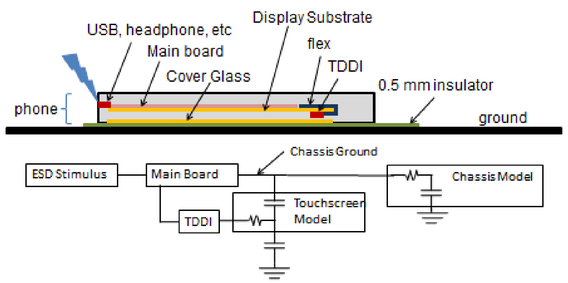
- Simulated discharge of an ungrounded person through a metal object (such as a tool or a connector)
- Intended to protect the end item from normal usage ESD stress
- System level testing is done to IEC 61000-4-2 standards



Comparison of ESD generator models for HBM and IEC

Image Texas Instruments : http://e2e.ti.com/support/interface/industrial_interface/f/142/t/359524

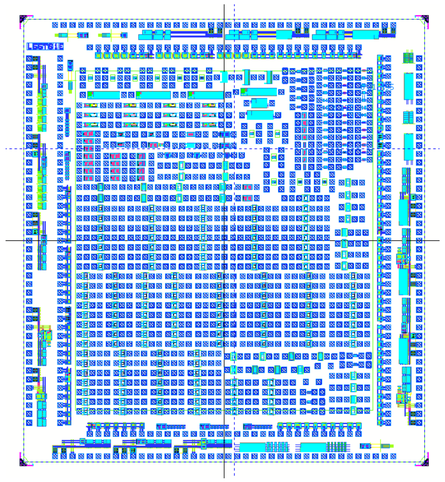
Display Side Down IEC Testing



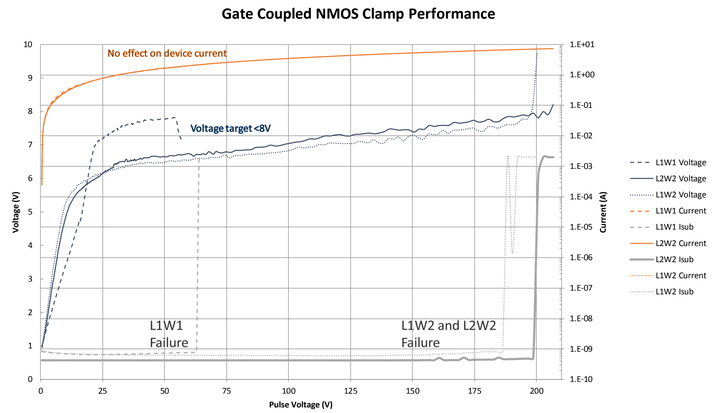
In this configuration, the display has a large capacitance to ground which can put the TDDI IC directly in a discharge path, causing both hard and soft failures.

IV. Experimental Results

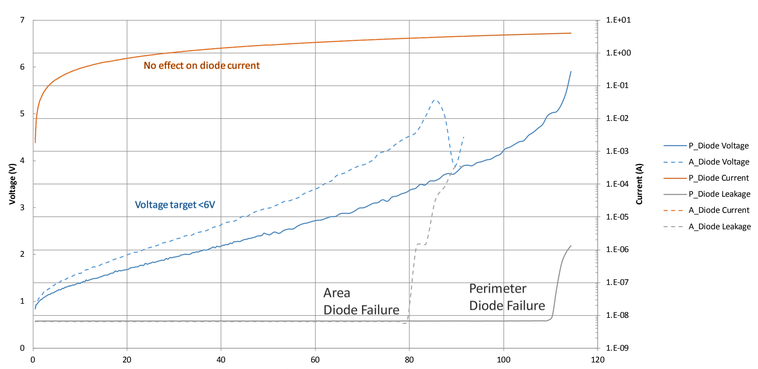
ESD Test Chip



I-V Response of Primary ESD Devices under Transmission Line Pulse (TLP) Stimulus

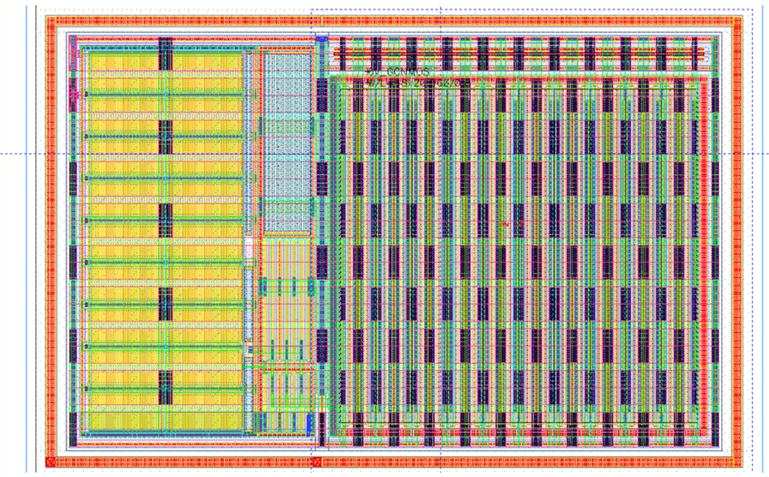


Perimeter Diode vs Area Diode

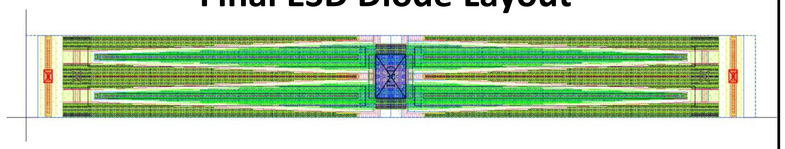


Results (con't)

Final Gate Coupled NMOS Layout



Final ESD Diode Layout



V. Conclusions

Initial experiments show that system level ESD stress is better modeled using a TLP stimulus.

Future work will be needed to evaluate the ability of TLP stimulus to predict the IC performance in system level ESD testing.

Additional test chips could develop multi-staged ESD protection to incorporate silicon controlled rectifiers, potentially reducing the cost impact of ESD protection.

Acknowledgements

- Synaptics Inc.
- Dr. Robert Pearson
- Dr. Dale Ewbank