Design, Fabrication, and Testing of a MEMS Peltier Cooler (TEC-Thermoelectric Cooler)

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***Abstract*—In this paper, a MEMS Peltier Cooler was designed, fabricated, and tested to prove TEC (Thermoelectric Coolers) can be created with a fabrication process. Design was done using Mentor Graphics IC Station software, fabrication was done using a custom process, and testing was done using built in temperature sensors to observe the temperature difference between each side.**

Keywords—MEMS; TEC; Peltier; cooler; thermoelectric

I. Introduction

A. Theory: Peltier Effect

THE Peltier Effect happens when two dissimilar semiconductors or metals are connected in series and a current is passed through them. As the electrons move through the materials they gain energy in the form of absorbed heat at the p-n junction and lose energy in the form of rejected heat at the n-p junction. The changes in energy are due to the different work functions/energy levels of different type semiconductors and metals. The Seebeck Coefficients shown in Fig.2 are caused from the different work functions of the material. (The Seebeck Effect is the opposite of the Peltier Effect and is the output voltage caused by two dissimilar materials that have a temperature difference at their junctions). P-type semiconductors have a positive Seebeck coefficient which means they get an increase in temperature per volt and n-type semiconductors and metals have a negative Seebeck coefficient which means they get a decrease in temperature per volt. The difference between the Seebeck coefficients of the two materials is an important parameter in determining the effectiveness of the TEC (Thermoelectric Coolers). Fig 1 shows the simplest form of a Peltier Cooler. Generally, the thermocouple in Fig. 1 is repeated many times in a TEC to increase the cooling effect.

Eqs. 1-11 represent the parameters that describe the TECs operation. The 3 important parts of the TEC are the Peltier effect, the joule heating of resistors, and thermal conduction. The Peltier effect is the first term of equations 1 and 6 (SIT_C) and it takes heat from the cool side and brings it to the hot side. The Seebeck coefficient S is combined effect of the Seebeck coefficients in both the materials used which is shown in equation 7. This is multiplied by the current and the cold side temperature. The second term in those equations is the joule heating of resistors ($\frac{I^2R_T}{2}$). If a current passes through any resistive material the resistor dissipates heat. This term is a net heating of the entire cooler device. R_T is the combined resistance of the cooler which is the pillars of material in series (Eq. 8) and the geometry of each pillar multiplied by their sheet resistance ρ (Eq. 9). The last term of those equations is thermal conduction, which is the flow of heat from a hotter area to a colder area through a thermal path ($\frac{\Delta T}{R_{TEC}}$). This acts in opposition to the Peltier Effect and brings heat to the cold side. R_{TEC} is the thermal resistance path back through the cooler shown in Eqs. 3 and 4. The coefficient of thermal conduction is δ in Eq. 4 which is important to look at when selecting materials when designing a TEC. In order for a TEC to work, the Peltier Effect must be greater than the joule heating of the device and the thermal conduction from one side to the other. The thermal conduction will increase with an increase in the temperature difference of the cooler which results in a limiting factor to the Peltier effect, a max temperature difference achievable.

The TEC's operation is predicted using Eq. 11 to observe the temperature change in the device when power is added to one side and removed from the other side. This created Fig.3 which used expected parameters achieved after fabricating the device to estimate the results that were likely to be obtained. Eq. 11 is the coefficient of performance and is a common measurement for TEC's comparing the input power to the output power flow.

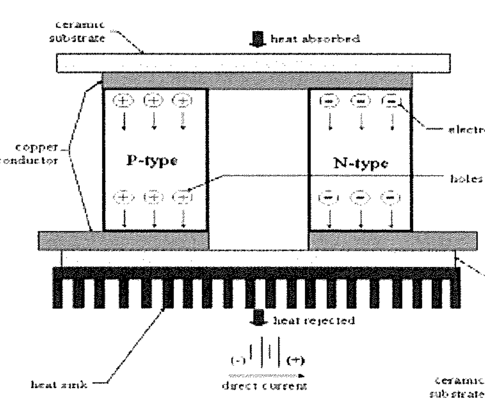

Fig. 1. Peltier Cooler Diagram from Mohammad Al-Naby, pg 2

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B. Equations

(1.) $Q_H = SIT_C + \frac{I^2 R_T}{2} - \frac{\Delta T}{R_{TEC}}$

(2.) $\Delta T = T_H - T_C$

(3.) $R_{TEC}(Total) = R_{TEC1} + R_{TEC2}$

(4.) $R_{TEC} = \frac{\delta}{K_m N_C}$

(5.) $\delta = \frac{L}{Wt}$

(6.) $Q_C = -SIT_C + \frac{I^2 R_T}{2} + \frac{\Delta T}{R_{TEC}}$

(7.) $S = 2N_C |S_1 - S_2|$

(8.) $R_T = N_c(R_1 + R_2)$

(9.) $R = \frac{\rho L}{tW}$

(10.) $Temp\ Change = \frac{Q_C}{MC}$

(11.) $COP = \varphi = \frac{Q_C}{P_{IN}}$

Variable	Description
Q_H, Q_C	Power hot and cold side
T_H, T_C	Temp. hot and cold side
L,w,t	Length, width, thickness
S	Total Seebeck Coef.
S_1, S_2	Seebeck Coef. Of Materials
N_c	# of Couples
ρ	Resistivity
R_{TEC}	Thermal Path
K_m	Thermal Coefficient
M	Mass
C	Specific Heat
COP=φ	Coef. of Performance

Element	Symbol	Type	α (μV K⁻¹)	ρ (μΩ m)	λ (W m⁻¹ K⁻¹)
p-Si	Si	semiconductor	100–1000	10–500	≈150
p-Poly-Si	Si	semiconductor	100–500	10–1000	≈20–30
Antimony	Sb	metal	32	18.5	0.39
Iron	Fe	metal	13.4	0.086	72.4
Gold	Au	metal	0.1	0.023	314
Copper	Cu	metal	0	0.0172	398
Silver	Ag	metal	−0.2	0.016	418
Aluminium	Al	metal	−3.2	0.028	238
Platinum	Pt	metal	−5.9	0.0981	71
Cobalt	Co	metal	−20.1	0.0557	69
Nickel	Ni	metal	−20.4	0.0614	60.5
Bismuth	Bi	metal	−72.8	1.1	8.1
n-Si	Si	semiconductor	−100 to −1000	10–500	≈150
n-Poly-Si	Si	semiconductor	−100 to −500	10–1000	≈20–30

Fig. 2. Material Parameters from ref. [1].

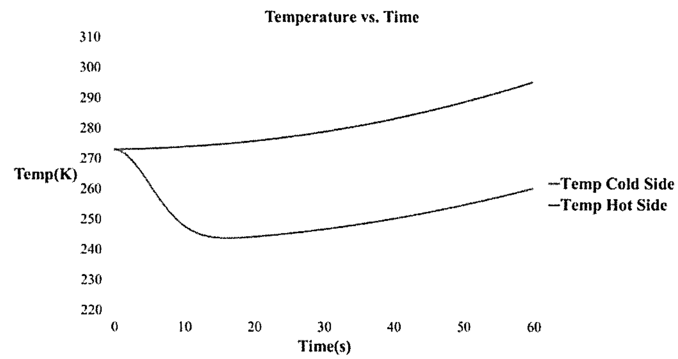

Fig. 3. Theoretical Calcution for Temperature Change in a TEC with 25 Couples of Aluminmum and P-Poly Silicon Pillars at 5V

C. Theory:Resitive Temperature Sensors

Polysilicon resistors change resistance based on the temperature of the resistive material. The temperature changes the mobility of the active particles in the polysilicon. An increase in temperature decreases the mobility which in turn increases the resistance. The polysilicon resistor on the hot side of the TEC should increase resistance and the polysilicon resistor on the cold side should decrease in resistance.

II. Design and Fabrication

A. Design

Two materials are needed to create the Peltier Effect in the cooler. These materials must have a large difference in Seebeck coefficients, low resistance, and a low thermal conduction. Looking at these parameters and the materials available in the Semiconductor Microsystems Fabrication Laboratory (SMFL) at RIT, aluminum and p-type polysilicon was chosen. The TEC fabricated consists of 25 thermocouples made up of these materials. Each thermocouple is laid out with an aluminum resistor on top of a layer of insulating oxide on top of the p-type poly silicon resistor on top of another insulating oxide layer. The couples are laid out in series and connected by a contact cut through overlapping sections. The main part of the pillars is 60μmX200μm. The contact cuts are 20μmX20μm. Two temperature sensors are placed on each side of the material to monitor the temperature change. Six 500μmX500μm bond pads are used, four for the temperature sensors and two for the TEC. Fig. 4-6 show screen shots of the

mask design, the aluminum layer is blue, the contact cuts are black , and the P-type poly silicon later is red.

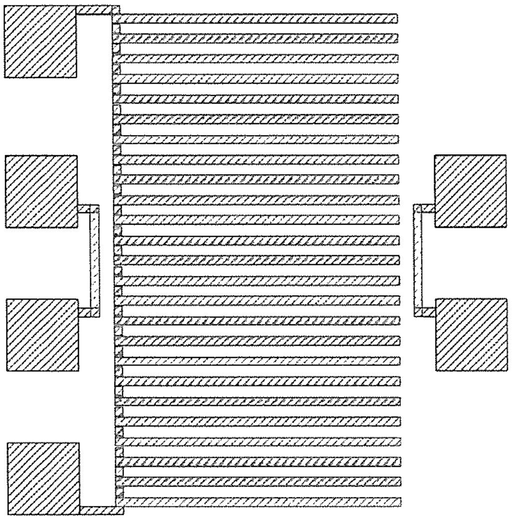

Fig. 4. Mask Design- Total Device

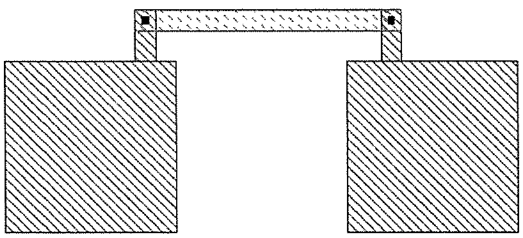

Fig. 5. Mask Design- Temperature Sensor

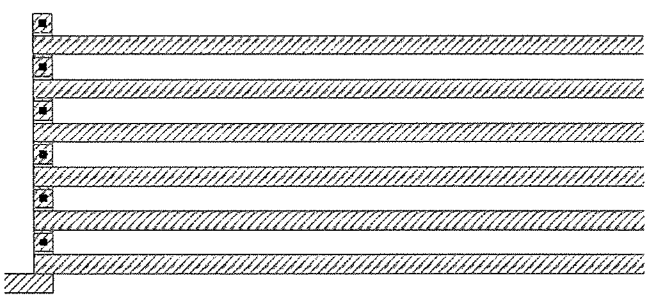

Fig. 6. Mask Design- Contect Cuts

B. Fabrication

The fabrication process was divided into 4 levels of photo. The first level of photo was the zero etch which etched into the silicon to create the alignment marks to align the different layers. Then, about 500 nm of polysilicon was deposited on top of an oxide grown on the silicon wafer. The poly silicon was implanted with boron to create a p-type poly silicon material with a desired sheet resistance of 35Ωper sq. The next level lithography defined the mask to dry etch the polysilicon resistors. The polysilicon was put through a thermal process to activate the boron in the silicon and grow an insulating oxide on top of it. The third lithographic level was performed to etch the contact cuts. The oxide on top of the poly silicon was thoroughly etched to make sure none was left to create an open circuit. Aluminum was then sputtered on and the fourth level of photo etched the aluminum resistors. The device was then ready to be tested.

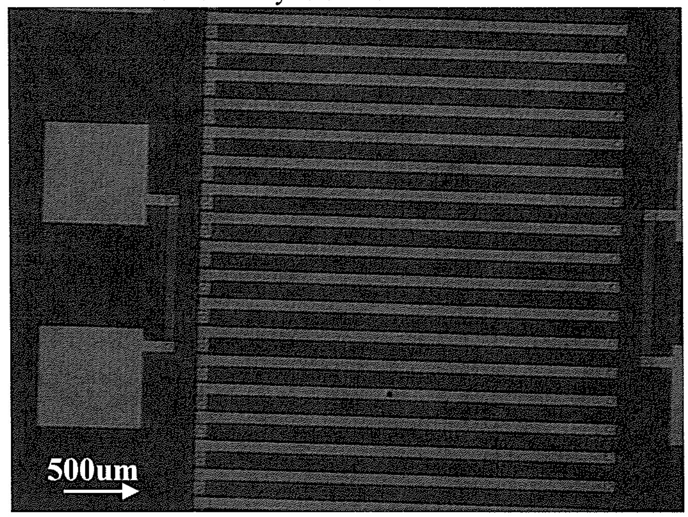

Fig. 7. Fabricated Peltier Cooler

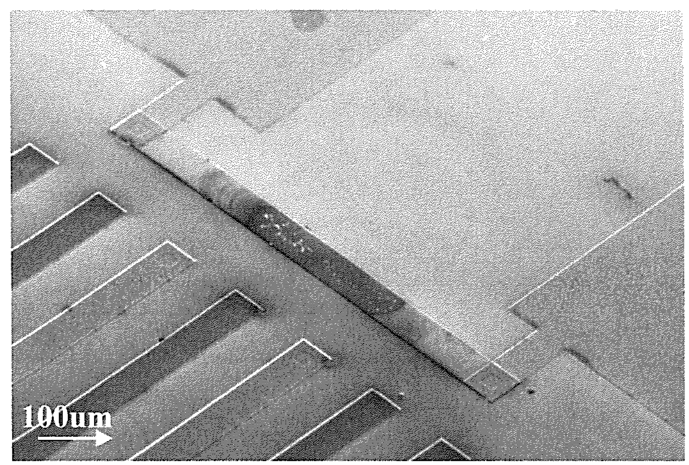

Fig. 8. SEM Picture of Peltier Cooler

III. Testing/Analysis

A. Results

The most important factor to obtain a working Peltier Cooler is the current drive. The current has to be a high enough to create a large enough Peltier Effect while also low enough to keep the joule heating of resistors (an I^2 term) at a minimum. The correct current drive needed polysilicon resistors with a low resistance. The total resistance of the cooler should have been around 30 KΩ, but due to problems in the implant, two of the wafers fabricated came out to be a factor of ten higher in resistance. According to the theoretical results this would allow for a small change in temperature, but

this was too small of a change to observe with the temperature sensors. The sensitivity of the multimeter measuring the resistances was too low to see this change.

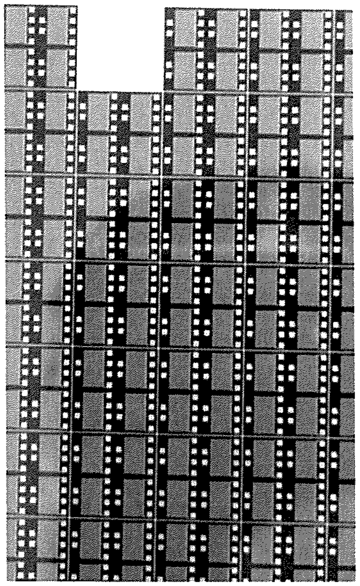

Fig. 9. Fabricated Devices on Silicon Wafer

One wafer appeared to have the resistances needed to obtain some working coolers. But, this wafer experienced another problem in the process during the contact cut etch. The oxide that was used as an insulator beween the poly silicon resistors and the substrate was overetched shorting the poly silicon resistors to the substarte. As a result there was a resistance between all the pads even though they should have been electrically isolated. Fig. 10 and Fig. 11 show the over etch problem.

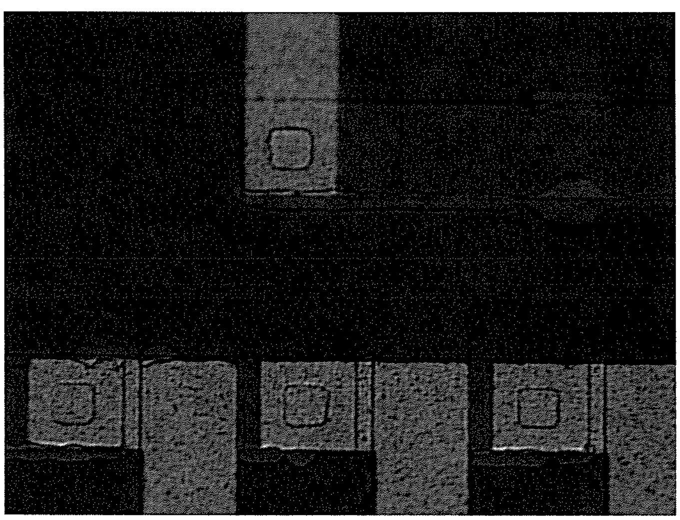

Fig. 10. Microscope Picture of Overetch

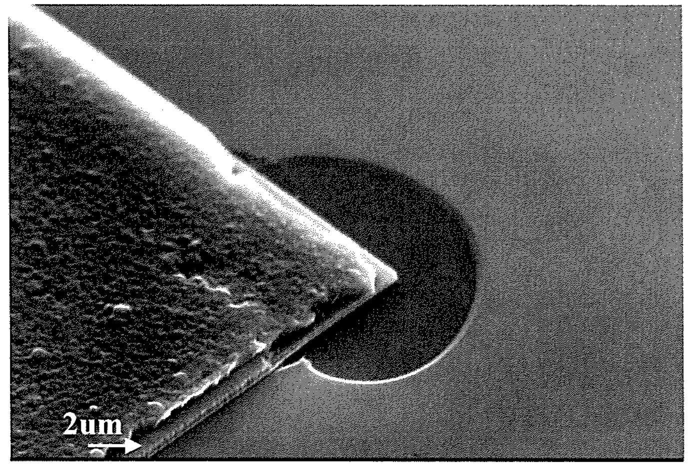

Fig. 11. SEM Picture of Overetch

IV. Conclusion

The Peltier Cooler did not work, but there were important lessons learned in its fabrication. The most important step was the implant and the annealing of the p-type poly silicon resistors. These are the main contributor to the high resistance. The next mask design should have some test structures to look at the sheet resistance of the poly silicon and make sure the high dose and long implant was enough to achieve a low enough sheet resistance. This would save process time and help achieve a correct implant recipe. Another problem was the thickness of the insulating oxide. The contact cut etch needs to be significantly long to make sure there is no open circuits because of left over oxide. Therefore, the insulating oxide needs to have a larger thickness to avoid etching all the way through to the oxide shorting out the device. Repeating this process with thicker oxides and the correct implant recipe should theoretically achieve the desired goal.

V. Appendix

A. Fabrication Process

5 6" silicon wafers that have been polished and clean were used in this process.

1. Photo Level 0- Zero Etch
2. Etch alignment marks for the ASML into the silicon.
3. Remove resist and RCA clean.
4. Grow 1000A of silicon oxide.
5. Deposit 5000A of poly silicon.
6. Implant polysilicon with Boron to create p-type poly silicon with a sheet resistance of 35ohms/sq
7. Photo Level 1- Poly Silicon
8. Etch poly silicon.
9. Remove resist and RCA clean.
10. Anneal poly silicon and simultaneously grow 1000A of oxide.
11. Photo Level 2-Contact Cut
12. Etch oxide with 10:1 BOE for 10min. Stop on poly silicon.
13. Remove resist and RCA clean.
14. Deposit 5000A of aluminum.

15. Photo 3-Metal
16. Etch aluminum.
17. Remove resist.
18. Test.

VI. ACKNOWLEDGEMENTS

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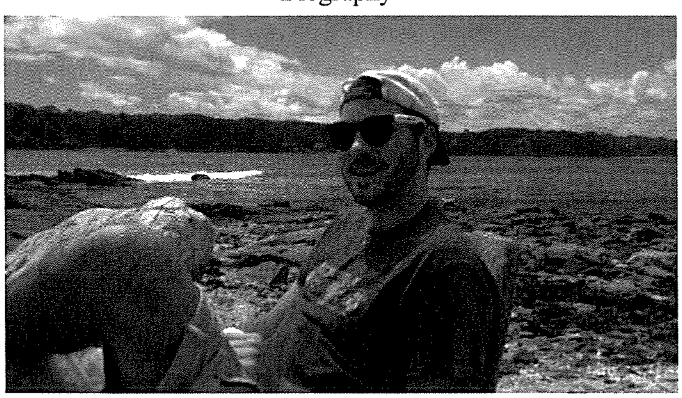
Biography



My name is Brendan Merna, I am from Ogdensburg, NY, and I am a 5th year Electrically Engineering student in the BS/MS program here at RIT.I have specialized my graduate focus into MEMS. I have learned a great deal about the processing that goes into them and the external circuitry used to extract their signals. Outside of school my hobbies and interests include beach volleyball, golf, astronomy, and philosophy. I hope to gain a job in inudstry working with MEMS devices and eventually create my own company in this field.