"Black Silicon" by RIE for Photovoltaics

Jacob D. Lana

Abstract— **Silicon-based solar cell technology continues to dominate the solar cell market making efficiency improvements to this class of devices sought after. A RIE process for creating "Black Silicon (BS)" was developed and integrated into a mono-crystalline-Si solar cell process. Solar cells with BS exhibited an R_{avg} of 3.8% compared to 38.4% for solar cells with no anti-reflection apparatus (λ = 360-750 nm). BS solar cells were also found to have an *EQE* 16.4% higher than that of the control (λ = 360-1100nm). On average J_{sc} and *FF* was higher for the BS solar cells as compared to the control however solar cell performance comparisons were corrupted by manufacturing defects resulting in poor diode characteristics across all fabricated devices.**

Index Terms— **anti-reflection, Black Silicon, *EQE*, *FF*, J_{sc}**

I. Introduction

As the global demand for energy increases – exceeding 15TW in 2011 [1] – renewable energy sources become more desirable. Imminent threats to environmental stability and the depletion of traditional energy sources, namely fossil fuels, have spurred the development of alternative energy sources such as solar technology. By directly converting radiant energy from the sun into electrical energy, solar cells take advantage of a virtually infinite source of power without possessing many of the disadvantages of conventional energy production ("grid" energy).

While solar technology has many holistic advantages over traditional energy production, solar cells produced in large volumes exhibit efficiencies around 20% for silicon-based solar technology. At this level of efficiency, the cost of producing energy using solar cells is greater than that of traditional means. While it is a subject of debate, solar energy costs are projected to converge with grid costs as solar energy costs trend downward and grid costs trend upward. Silicon-based technologies dominate the solar cell market making efficiency improvements to these devices very impactful, driving solar energy costs further downward.

Much of the efficiency loss in solar cells is due to the reflection of light incident upon the surface of the device. In being reflected, the light cannot contribute to the production of charge carriers which ultimately produce electrical power. One avenue being pursued to increase the efficiency of Si solar cells is to alter the surface as to absorb more photons. One method of achieving a high rate of absorption is to texture the surface by way of reactive ion etching (RIE). Under certain etching conditions, the Si can be textured in such a way that it creates what is referred to as Black Silicon (BS) [2]. The Si is referred to as being "black" because of its dark appearance due to its low reflectivity over the visible light spectrum.

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II. Theory

A. Power generation is solar cells

The most basic form of a Si solar cell is a single p-n junction (photodiode). The energy of photons which are incident to the diode can be absorbed by the Si crystal lattice if the energy of the photon is equal to or greater than the band gap energy of the Si lattice (E_g).

Under short-circuit conditions the current in the photodiode is equal to the photo-generated current (photocurrent) and is denoted as I_{sc}, or as the current density J_{sc} when normalized by the area of the solar cell. As the load of the external circuitry connecting the two regions of the diode increases, the voltage across the load begins to forward bias the diode creating a current which opposes the photogenerated current. The voltage at which the forward biased diode current begins to overcome the photogenerated current is known as the open circuit voltage (V_{oc}).

By way of the theory discussed above, solar cell efficiency can be increased by increasing the amount of absorbed photons with energies greater than E_g. Doing so increases I_{sc}, V_{oc}, as well as other metrics which relate to the efficiency of solar cells such as fill factor (*FF*) as expressed in (1). I_{sc} is often expressed as the current density J_{sc} to normalize the current to solar cell area. V_{mp} and J_{mp} are the voltage and current density at which maximum power is generated, respectively. The product of I_{mp} and V_{mp} is the maximum power output of the cell. Parasitic effects such as shunt resistance (R_{sh}) and series resistance (R_s) alter the I_{sc}-V_{oc} curve of the photodiode such that the maximum power P_{max} is decreased. In essence, the presence of parasitic resistances decreases the *FF* which is a measure of how close the solar cell is to being an ideal diode with infinite shunt resistance and zero series resistance where V_{mp} and I_{mp} would be equal to V_{oc} and I_{sc}, respectively. See Fig. 1 for an illustration of this concept. Series resistance is indicative of poor solar cell design, where the resistance of the body of the diode restricts current flow. Carriers must flow through the body to reach the external circuitry which allows photocurrent to generate

power. Shunt resistance is indicative of manufacturing defects which provide leakage paths which photocurrent will be lost to instead of flowing through the external circuitry to power a load.

$$FF = \left(\frac{J_M \cdot V_M}{J_{SC} \cdot V_{OC}} \right) \quad (1)$$

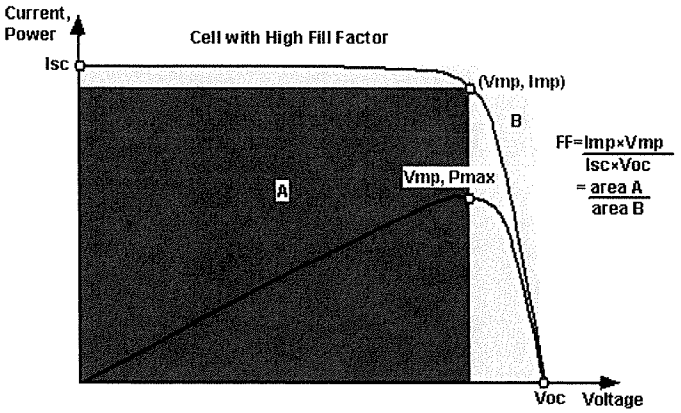

Fig. 1. Solar cell I_{sc}-V_{oc} curve. Appended to the graph is the power output of the cell and an illustration of the *FF* [3].

Increasing the amount of light absorbed by the solar cell will increase the photogenerated current (I_{sc}) and will increase the *FF* and P_{max} as a consequence – all other things constant.

Surface recombination can play a significant role in determining the efficiency of a solar cell, as recombination eliminates electron-hole pairs needed to create current. Passivating the surface can reduce the rate of recombination. The unpassivated surface of a solar cell contains a large number of energy traps because in effect the surface is a defect in the crystalline structure of the semiconductor. Passivating the surface is the process of eliminating dangling bonds at the surface, in turn reducing the amount of energy traps and can be done with thermal oxidation.

B. *Black Si by RIE*

A SF_6/O_2 based RIE process exists which creates a textured Si surface suitable for decreasing the reflection of a Si solar cell. The process takes advantage of competing etching and passivation mechanisms [4]. Fluorine and oxygen radicals created by dissociative ionization within the plasma act to etch and passivate the silicon, respectively. Native oxide and particulates on the surface of the Si provide micro-masks. The regions between micro-masks are anisotropically etched creating needle-like structures beneath the micro-masks. The sidewalls of the needle structures remain passivated by silicon oxyflouride preventing etching by fluorine radicals. Using a moderately low process pressure will result in a high degree of ion vertical directionality. Due to the dependence of sputter yield on the angle of incident ions, the passivation layer at the horizontal bottom of the trenches is removed while the vertical sidewall passivation layer – resistant to spontaneous chemical etching – remains largely intact. The needles continue to become deeper as the passivation layer is removed by sputtering at the bottom of the trenches exposing the Si to F radicals which etch the Si by spontaneous chemical etching.

By altering the relative flow of SF_6 and O_2 into the chamber, the degree of passivation can be adjusted in turn altering the profile of the Si needles.

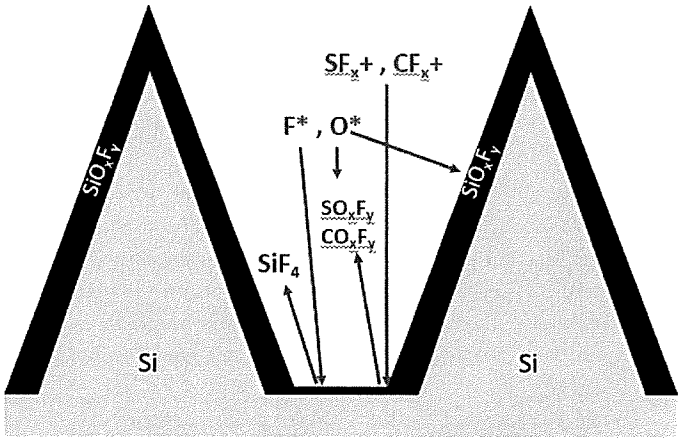

Fig. 3. Illustration of competing etching and sidewall passivation mechanisms in BS RIE process.

The BS RIE process does not require any lithographic steps, as the micro-masks are created by native oxide, dust, and passivation which occurs during the process [4]. Typically, BS-producing regimes are found at moderately low pressures due to the need for a high degree of ion directionality.

C. *BS Optical Properties*

The Si needles create low a reflection condition by way of two mechanisms depending on the dimensions of the features relative the wavelength of the incident light. When the periodicity or *pitch* of the features is larger than the wavelength of the incident light, geometric light trapping causes reflected light to be directed towards adjacent structures. This mechanism increases light absorption by allowing the light to interact with the surface multiple times, where each interaction results in a portion of the light being absorbed. When the pitch of the structures is on the order of the wavelength of the incident light or less, the surface effectively takes on a graded index of refraction (n). Abrupt changes in n cause reflection as expressed in the Fresnel Equation (2) for small angles of incidence.

$$R = \left| \frac{n_1 - n_2}{n_1 + n_2} \right|^2 \quad (2)$$

Using (2) it can be shown that R can be decreased by providing multiple interfaces which discretely increment n from n_1 (air) to n_2 (Si) or by a continuous gradient of n from n_1 to n_2 (graded index of refraction).

III. Experimental Setup

The basic solar cell process used as the control in this experiment is described in detail in the Appendix. In order to create BS solar cells, processing steps were inserted into the basic process as indicated in the process flow in the Appendix.

Multiple square solar cells of varying area were fabricated on a single substrate by isolating each device with a field oxide (3700 Å as-grown) as seen in Figure 5. The design was intended to be implemented on a 100 mm substrate, however a 150 mm substrate was used in this experiment as explained in the Discussion of Results section. The field oxide was removed on the perimeter of the 150 mm substrate as to expose as much Si as possible in order to mitigate the loading effect as described in the Discussion of Results section.

The BS samples were created by inserting the BS RIE process, as specified in the Appendix, prior to ion implantation. Excluding the insertion of the BS RIE process, the control sample and the BS samples underwent identical processing.

When necessary, the thickness of certain films were measured in order to determine the duration of etch processes based on the etch rate of the process. Film thicknesses were also monitored throughout the process to ensure adequate ion implant masking in the field regions.

Fabrication of the devices yielded one control substrate and two substrates which had undergone the BS RIE process prior to ion implantation. Only one of the BS samples was analyzed and reported in the Discussion of Results section for the sake of simplicity. Each substrate contained 10 solar cells of varying area and metallization patterns, allowing for a moderate volume of data to be collected.

Each device was measured with no illumination in order to extract the diode characteristics using a HP 4145 parameter analyzer with a dark box. Each device was also measured under fluorescent illumination using the parameter analyzer to extract J_{sc}-I_{sc} curves. Devices were measured for external quantum efficiency (EQE) using a Newport QE-PV-SI Measurement Kit. SEM images were acquired from tools available at the Rochester Institute of Technology and the University of Rochester in order to study the feature profiles.

IV. Discussion of Results

A. BS RIE Process and Optical Properties

Using the baseline RIE process determined by [2] to result in a rough surface, BS with very low reflection (2%) over the visible spectrum when a 100 mm bare Si substrate was acheived while mounted on a 150 mm Si carrier. This amount of Si provided a sufficient macroscopic Si load which was found to be critical for achieving needles of high pitch and sufficient depth. This dependence on Si loading was found to be an important parameter in determining the feature profile as alluded by [4]. When an identical 100 mm Si substrate was mounted on an Al carrier, the critical Si load required to create uniform feature profiles over the entire area of the substrate was not met resulting in inadequate (large pitch) features near the edge of the substrate. However, adequate feature profiles were achieved in the center of the substrate under these conditions. It is hypothesized that since the center region of the substrate was effectively surrounded by Si while the edge regions were only partially surrounded by Si, the localized Si loading in each region was above the critical value in the center but not at the edge.

The cause of the Si *loading effect* was investigated on small pieces (1/4 wedges of a 100 mm substrate) of Si where the loading effect could be exaggerated. When a small piece was etched on an Al carrier, the formation of Si needles was sparse. SEM images of the feature profiles under these conditions indicated that the degree of sidewall passivation was substantially decreased. This resulted in isotropic etching, hindering the formation of high aspect ratio features. Varying the flow of oxygen to 50%, 130%, and 150% of the nominal value of the BS RIE process resulted in the features seen in Fig. 4. With an increase in the flow of O_2, sidewall passivation was restored along with anisotropic etching. Varying power by the same proportions did not result in as much of an effect of the feature profiles. These results suggest that the Si loading effect is caused by the relative proportion of exposed Si on the substrate to the amount of SF_6 and/or O_2 in the system. When a critical amount of Si is not present, F radicals saturate the system leading to isotropic etching overwhelming the passivation mechanism. It was found that to some extent this could be counteracted by increasing the concentration of passivation-enabling O radicals. However, sufficient levels of passivation were still not achieved at the outermost regions of the Si pieces. As the O_2 flow was increased above 130% of the nominal value, the passivation mechanism dominated in the center of the pieces while the edges still exhibited isotropic etching.

Since anisotropic etching could only be partially restored over the area of the substrate when the macroscopic Si loading was less than that of a 150 mm substrate, using a 150 mm substrate for the fabrication of the solar cells was determined to be the best option if small pitch features of adequate depth were to be achieved across the entire cell.

It was observed that the device substrates which underwent the BS RIE process under nominal conditions exhibited reduced levels of blackening near the edge of the substrate in the load-correction region (Fig. 5). This effect was also observed in the emitter regions of the devices which were nearest the edge of the substrate. This effect can possibly be understood in light of the loading effect discussed above. Since the field oxide contains less Si atoms to react with F radicals than an equivalent area of Si, it effectively creates less of a Si load than if the area had been bare Si. The result is that the minimum Si load requirement is strained in areas near the edge and surrounded by oxide, allowing the loading effect to emerge. The presence of a backside oxide during the BS RIE process for the fabricated solar cells may have also played

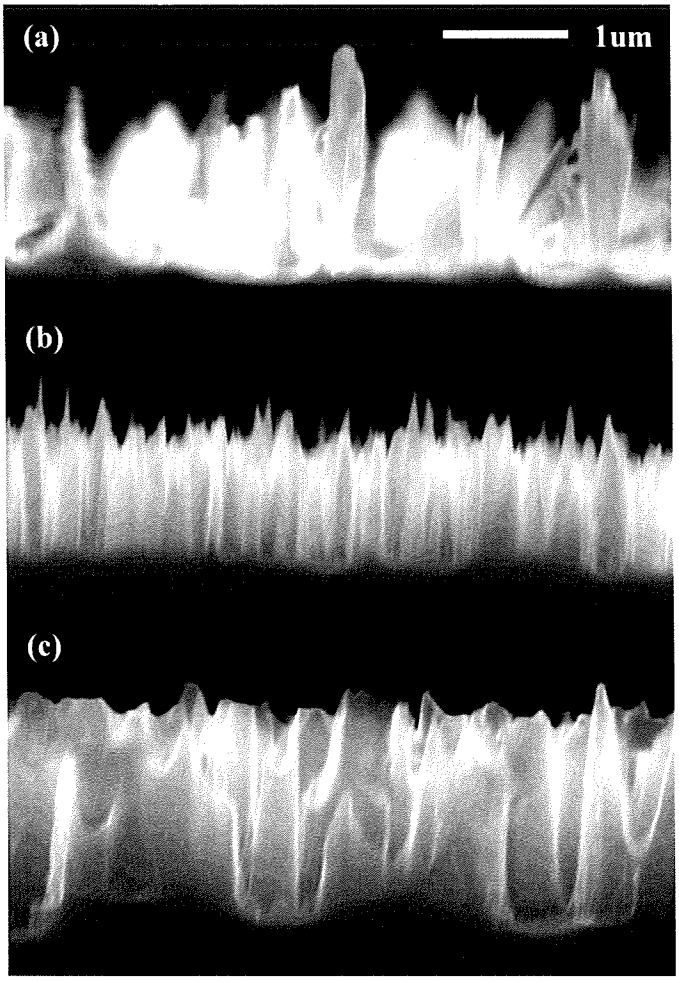

Fig. 4. Feature profiles obtained on Si pieces with O_2 flows of (a) 50% (b) 130% and (c) 150% of the nominal value (10 sccm).

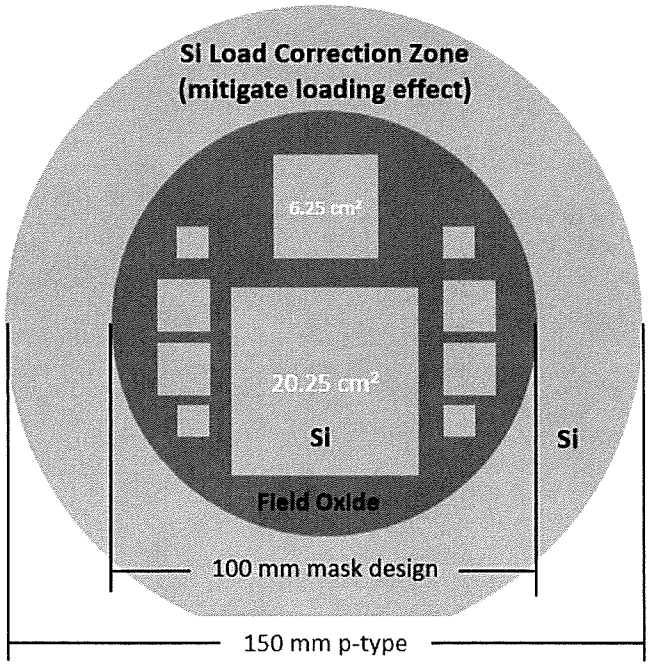

Fig. 5. Design of the solar cell.

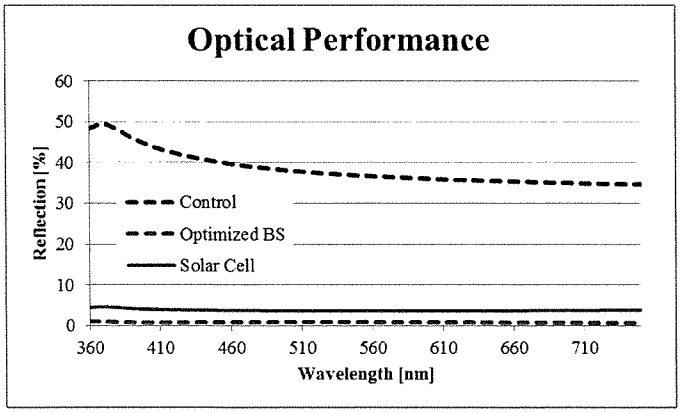

Fig. 6. Plot of reflectivity comparing control device, optimized BS, and fabricated solar cell with Al contacts.

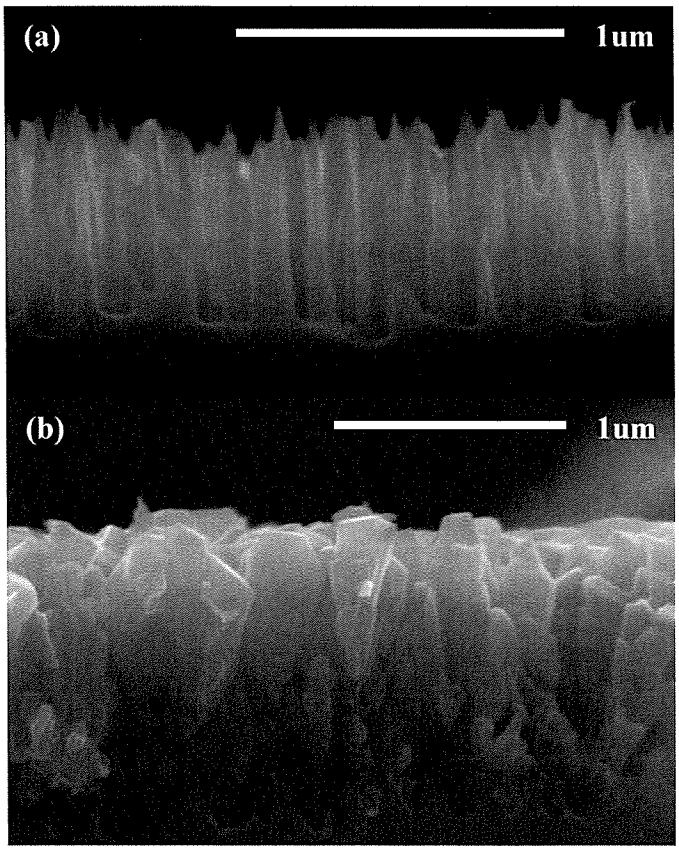

Fig. 7. (a) Final BS structures of fabricated solar cells. (b) Al contact on BS structures.

a role in affecting the uniformity of the etch by altering the coupling of the RF power to the substrate. This theory was not explored independent of other factors.

In similar fashion to the Si loading effect, the presence of photoresist was found to prohibit the formation of desirable features. Here it is theorized that the carbon present organic photoresist scavenges O radicals reducing the amount of O radicals which could contribute to passivation.

The reflectivity of fabricated solar cells exhibited a marked increase as compared to the optimized BS. These results are plotted in Fig. 6. The higher reflectance observed in the fabricated solar cells can be partially attributed to the presence of Al contacts. Wet etch and thermal oxidation processes may

have also had an effect on the final profiles of the features. Due to a limited number of samples, the structures could not be cross-sectioned and imaged at each stage of the solar cell processing. Even with optical performance degradation due to solar cell processing, the BS solar cells exhibit much less reflectivity (R_{avg} = 3.8%) as compared to the control which have only the passivation oxide (250 Å) on the surface of the Si (R_{avg} = 38.4%).

The relatively high reflectivity of the control device in the UV range is due to a sharp increase in the index of refraction of Si at UV wavelengths. The low reflectivity of BS relies on a graded index of refraction, making it effective even for UV light, eliminating the sharp increase at this range.

B. BS Solar Cell Performance

Both the BS and control devices which were fabricated exhibited poor diode characteristics. The deviation of the fabricated diodes from an ideal diode are primarily attributed to a low shunt resistance R_{sh}. The effect of the shunt resistance is most evident when plotting the dark diode *I-V* or *J-V* curve of the photodiodes. The *J-V* curve of a 0.75 cm x 0.75 cm device and 4.5 cm x 4.5 cm device and has been plotted in Fig. 8a and Fig 8b, respectively, for the control substrate and a BS substrate. For most devices the BS substrates approached ideality more so than the control substrate. Decreasing shunt resistance was observed with increasing device area and perimeter. Why the BS substrates were typically closer to ideality remains unexplained.

Since the diodes were compromised by such variation, a comparison of J_{sc}-V_{oc} curves for the control and BS cells was largely inconclusive due to the impact of diode performance on solar cell performance. Plotting the illuminated J_{sc}-V_{oc} curves in Fig. 9 for the same devices seen in Fig. 8 it is seen that the BS solar cells exhibited higher J_{sc} and V_{oc} than the control cell. The higher performance of the BS cells is most likely due to the confounded effects of the more ideal diode characteristics and the increase in light absorption.

In an attempt to separate these effects, the EQE of the cells was measured. This method was chosen because EQE measurements are executed under short circuit conditions, minimizing the effects of low R_{sh}. Fig. 10 illustrates that the average EQE of the BS cells was on average higher than that of the control cells at 66.9% and 50.5%, respectively. EQE is shown for the 4.5 cm x 4.5 cm cell in Fig. 10. The EQE of the control cell only surpasses the EQE of the BS cell at wavelengths below 500 nm. It may be possible that the efficiency loss due to surface recombination in the BS device overwhelms the efficiency gain due to increased light absorption at short wavelengths which absorb close to the surface. These results suggest that a more effective passivation method is required in order to compensate for the large increase in surface area associated with incorporating BS into a solar cell design.

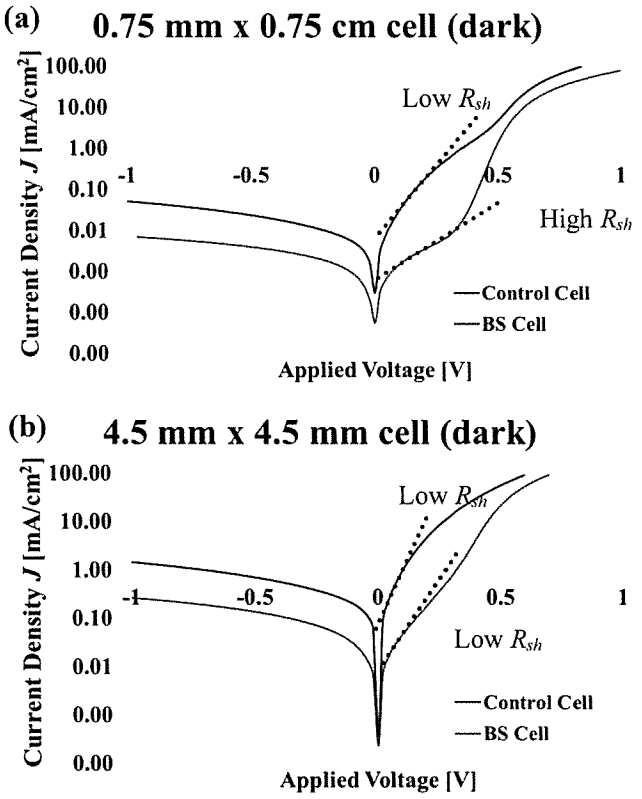

Fig. 8. Dark diode *J-V* curves for (a) 0.75 mm x 0.75 mm and (b) 4.5 mm x 4.5 mm devices.

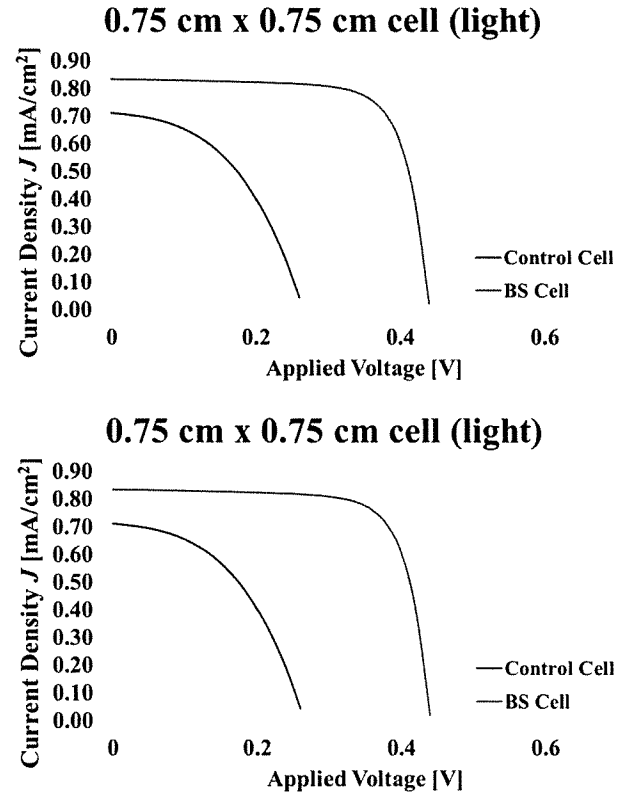

Fig. 9. Illuminated diode *J-V* curves for (a) 0.75 mm x 0.75 mm and (b) 4.5 mm x 4.5 mm devices.

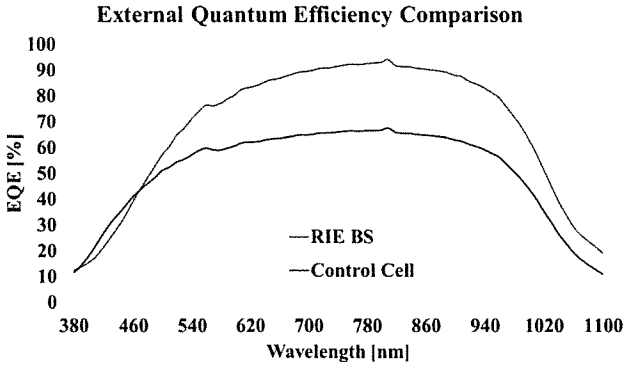

Fig. 10. External quantum efficiency comparison of control and BS cells.

APPENDIX

Solar Cell Process Flow

The solar cells were fabricated on 150 mm PRIME p-type solar cells with a sheet resistivity of 5-15 Ω-cm. The basic process flow is as follows, with the BS solar cell process steps inserted as indicated with an asterisk. Recipe names refer to recipes available on tools in the RIT SMFL.

1. RCA clean substrate.
2. Grow 3700 Å of oxide using steam oxidation. Recipe 341 Bruce Furnace Tube 1.
3. Coat substrate with ~1 um of HPR504 resist.
4. Expose substrate with level 1 emitter mask to define emitter regions.
5. Mask device region with 100 mm substrate and flood expose perimeter of device substrate.
6. Remove remaining resist in perimeter of device substrate using Acetone.
7. Develop using CEE Developer, recipe 1.
8. Etch oxide to ~1000 Å using Trion etcher, recipe PVEmit.
9. Etch remaining oxide in emitter regions, 10:1 BOE.
10. *Remove photoresist from substrate using Trion etcher, (300 mTorr, 150 W, 20 sccm O_2).
11. *BS RIE process in Drytek Quad (after 10 min. O_2 clean and 5 min. precondition etch using BS RIE process parameters).
12. Ion implant P, 1E15 dose, 65keV.
13. Remove photoresist in GaSonics asher, recipe FF (control substrate).
14. RCA clean substrate
15. Anneal, drive in, passivate. Recipe 21 Bruce Furnace Tube 1.
16. Coat substrates with ~1.5 um AZ 1518 photoresist. Expose substrates with dark-field contact mask, align to emitters.
17. Develop using CEE Developer, recipe 1.
18. Deposit ~2700 Å AlSi using CVC evaporator (2 pellets).
19. Lift off in Acetone bath using Ultrasonic bench. Place in clean Acetone and contunie lift off process when Acetone bath accrues large amount of AlSi debris. IPA dry.
20. Spin-rinse-dry.
21. Coat substrate with HPR504 photoresist.
22. Remove backside oxide with 5.2:1 BOE.
23. Deposit ~4000-5000 Å AlSi on backside of substrate in CHA Flash Evaporator.
24. Remove photoresist with Acetone, IPA dry.
25. Spin-rinse-dry.
26. Sinter, recipe 204 Bruce Furnace Tube 2.

BS RIE process

Drytek Quad chamber 1.
Power = 155 W (to obtain 140 W)
Pressure = 140 mTorr
Time = 5 min.
SF_6 Flow = 30 sccm
O_2 Flow = 10 sccm
CHF_3 Flow = 10 sccm
DC Bias should read ~55 V.

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Development, Fabrication, and Characterization of a Vertical-Diffused MOS Process for Power RF Applications

Abstract—**The objective of this experiment was to design, simulate and test a VDMOS device with a breakdown voltage of 150 V. Power MOSFETS are transistors capable of handling voltages up to 500 V. High power transistors have a wide range of applications ranging from motor control, power supplies and DC converters. A Vertical Diffused MOSFET (VDMOS) has many advantages over Bipolar Junction Transistors such as an IGBT because of their faster switching capabilities .This is due to the MOSFET being a unipolar device which mitigates minority charge carrier storage. Vertical Diffused MOSFETs are an attractive choice for high power device applications due to their large gate impedance which simplifies the circuitry needed to bias the gate. The majority of the vertical channel length resides in the thickness of the wafer and allows larger depletion widths to reduce effects of punch through. In addition these devices are preferred over lateral devices because of their larger source area and reduced electric fields at the gate which minimize hot carrier effects. This project studies the effects of breakdown mechanism such as punch through, avalanche breakdown, and latch up. The breakdown voltage was found to be 9 volts due to punch through for the VDMOS devices.**

I. Introduction

Many obstacles arise when designing and fabricating power transistors. Effects such as punch through, avalanche breakdown and latch up are common breakdown mechanisms that are encountered for power devices. Punch through occurs when a PN junction is heavily reversed biased and as a result large depletion regions are created. If the source and drain depletion regions touch or are close enough, significant current can be drawn without any control over the gate. This is more likely to occur in smaller transistors with large reverse biased junctions. Vertical channels are much larger than lateral MOSFETS allowing depletion regions to extend further at the junction.

Electric fields must also be reduced to avoid Avalanche breakdown. Avalanche breakdown is another breakdown mechanism that occurs when a carrier experiences a high electric field colliding into other carriers repeatedly until significant current is drawn.

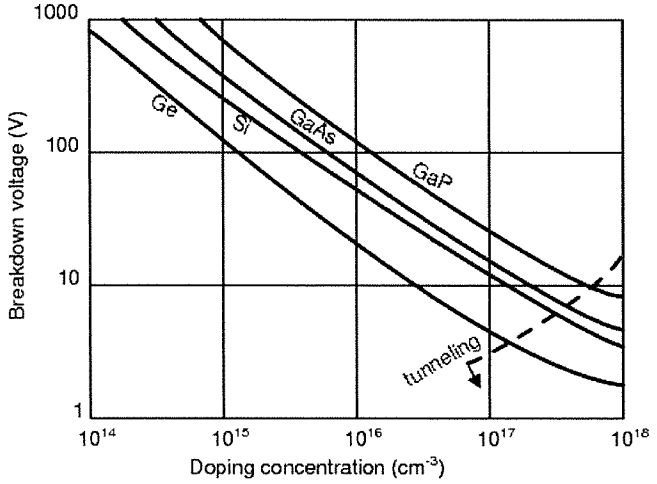
Latch up is observed when a parasitic BJT turns on within a MOSFET leading to improper control of the device and uncontrollable current gain. This phenomenon usually displays thyristor behavior with a negative differential resistance.

With lower doping regions the breakdown voltage is significantly increased however larger source drain resistance is observed. This inverse relationship indicates that a middle ground must be optimized to achieve desired results. An optimal design for a VDMOS device requires an epitaxial layer to obtain these low doping levels for higher breakdown voltages while the substrate will remain at higher doping levels to reduce the series drain resistance. Due to constraints and availability standard N type wafers with resistance between 1-10 ohms will be used. The thickness of the epitaxial layer must also be chosen to be large enough to withstand the depletion width. Figure 1 displays the doping concentration vs. breakdown voltage plot. The depletion width for PN junction can be modeled by Eq. 1. Using Eq. 1 the epitaxial thickness can be determined for a desired breakdown voltage. Eqs. 2 and 3 are utilized to find the optimal doping concentrations for a specific breakdown voltage.

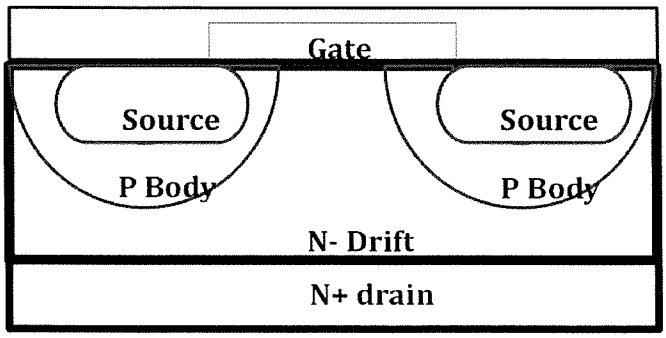
$$Wn = \sqrt{\frac{2\varepsilon 0 \varepsilon s V R}{qND}} \tag{1}$$

$$V_{BR} = \frac{\varepsilon_0 \varepsilon_S s E^2 crit}{\varepsilon_0 \varepsilon_s} \tag{2}$$

$$E_{crit} = \sqrt{\frac{2qNDV_{BR}}{\varepsilon_0 \varepsilon_s}} \tag{3}$$



1. Displays approximate breakdown voltages for various silicon n type doping concentration.[1]



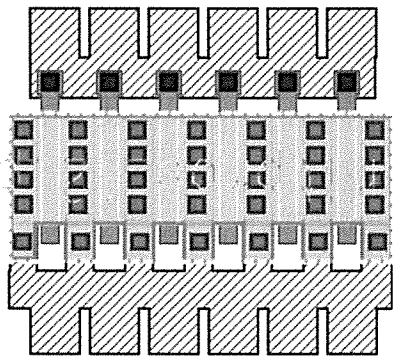
2. CROSS SECTION A VDMOS DEVICE WITH ON RESISTANCE SHOWN.

II. DESIGN

To achieve the best device performance an epitaxial region of 20 μm with a doping concentration of $1x10^{15}$ atoms/cm^3 and a substrate doping of $1x10^{20}$ atoms/cm^3 is required . This epitaxial region was chosen such that the depletion region was contained within the device. With a 150 volt reverse bias a depletion region of 14 μm was simulated. The high doping profile allows for low series drain resistance and an ohmic backside contact. The epitaxial layer on top of a highly doped region also helps mitigate effects of latch up due to the highly doped region serving as a current sink and allows carriers to recombine. While the design of this project is optimized with an epitaxial wafer, this project will focus on the design without the wafer due to budgetary constraints.

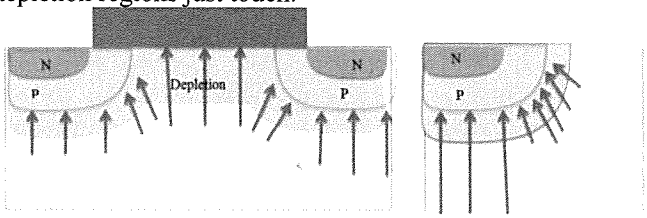
An optimum gate oxide must be designed to withstand the capacitance between the drain and gate bias while still having a low enough threshold voltage. Breakdown of the gate oxide can lead to undesirable effects such as gate leakage through the oxide. The dielectric breakdown of silicon dioxide was found to be about 11 mV volts per cm and a thickness of 1500 Å dry oxide was chosen for the gate oxide [2].

A self- aligned gate process was used to simplify lithography by using a poly silicon gate to align source drain contacts. Six devices were connected in parallel to reduce the series drain resistance. Devices utilized 4 different biases to the p-body, gate, source, and backside drain.

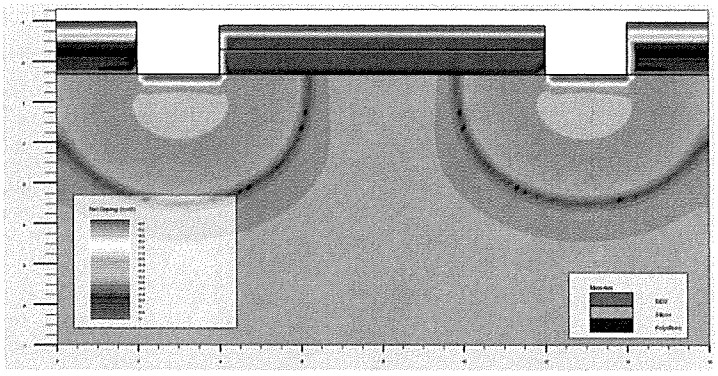


3. Layout of VDMOS devices

The spacing between source regions of the VDMOS must be optimized to reduce current crowding effects. With high electric fields the edge of the source regions will experience current crowding. A possible solution to remedy this extra series resistance entails having the depletion regions of each source touch to reduce high electric fields. Diffusion models will be simulated to obtain the optimal spacing where the depletion regions just touch.



4. Effects of current crowding in at the P well



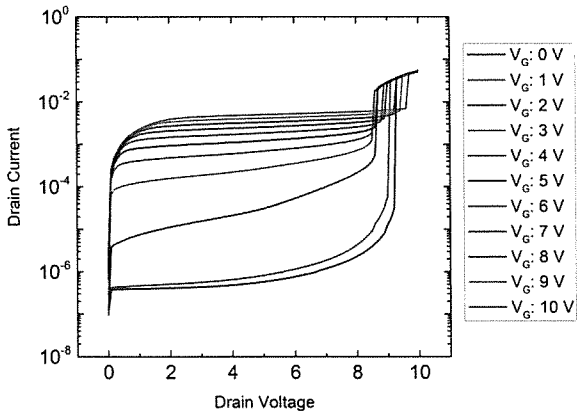
5.Silvaco ATHENA simulated doping profile and junction depth results.

III. FABRICATION

The fabrication of a VDMOS device consisted of 6 mask levels including active, gate, P+ contact, source, contact cuts and metal. First a six hour wet oxide growth recipe was used to grow 5000 A of field oxide. The field oxide was then patterned for the active region and 1500 A of dry gate oxide was grown. Next 500 nm of polysilicon was deposited using Low Pressure-Chemical Vapor Deposition The polysilicon was implanted with phosphorous at a dose of $1x10^{16}$ atoms/cm^2 at 50 keV. Then an anisotropic etch was used to pattern the gate which was followed by a boron P body implant with a dose of $5x10^{13}$ atoms/cm^2 at 100 kev. A six hour drive-in was immediately done after the implant the allowing the p-body to diffuse laterally to make a channel. Source drain implants were implanted using phosphorous to help push the drive-in the p-body wells. A p-body contact must also be made to avoid floating bodies. 500 nm of TEOS was deposited to serve as an interlayer dielectric (ILD) and contact cuts were subsequently lithographically defined. A 510 nm metal layer was evaporated using aluminum silicon and sintered. The last mask level was unintentionally fabricated as the inverse of the contact cuts leading to small contacts that would later effect testing.

IV. Testing

Testing of devices were done using a Keithley 4200 semicondcutor parameter analyzer. IDS vs VDS plots were generated with varying gate voltages. The drain voltages were swept from 0 to 10 volts while keeping the p body and source at 0 while the gate voltages were also swept from 0 to 10 volts. The threshold voltage of the devices were found to be about 4.5 volts for wider devices and the breakdown was similar for each gate length and was found to be about 9 volts. Devices were intended to be multi-finger devices with large bond pads but testing was done manually because error in the metal lithography step. Electrical connections could only be practically made to one of the six transistors intended to be connected in parallel. Series resistance did not appear to be a significant factor for these measurements.



4. ID vs VD curves for varying gate voltage

V. Conclusion.

It can be concluded that the devices prematurely broke down due to punch through in the P body. A breakdown of 9 volts was observed for the VDMOS devices.A P+ halo implant can be done in the well at the saddle point to prevent punch through of devices. This implant will need to be done at high energies around 300 kev and $5 \cdot 10^{15}$ atoms/cm^2 . This implant will make most of the depletion region occur within the vertical channel. Furthermore epitaxial wafers of 30um on arsenic substrates would help reduce series drain resistance and effect of latch up. In conclusion error in metal patterning caused higher series resistance due to the inability to test fingers of devices in parallel. Parallel devices would help spread the electric field and reduce effects of punch through in the P body.

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[2] "Oxide Breakdown." [Online]. Available: http://www.siliconfareast.com/oxidebreakdown.htm. [Accessed: 06-Dec-2013].

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