Dry Etching for High Aspect Ratio Silicon Fins

Michal Kucer

Abstract—**The aim of this project is to develop a dry etching process that could be utilized to realize high aspect ratio fins. The traditional planar silicon transistor has seen amazing development ever since it became the workhorse of the semiconductor industry and the dominant way of realizing logic and analog circuits. However as its gate channels length is scaled down, the transistor encounters issues termed short channel effects and which has sprouted an extensive research into future replacements for the planar MOSFET. One of such devices is the Fin Field Effect Transistor or FinFET. Most of the FinFET fabrication processes rely heavily on a highly anisotropic etching process to realize very thin fins. This report details the investigation into the possible chemistries used for anisotropic etching, further exploration and improvement of the process on wafers pieces. In the end, the report descibes the transfer of the Silicon etch from the wafer pieces to a full six inch wafer.**

Index Terms—**FinFET, dry etching, MOSFET, anisotropy.**

I. Introduction

THE MOSFET has been the workhorse of the industry for the past few decades. The basic principle for the functioning of the general transistor was invented and patented by Lilenfeld in 1925. However not until 1960 was the MOSFET invented and manufactured at Bell Labs by Kahng and Atalla, but did not reach their widespread popularity until the 1970s. Ever since the early 1970s MOSFETs were the predominant technology used for building digital circuits. Initial improvements simply consisted of supply, voltage thickness and gate length reduction, which did not provide significant challenges to the operation of the MOSFET. However as the prior mentioned dimensions were scaled further, transistors started exhibited unwanted short channel effects such as channel length modulation, drain induced barrier lowering, gate induced drain leakage or Vt roll-off [3]. Many of the problems have been solved by techniques such as dual-doped gates, silicon oxynitride, copper interconnects, lightly doped drains or SiGe source/drain regions.

However, one of the main drawbacks of the MOSFET was the inability of the gate dielectric to be scaled fast enough [1]. This poses a problem for example in high performance microprocessor applications with observe high active power dissipation. In order to solve resolve the issue, the voltage would have to be scaled which requires scaling of the dielectric thickness. Similarly, control over the channel results in a higher off-state current posing problem for the consumer electronics market, where the battery is often limited. The FinFET architecture thus emerged as a potential solution to the problem of leakage in the uncontrolled silicon under the transistor channel.

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Two main function of the source/drain junction is to provide a low-resistance contact between the metal silicide and the inversion layer in the channel and to provide isolation from the bulk majority carriers. As the channel length gets smaller, it is becoming increasingly difficult to realize this function.

As the channels get smaller, one of the largest problems that occur is drain induced barrier lowering, which refers to the reduction in the threshold voltage of the transistor at higher drain voltages. It often results in undesirable sensitivity to uncontrolled variations in the manufacturing process. In advanced CMOS manufacturing processes the source/drain regions comprise of two parts the high doped source/drain and then lightly doped extension, which aim to minimize the extension of the depletion region into the channel and the DIBL induced by the highly doped region.

However, as the channel length is further scaled, the channel doping must be increased to minimize the extension of the source drain depletion region which comes with several drawbacks:

- Highly doped p-n junctions are susceptible to band-to-band tunneling
- Increased ionized impurity scattering
- Degradation of the sub-threshold slope

In the end, one of the major challenges for planar CMOS is the variability of the transistors, as the slowest devices become the limiting factor in achieving higher clock frequencies. As the devices are scaled, the variability is higher because as the channel gets smaller, the random fluctuations in the number of dopant atoms become higher.

A. Introduction to the FinFET

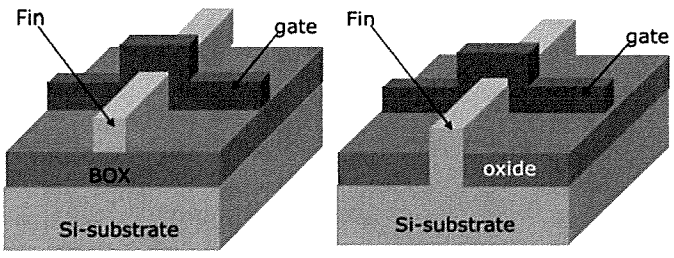

Fig. 1. Two most common realization of the FinFET

Figure 1 depicts the two most common realization of the FinFET: the Silicon in Insulator (SOI) FinFET and the FinFET manufactured in the bulk wafer without a buried oxide layer. The bulk FinFET uses a variation of the STI technology in realizing the isolation in between fins [1]. However both of the variations illustrate the main benefits from which the FinFET derives its desirable properties and thus is currently in the process of replacing the planar MOSFET technology.

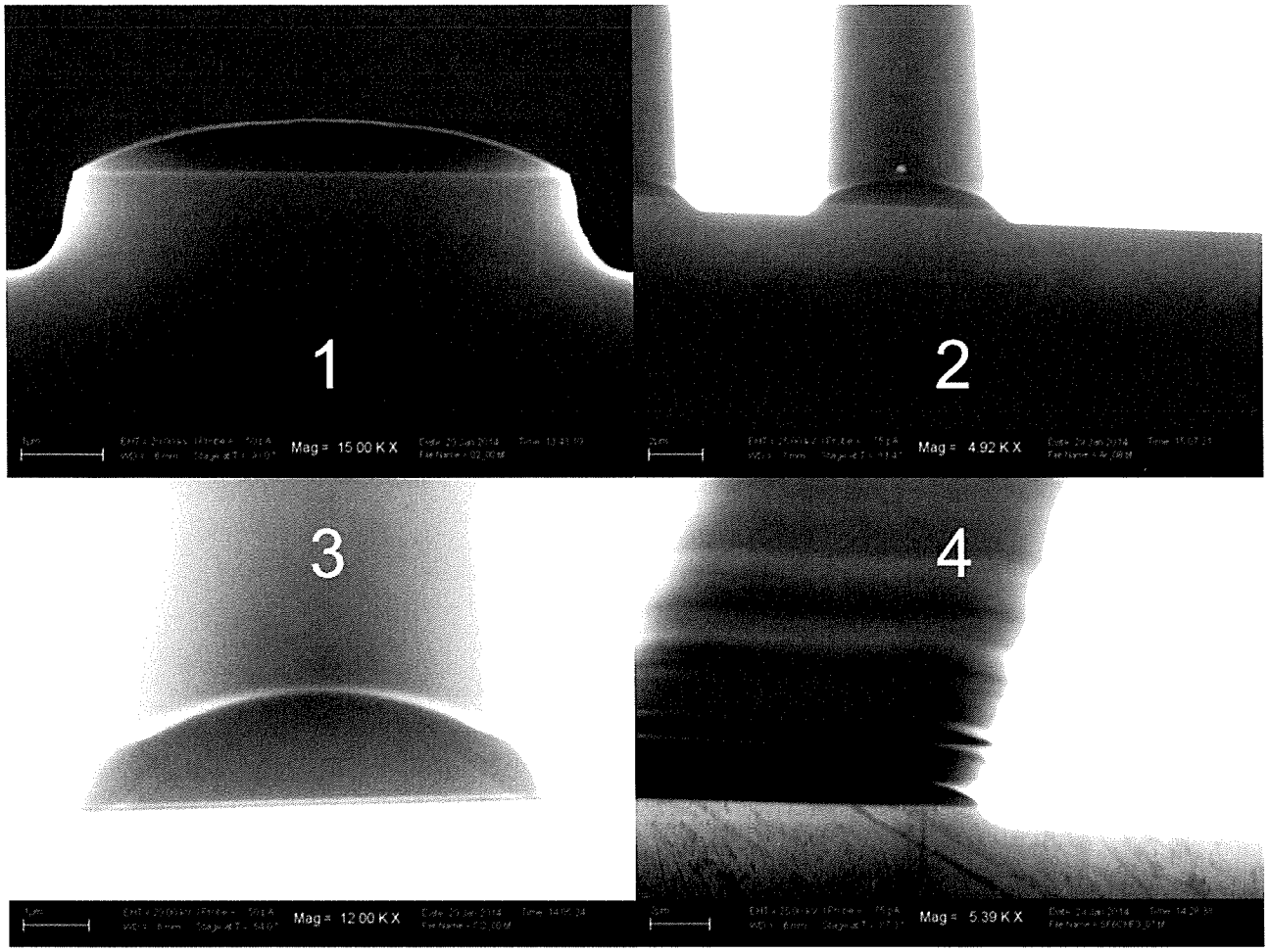

Fig. 2. Etch profiles of the Screen Experiment for the following chemistries : 1)$SF_6/CHF_3/O_2$, 2) $SF_6/O_2/Ar$, 3) Cl_2/BCl_3 and 4) SF_6/CHF_3.

The FinFET architecture was invented at the University of California at Berkeley by Hu et al. with the aim to reduce the leakage of the uncontrolled silicon underneath the channel [4]. The introduction of this device was met with great excitement, and ever since much research has spurred that aimed to study the fabrication techniques and electrical characteristics for the FinFET.

The increased control over the channel has a desirable influence of the drain in the form of reduced DIBL effect. In sufficiently narrow fins, the gate coupling over the channel could be so strong as to permit the removal of any channel doping which results in the following desirable effects:

- Reduction of the parasitic channel at the corners of the fin
- Improved sub-threshold slope because the gate voltage is free of the need to modulate the charge state of the channel doping
- Elimination of variability due to dopant atom fluctuations
- Increase in carrier mobility

The main benefit behind the finFET is realized when the fin is tall enough and thus the effective channel width ($W_{fin} + 2xH_{fin}$) is larger than then the fin pitch, since in this case device can realize more current per unit area. This is crucial in digital circuit since the higher drive current can change the states faster.

II. Background

A. Fin Patterning

As is apparent from description for, the process relies heavily on highly anisotropic silicon etching of the hardmask (HM), spacer and the Si. Therefore in the while designing a fabrication flow, it is important to choose processes that are likely to provide the desired outcome.

Currently the two materials that are being considered for the role of the HM, the spacer material and the sacrificial layer are: grown SiO_2, Low temperature oxide (LTO) and Si_3N_4. All of these films have well defined recipes that provide sufficient level of anisotropy and thus will not be discussed in detail. The critical step in the process in the definition of silicon fins. Dimensions small enough are important to realizing the desirable fully-depleted characteristic, which is responsible for the superior control over the leakage current. In order to realize the Si patterning, the following techniques are being considered: Reactive Ion Etching, Crystallographic etching using KOH and TMAH.

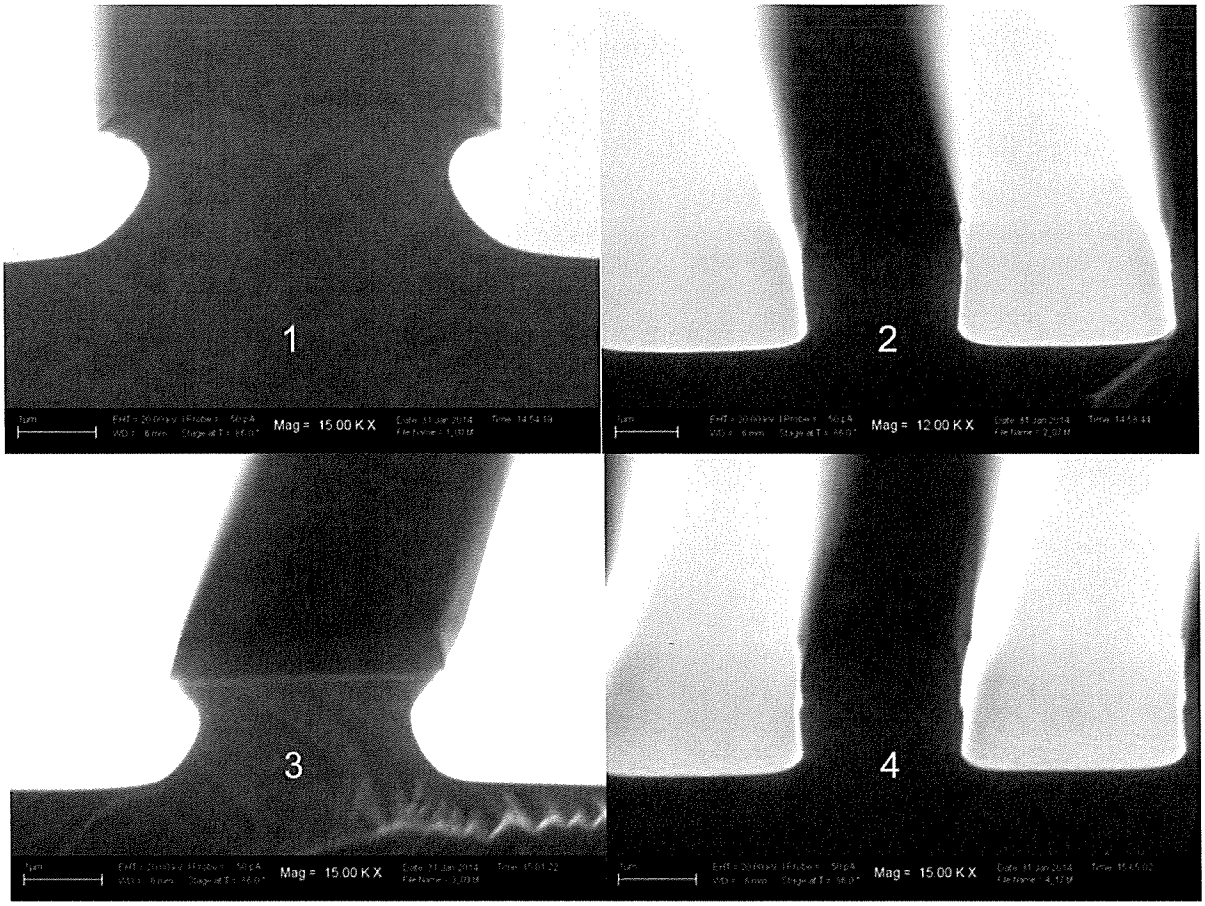

Fig. 3. Etch profiles of Experiment 2

B. Reactive Ion Etching (RIE)

Reactive ion etching is one of the most widely utilized etching technologies currently used in the industry. It uses chemically reactive plasma in order to remove the material deposited on the wafer. A typical setup is shown in Fig. 6 and consists of the following parts: Electrodes (1 and 4) used to create an electric field (3) meant to accelerate ions (2) toward the samples.

Region 2 represents the plasma that contains both positively and negatively charged ion which are generated from the gases pumped into the chamber. RIE is often the preferred method of etching because:

- Eliminates handling of dangerous acids and solvent
- Uses small amount of chemicals
- The etch profile can be tuned by varying the gas flow, power, etc.
- Could provide less undercutting
- Ease of automation

These are only some of the many advantages that RIE provides (major disadvantages include the cost of the equipment, the various dangerous toxic and corrosive gases and damage induced by plasma processing could be a major factor).

The most popular gases that are used for anisotropic etching of Si are SF_6, CHF_3 and O_2. Therefore one of the major tasks for initial processing is determination of a suitable recipe that should be used is there one?

C. Crystallographic Etching

One of the other possible ways that Fins can be formed is Crystallographic etching, which is simply anisotropic etching along crystal planes. Different alkaline etchants such as KOH or TMAH etch at very different rates depending upon which crystal face is exposed.

In our case, KOH etches anisotropically with a 54.7° angle with respect to the surface and thus produces a profile as shown on Fig. 7.

III. Results

A. Limitations of the tool

The Drytek Quad 4200 has been at the RIT SMFL since 1995. Originally suited for etching of rectangular plates, it was repurposed by B. Tolleson of SMFL in order to handle wafer pieces up to full six wafers. The tool itself contains fours chambers with varying gas availability per chamber. The first and second chamber flow SF_6, CHF_3, O_2 and Ar suitable for Silicon, Nitride and various metal etches. Chamber three replaces SF_6 with CF_4 in order to allow for sulfur-less ething of silicon dioxide. In the end, the fourth chamber flows CH_4 in order to allow for the PECVD deposition of carbon films.

One of the major dry etch components is the pressure of the process and thus it is very important to understand the limitation of the tool in this regard. It was very desirable to achieve very small pressures (3 mTorr - 20 mTorr), since it is called for many of the papers that report successful anisotropic silicon etching.

The exploration of the minimum pressure started at 20 mTorr, since the was the lowest pressure used and reported in a student thesis [7]. The first experiment aimed to create or "stirke" plasma at 20 mTorr for a period of a minute with little reflected power reported by the system. Thus proved to be futile as no plasma was created and all of the power supplied to the tool was reflected back to the tool. Thus, the experimentation continued with increasing the plasma in 10 mTorr increments and it was found that the tool could operate at 40 mTorr with limited success (2 out of 4 tested runs ended due to error caused by excessive reflected power , because it was not corrected for my the matchbox) and operate successfuly at 50 mTorr pressure.

This knowledge provided us with a starting point and constraint for the first screening experiments, since some of the recipes used in the literature [5] and [7] aimed to run the processes in the 10 mTorr range.

B. Etchin of Si

1) Screening experiment: Figure 1 shows the results of the screening experiment, which served as the starting point for the exploration for the suitable silion etching recipes. First, a survey of the available literature was conducted to understand the information available about silicon etching for anisotropic etching. Then, we an initial experiment with four varying etch chemistries was chosen. The following gas mixtures were explored Cl_2/BCl_3, $SF_6/CHF_3/O2$, SF_6/CHF_3, $SF_6/CHF_3/Ar$. The initial conditions for some of the screening etches had to be adjusted in order to account for the limitations of the tools that were are using (the Chlorine etch was preformed at the LAM 4600 at the RIT SFML, however since the process itself did not yield satisfactory results, the tool is not discussed in detail in the paper). This meant adjusting the gas flows and chamber process pressures in order to account for the lower limit of achievable pressure and lower limit for the accuracy of the mass flow controller (20 % of the maximum flow).

The resulting etch profiles for the screening experiment can be seen in Figure 1. It is evident, that none of the etch conditions shown in the figure provide suitable conditions, since all show excessive mask erosion at the edge of the feature. Despite this, a treatment of $SF_6/CHF_3/O2$ was chosen to be a starting poin for the subsequent experiments, since it was the only condition that provided any significant etching of the silicon wafer.

2) Experiment 2: The second experiment aimed to further explore the suitable conditions for silicon etching. Due to the evident mask erosion at the edges of mask features, the initial power setting of 200 W was lowered to 125 W. Furthermore, since the etches were preformed on wafer pieces, we changed the nominal pressure and oxygen gas flow in order to observe their effect on the etch profile. The condition of the etches and their results are detailed in table 1 and the resulting etch profiles are shown in Figure 3. Ascan be seen from both the SEM captures and the measured values, condition 2 and 4 are the standout candidates that would be chosen for futher etch optimization, since both of the etches provided nearly vertical sidewalls.

It is worthwhile pointing out the difference between the etches on wafer pieces 2 and 4. The latter etch condition reduced the SF_6 flow rate to 50 sccm and as can be seen in Table 1, we saw an increase in anisotropy and decrease in the etch rate and thus giving us better control about the etch thickness. Both of the observed features can be explained by the decrease in the SF_6 to O_2 ratio.

The decrese in the SF_6 concentration would account for the decreeased etch rate (due to lower Fluorine ion concetraion). Additionaly increase in the O_2 would concentration explain the incresea in the rate of anisotropy due to better sidewall passivation by the formation of SiO_2.

3) Experiment 3 and verification of the etch conditions: Experiment 2 yielded promising results and thus it was desired to verify that the achieved profiles were not just an artifact and were truly repeatable. Thus Experiment 3 simple ran under conditions match the best cases from experiment 2. However it was a big surprise to find out that the etch result were drastically different from what we saw previously as can be seen in Figure 4 below.

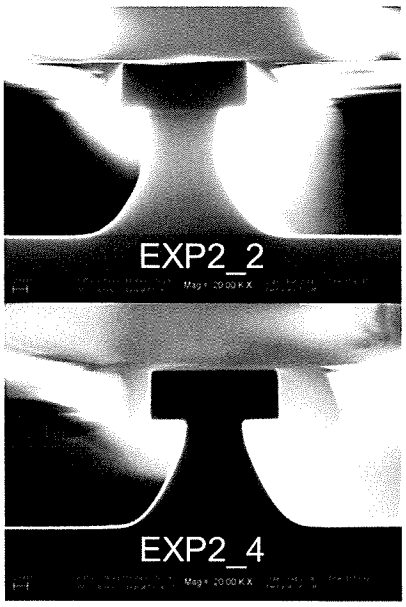

Fig. 4. Etch profiles of the samples for Experiment 3.

Thus in order to determine the reason for the significant difference between the two experiments, we have devised the following runs:

In our experiment, we varied the following three parameters: Size of the wafer (simply refers to a fraction of the wafer used for etching), mask (different standard ASML mask patterns at SMFL) and the wafer carriers (which were suspected to be made of different materials, thus providing a varying load

TABLE I
TABLE DETAILING THE ETCH SETTINGS RESULTS CONSISTING OF THE ANISOTROPY, ETCH RATE AND SI:PHOTORESIST ETCH RATE.

Experiment 2						
Wafer Name	SF6/CHF3/O2 (sccm)	Pressure(mTorr)	Power(W)	Anisotropy	Etch Rate	Si : PR
EXP2_1	60 / 24 / 20	100	200	0.583	553.333	2.468
EXP2_2	60 / 24 / 20	100	125	0.935	479.000	N/A
EXP2_3	60 / 24 / 20	60	125	0.674	471.333	2.952
EXP2_4	50 / 24 / 20	100	125	0.942	382.000	2.684
Experiment 3						
Wafer Name	SF6/CHF3/O2 (sccm)	Pressure(mTorr)	Power(W)	Anisotropy	Etch Rate	Si : PR
EXP3_1	60 / 24 / 20	100	125	0.755	1202.000	5.854
EXP3_2	60 / 24 / 20	100	110	0.784	1047.333	3.280
EXP3_4	55 / 24 / 20	100	125	0.661	1037.333	5.441
Experiment 4						
Wafer Name	Size / Mask(ETM) / Carrier	Time	DC Bias	Anisotropy	Etch Rate	Si : PR
EXP4_1	1/6 / 13 / 1	1.5	150-160	0.725	1245.333	11.186
EXP4_2	1/6 / 1 / 2	1.5	122-140	0.929	491.333	3.204
EXP4_3	1/4 / 13 / 1	1.5	160-180	0.761	1285.333	12.126
EXP4_4	1/4 / 1 / 1	1.5	160-180	0.695	1220.667	7.825
Experiment 5						
Wafer Name	SF6 / CHF3 / O2 / Power	Time	DC Bias	Anisotropy	Etch Rate	Selectivity (Si : PR)
EXP5_W1	60 / 24 / 20 / 125 W	1.5	140-160	0.873	1232.000	6.600
EXP5_W2	60 / 24 / 20 / 120 W	1.5	90-110	0.894	1136.000	9.276

TABLE II
ADD CAPTION

	Size of the Wafer	Mask	Carrier
EXP4	1/6	ETM13	1
EXP4	1/6	ETM1	2
EXP4	1/4	ETM13	1
EXP4	1/4	ETM1	1

resuilting in different induced self bias thus effecting the Electric field that acceletares charged particles in the system).

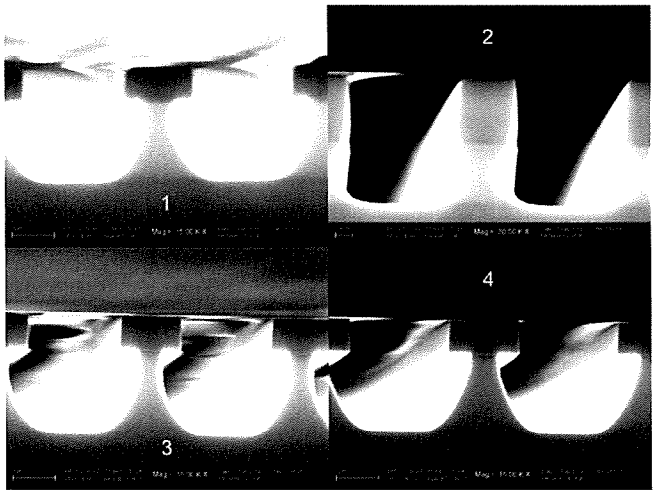

Fig. 5. Results showing the difference between using carrier 2 (2) as opposed to carrier 1 (1,3,4).

As can be seen from the figure 5 above, representing the etch profiles corresponding to the four wafer treatments detailed in table 2, we can see that all of the treatments whose used carrier one observe a very similar profile previously encountered in experiment 3. On the other hand etch profile of the second sample resembles the desirable profile we initially observed in experiment two. This indicated that the choice of the wafer carrier for smaller pieces has a serious effect on the load and thus the bias voltage of the plasma for a given power setting - as can be seen in table 1 which shows us the large difference between the biases of the two carriers.

4) Transferring the etch onto a full 6" wafer: Once we determined the culprit preventin the repeataility of the results and thus verifying the recipe, we decided to proceed to tranfer the recipe to a full six inch wafer, since it is desirable for the recipe to be used in full production in the RIT SMFL as well as for possible FinFET fabrication at RIT. The etch trasfer yielded results shown in the image below.

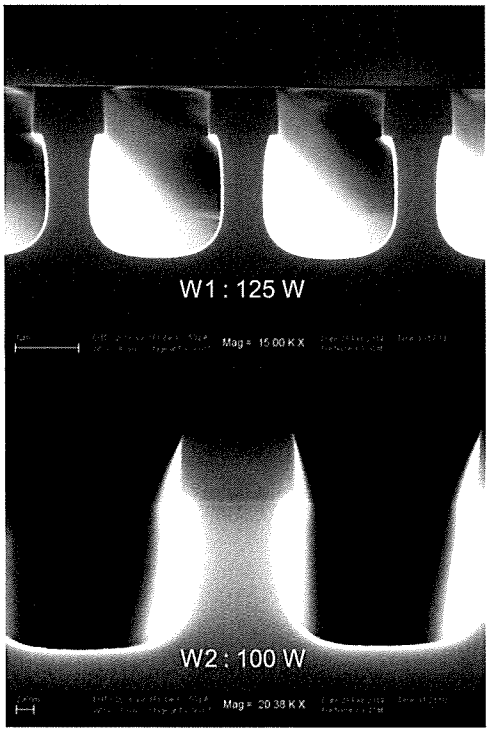

Fig. 6. Etch profile of the 6" wafer for two different power settings

It can be seen that the results provided satisfactory results with rate of anisotropy of 0.894 at 100 W power setting.

5) Design of Experiments for furter recipe tuning: The transfer to the six inch wafer was reasonably successfull, however it is desirable to further optimize the results to obtain steeper sidewalls. Thus a Central Composite Design was chosen varying SF_6 flow and the chamber pressure. The design was modeled using JMP IN, which automically chose the order of the trials and treatments in the following way:

TABLE III
TABLE OF TREATMENTS FOR THE 6" DOE

	Pattern	Pressure	SF6 Flow
1	a0	90	60
2	++	110	70
3	–	90	50
4	+-	110	50
5	0A	100	70
6	-+	90	70
7	0	100	60
8	0a	100	50
9	A0	110	60
10	0	100	60

Due to the time constraints, it was not possible to fully analyze the SEM crossections of all of the wafers.

IV. CONCLUSION

The primary aim of the project was to develop a highly anisotropic etch that would for high aspect ratio fin etching aiming to provide the building ground and infrastructure for FinFET fabrication at RIT SMFL. The work fist explored the various different chemistries that could possibly be used $(Cl_2, BCl_3, SF_6, CHF_3, O_2, Ar)$ and then surveyed the limitation of the different tools used for the work. As it was reported, Drytek Quad had several limitationss in terms of the lowest achievable pressure and gas flow. This resulted in the need to approriate some of the reported result in the literature to suit our tool. Initial chemistry investigation found the $SF_6/CHF_3/O_2$ gas combination to be the most suitable for our current experiment. First promising results were hampered by the subsequent inadequate and unexpected results on wafer pieces. In order to determine the reason for the inconsistency in our results, we devised a simple experiment, which showed us that the individual wafer carriers were manufactured out of different materials and thus provided different DC bias resulting in different etch profiles. Subsequently we proceeded into transferring the recipe onto a 6" wafer, which prooved to be successfull, since we obtained anistropy of 0.894.

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