

# Investigation of Electrical Characteristics of Sputtered IGZO TFTs

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**Abstract**—A study on the gas ambient (varying percent  $O_2$  flow) and gap spacing (distance between the target and wafer) during the sputter deposition of indium-gallium-zinc-oxide (IGZO) for a TFT channel material was executed. The effect these parameters have on electrical characteristics was investigated to better understand the role  $O_2$  vacancies play on device performance. This experiment was performed to enable investigations on IGZO TFTs without the use of external resources. Devices fabricated exhibited differences between treatment combinations, however results show a lower on-off current ratio, larger sub-threshold swing (SS) and higher threshold voltage ( $V_{th}$ ) than observed from devices fabricated with IGZO deposited through collaboration with Corning Incorporated.

**Index Terms**—IGZO, sub-threshold slope, thin-film transistor.

## I. INTRODUCTION

**T**HIN film transistors (TFTs) are used in flat panel display (FPD) backplanes in an active matrix configuration to switch on and off pixels as the scanning electrodes are activated during the frame refresh. Active matrix displays offer significant performance improvements over legacy passive matrix designs where the scanning and signal electrodes are directly connected to the pixel. An inherent problem with this design is the resulting blurred images from non-selected pixels being turned on through leakage paths. This is a result of the pixels being addressed for longer durations due to the low voltages required to control the liquid crystal. this voltage is too low to realign the crystals quickly and also results in slower response times and reduction in contrast ratio. The addition of a switching transistors and storage capacitors as seen in Fig. 1 reduces crosstalk between scanned rows by eliminating leakage paths present in passive matrix designs resulting in the ability to produce high resolution displays with faster refresh rates than allowed by passive matrix designs [1]. The dominant technology in the flat panel display (FPD) industry has historically been amorphous silicon (a-Si) TFTs. This is due to their transparent nature, ability to be deposited on large substrates, low temperature processing ( $< 400^\circ C$ ) compatible. In addition to these processing reasons they exhibit high on-off current ratios ( $> 10^6$ ). Issue arise when using an amorphous semiconductor and for a-Si these include low mobility ( $< 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ), electrical instability when illuminated requiring an opaque capping layer covering the TFT, and electrical bias stress resulting in threshold voltage ( $V_{th}$ ) shifts  $> 10 \text{ V}$  [2]. These electrical problems were not previously critical to AM-LCDs smaller than 90" diagonally due to driver circuits incorporated in LCD FPDs which provide correction for these issues. With the advent of organic light emitting diode (OLED) displays the limitations of a-Si such as mobility become

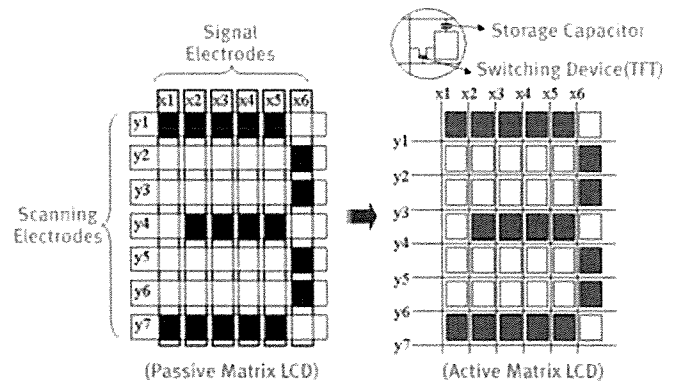


Fig. 1. Passive and Active Matrix LCD [1].

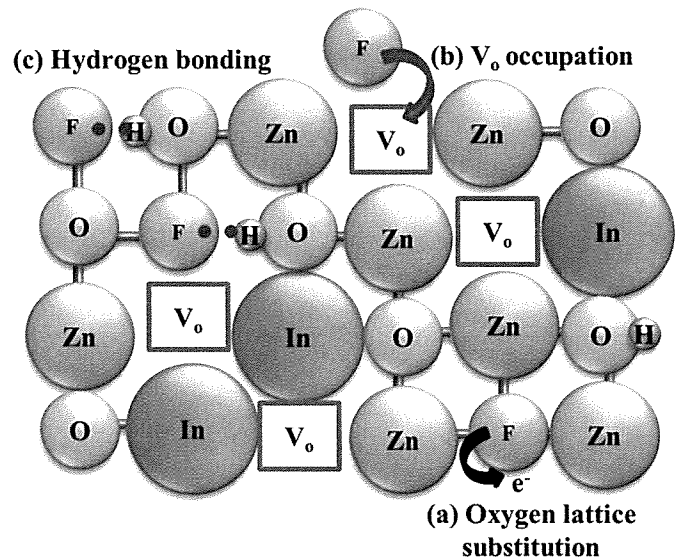


Fig. 2.  $O_2$  vacancies in indium-zinc-oxide (IZO) film [4].

apparent. These limitations are more pronounced with OLED FPDs because of the higher mobility required to drive the pixels due to their nature as a current-driving device. In OLED applications the  $V_{th}$  shifts are also critical and any non-uniformity will cause unacceptable differences in brightness between pixels. To solve this problem and continue using a-Si complex compensations must be used to address this problem resulting in larger and more expensive devices [3].

Amorphous indium-gallium-zinc-oxide (a-IGZO), a transparent semiconductor is being investigated due to promising electrical properties that rival a-Si. These improvements include mobilities above  $10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ , on-off current ratios of  $10^9$  and lower  $V_{th}$  shifts  $< 2 \text{ V}$ . The improved electrical charac-

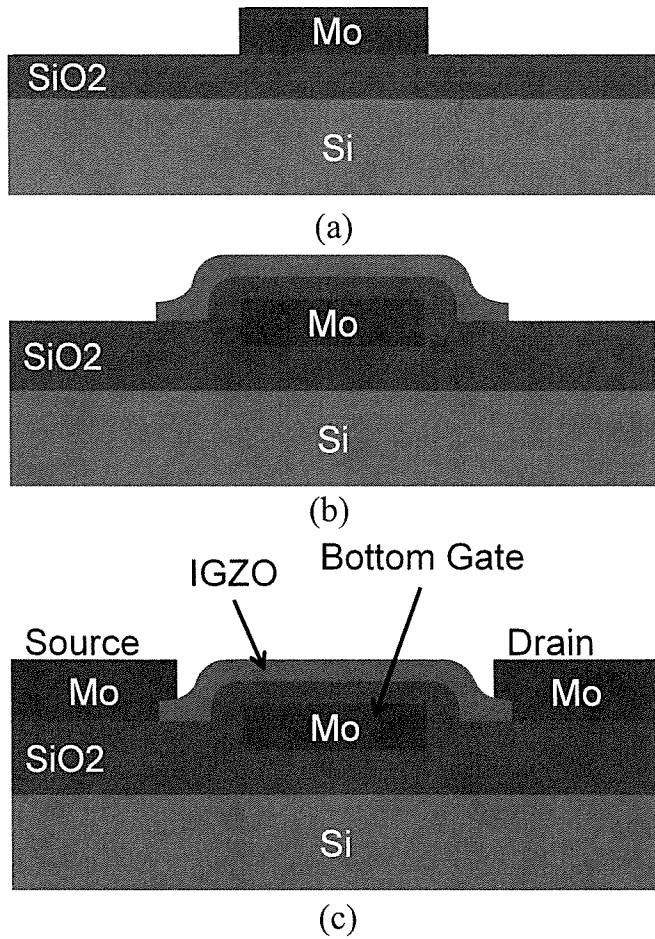


Fig. 3. Simplified process flow (a) isolation oxide and bottom gate metal, (b) gate dielectric and semiconductor deposition, and (c) gate contact and source/drain metal deposition and liftoff.

teristics makes IGZO TFTs a likely candidate to replace a-Si. The increased mobility of IGZO is sufficient for driving OLED displays without a separate LCD driver circuit resulting in higher yield and reduced costs [3]. a-IGZO is compatible with large substrate deposition and low temperature processing that already exists for a-Si so transition time would be minimal. Presently issues exist with a-IGZO TFTs such as controlling the number of  $O_2$  vacancies in the film, and passivation to reduce device stability issues.  $O_2$  vacancies act as donor states in IGZO and varying their concentration within the film results in  $V_{th}$  shifts and changes in free electron concentration. These adverse effects may be countered by annealing and passivation of the channel material. Fig. 2 depicts  $O_2$  vacancy states within an indium-zinc-oxide (IZO) film [4].

## II. EXPERIMENTAL PROCEDURE

Reclaimed silicon wafers were obtained and a thermal oxide of 5000 Å as an isolation layer between the TFT and silicon substrate. Molybdenum was sputtered in a DC sputter system to a thickness of 1000 Å. It was etched leaving the bottom gate of the TFT exposed. After the 1000 Å gate dielectric, a low temperature oxide (LTO), was deposited in a low-pressure

TABLE I  
DESIGNED EXPERIMENT VARYING  $O_2$  FLOW RATE AND SPUTTER GAP SPACING

Wafer	Ar/ $O_2$ Flow (sccm)	Sputter Gap Spacing (cm)	IGZO $\bar{X}$ (nm)	$\sigma$ (%)
1 Baseline	26/6.5	17 Baseline	57.7	NA
2	42/3		44.0	NA
3	39/6		63.1	28.9
4	36/9		45.4	14.1
5	26/6.5	4	28.4	NA
6	42/3		46.7	NA
7	39/6		47.1	8.7
8	36/9		38.6	7.1

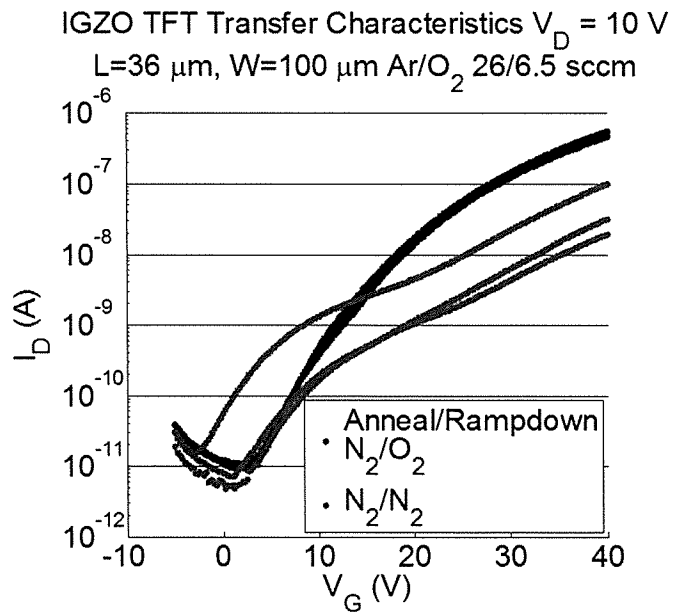


Fig. 4. Comparison between anneal ramp-down ambient of  $O_2$  and  $N_2$ .

chemical vapor deposition (LPCVD) and the gate dielectric was etched. The LTO was then densified in a  $N_2$  ambient for 600 °C for 120 min. After this a designed experiment was performed to evaluate the effects of  $O_2$  flow rate while keeping the total flow constant, and the sputter gap spacing as seen in Table I. The sputter was performed with an RF power source in a Kurt J. Lesker PVD 75B and a 4" target with an initial composition of  $(In_2O_3)(Ga_2O_3)(ZnO)_2$ . The film thickness and non-uniformity was measured on a Prometrix SpectraMap. The uniformity was evaluated by the standard deviation of a 41 point optical measurement. Some wafers were unable to be measured on the SpectraMap and had to be measured with the Woolam Vase ellipsometer to obtain the film thickness. Following the IGZO sputter an etch in dilute HCl was performed to define the active area. Contacts to the gate metal were opened and source, drain area was defined by lithography. Molybdenum was sputtered, 50 Å and then 3000 Å of Al was evaporated on top of that and a liftoff process was performed. The wafers were then annealed for 2 hours

TABLE II  
EFFECT OF VARYING SPUTTER GAP DISTANCE ON  $V_{th}$ , SS AND  $I_{ON}$

Sputter Gap (cm)	$V_{th}$ (V)		SS (V/dec)		$I_{ON}$ (A) @ $V_D = 40$ V	
	26/6.5	42/3	26/6.5	42/3	26/6.5	42/3
17	20.0	21.8	3.90	5.74	$4.85 \times 10^{-7}$	$8.63 \times 10^{-7}$
4	21.4	20.5	6.49	5.67	$8.16 \times 10^{-8}$	$6.39 \times 10^{-7}$

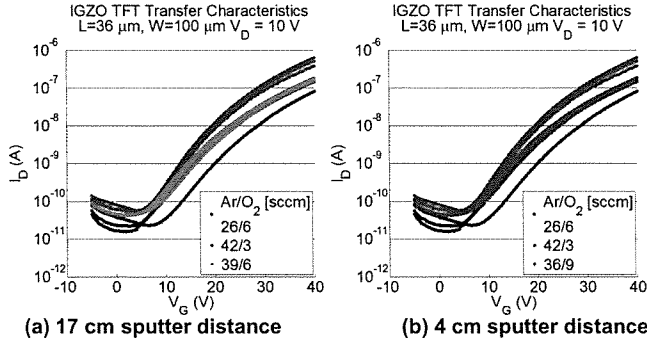


Fig. 5. Comparison of  $O_2$  flow rate during IGZO sputter for (a) 17 cm sputter distance and (b) 4 cm sputter distance.

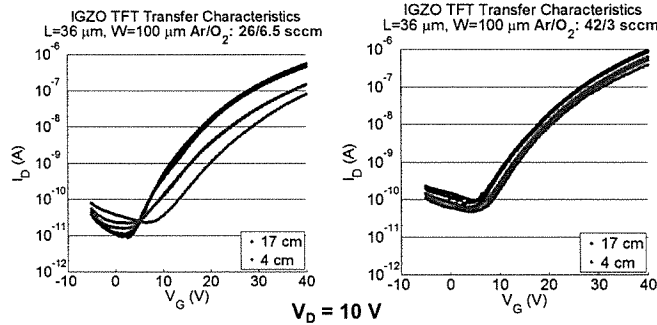


Fig. 6. Comparison of 17 cm and 4 cm sputter gap distances among flow rates of  $Ar/O_2$  26/6.5 sccm (left) and 42/3 sccm (right).

in a  $N_2$  ambient. A comparison between a 4 hour  $N_2$  and  $O_2$  ramp-down from 400 °C to room temperature was performed to evaluate the effect of annealing ramp-down ambient on TFT performance.

### III. EXPERIMENTAL RESULTS

Devices that were annealed and ramped-down in a  $N_2$  ambient showed degraded performance compared to devices that were annealed in  $N_2$  and ramped-down in  $O_2$  as seen in Fig. 4. The remainder of the wafers were annealed in  $N_2$  and ramped-down in  $O_2$  as that treatment resulted in the best device performance.

As the  $O_2$  flow rate during sputter decreased, the SS decreased and  $I_{ON}$  increased for the devices that were sputtered at 4 cm. Devices that were sputtered at 17 cm showed less sputter induced variation as seen in Fig. 5. This shows that there is an interaction between the  $O_2$  flow rate and sputter gap distance on TFT performance.

TABLE III  
ELECTRICAL CHARACTERISTICS OF RIT AND CORNING SPUTTERED IGZO TFTs.

	RIT	Corning
Current Drive (A) @ $V_D = 10$ V	$5.24 \times 10^{-10}$	$3.42 \times 10^{-5}$
Sub-threshold slope (V/dec) @ $V_D = V_G = 10$ V	3.9	0.159
$V_{th}$	20	0

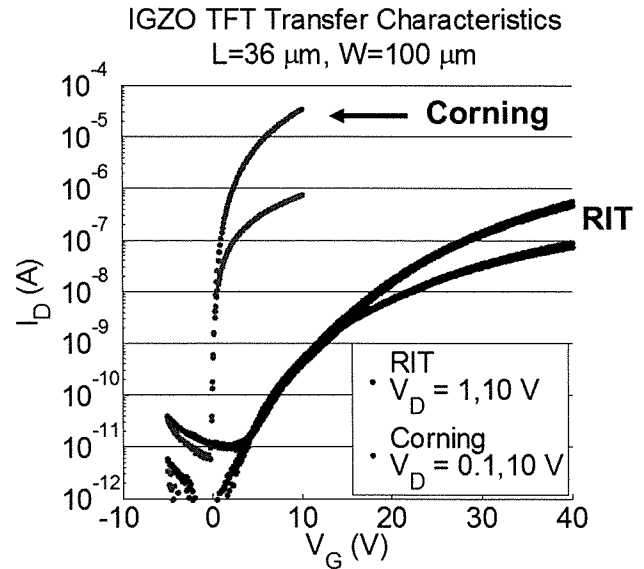


Fig. 7. RIT and Corning sputtered TFT transfer characteristics.

When sputter distance was decreased the deposition rate increased and non-uniformity decreased as seen in Table I. The effects on device performance depended on what  $Ar/O_2$  flow rates were used during sputter. For the baseline  $Ar/O_2$  sputter flow rate of 26 and 6.5 sccm respectively the sputter gap had a large effect on SS and  $I_{ON}$ . The decreasing sputter gap resulted in degraded SS from 3.90 to 6.48 V/dec and  $I_{ON}$  decreased approximately one order of magnitude while  $V_{th}$  remained consistent. The devices sputtered with an  $Ar, O_2$  flow rate of 42 and 3 sccm respectively showed no change in  $V_{th}$ , SS or  $I_{ON}$ .

In comparing TFTs where IGZO was sputtered at RIT and Corning the RIT sputtered devices show degraded SS of 3.9 V/dec compared to the 0.159 V/dec,  $V_{th}$  increasing from 0 V to 20 V and  $I_{ON}$  5 orders of magnitude lower as seen in Fig. 7 and Table III. The optical n and k values were extracted using a

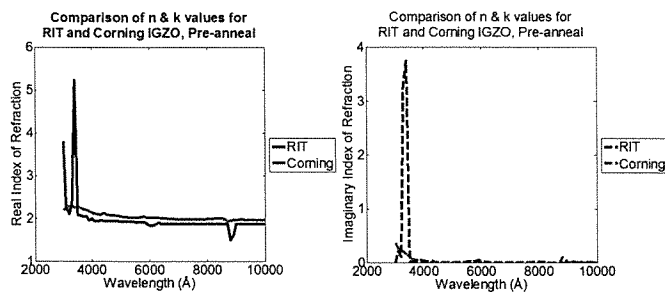


Fig. 8. Optical constant extraction of RIT (blue) and Corning (red) sputtered IGZO.

Woolam VASE ellipsometer to determine if the discrepancy in electrical performance was due to differing film composition.

As can be seen in Fig. 8 RIT sputtered IGZO has a large peak in reflection and absorbance at a wavelength of approximately 3500 Å. After this point the reflection drops below the Corning material. This indicates that the films are compositionally different as well as electrically.

#### IV. CONCLUSION

When evaluating the performance of TFTs it was determined that a  $N_2$  anneal followed by a ramp-down in a controlled  $O_2$  ambient resulted in devices with superior electrical performance than devices exposed to the anneal and a  $N_2$  ramp-down. The effect of  $O_2$  flow rate during sputter on  $SS$ ,  $V_{th}$  and  $I_{ON}$  was also dependent on the sputter distance. Decreased  $O_2$  flow during sputter resulted better performing devices at a sputter gap distance of 4 cm. The effects of process dependent variation with respect to  $O_2$  flow rate were minimized at a larger sputter gap of 17 cm.

Electrically, devices with IGZO sputtered at Corning produced vastly superior TFTs than those with IGZO sputtered at RIT in terms of  $SS$ ,  $V_{th}$  and  $I_{ON}$ . In addition VASE measurements extracted  $n$  and  $k$  values which showed that there were optical differences between the two sputtered films. This indicates that the films may be compositionally different from one another in terms of IGZO composition or crystal structure. A quantitative analysis of IGZO film composition is required via x-ray diffraction (XRD) or some other method to evaluate if any differences are present between RIT and Corning sputtered IGZO.

Additional future work required includes an analysis into the effect IGZO film thickness has on free electron concentration in the semiconductor. This will be investigated due to the process variation in sputtered IGZO film thickness inherent with the Kurt J Lesker RF sputter tool present at RIT. Characterization of the effect various passivation materials have on the electrical characteristics of IGZO TFTs is also required to improve device performance with respect to stability over time, and under bias stress conditions.

#### V. ACKNOWLEDGMENTS

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