Investigation of a Self-Assembled Monolayer as a Cu Diffusion Barrier for Solar Cell Metallization

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***Abstract*—Copper diffusion into the silicon bulk is a detrimental obstacle to advanced-CMOS and photovoltaic processes that seek to incorporate copper into the metallization steps because of its deep-level trap nature to carriers. Recent studies have hinted that an organic porphyrin or silane-based self-assembled monolayer (SAM) could be a method of prevention to copper diffusion. Inorganic alternatives using TiO_2 or Ni may also present a solution. The self-assembly of 5,10,15,20-Tetrakis(4-hydroxyphenyl)-21H,23H-porphine (OHTPP) over SiO_2 has been examined using atomic-force microscopy (AFM), contact angle measurements, and variable angle spectroscopic ellipsometry (VASE). Results indicate that this particular OHTPP chemistry fails to adsorb to the SiO_2 substrate. Metal-Oxide-Semiconductor (MOS) capacitors with varying dielectric stacks with and without TiO_2 over SiO_2 or Si_3N_4 and gate metals varying between Cu and Ni have been fabricated and analyzed via bias-temperature stress (BTS) capacitance-voltage (C-V) tests. Results indicate that Cu-coated TiO_2 and Ni MOS stacks with a SiO_2 insulator show drastic flat band voltage shifting compared to Cu over SiO_2 or with a Si_3N_4 dielectric over SiO_2.**

***Index Terms*—Bias-Temperature Stress, Copper Diffusion Barrier, Photovoltaics, Self-Assembled Monolayer**

I. Introduction

THE use of copper in metallization processes for CMOS and various advanced devices is becoming increasingly popular due to the low resistivity (1.7 μΩ-cm) and high resistance to electromigration at elevated temperatures and bias conditions [1] [2] [3]. Although Cu is not typically subjected to high electric fields in photovoltaic applications, it is of interest to replace conventional Al and Ag solar cell contacts with Cu for process compatibility with neighboring CMOS and bipolar circuit designs using Cu metallization and the industry standard dual-damascene process. It is also economically feasible to replace costly silver with copper. Typically, NiSi is used as a barrier between Cu and Si for solar cells, but no barrier exists between the Cu and anti-reflective coating (ARC) which is usually Si_3N_4. Therefore Cu migration into Si_3N_4 is also of interest. The use of Cu ultimately results in faster device operation by lowering the RC time constant and could improve the quantum efficiency of solar cells. However, copper readily diffuses through oxide and into silicon because it has a relatively small ionic radius on the order of 0.74 Å and poorly interacts with the silicon crystalline lattice. As an interstitial within the lattice, Cu will act as a donor and thus the electron configuration of Cu changes from $1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10} 4s^1$ to $1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10}$. This is an unusual configuration as a transition metal, but Cu is the only element of this group that exhibits this electron configuration [4]. The diffusion constant for an unpaired Cu atom in crystalline silicon is well known to be 0.0047 cm^2/s with an activation energy of 0.43 eV [5] [6]. The diffusion barrier for Cu in Si is 0.18 eV, which is substantially lower than that of the rest of the transition metals, which are usually found to be greater than 0.6 eV [4]. Copper, like any other atom, can only diffuse if it overcomes the potential barrier at the junction with its nearest neighbor [7].

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II. Theory

Copper interstitials within p-n junction diodes are known to cause increased leakage currents because Cu lowers the breakdown electric field of the device. This is due to defects formed by copper precipitates coupled with Fermi effects. Copper is less likely to form precipitates in p-type silicon than in n-type silicon [4]. Copper acts as a deep level trap in the silicon bulk and consequently lowers the minority carrier lifetime because of its high electronegativity (1.9) [8] [4]. A possible remedy for this is to instill gettering sites during fabrication to trap any Cu interstitials that find their way into the bulk [1]. The effect of copper on silicon dioxide has been thoroughly studied and the results vary substantially between each experiment [8] [4] [9]. It has been shown that copper causes a decrease in lifetime and breakdown electric field of the oxide. However, the differences found in each experiment are most likely due to variation in contamination levels, the number of gettering sites in the silicon, and the concentration of copper precipitates at the oxide-Cu interface. High contamination and copper precipitate levels increase the breakdown susceptibility of the oxide. Increasing the number of gettering sites lowers the breakdown effects.

In order to mitigate the detrimental effects of copper traps and impurities, barrier layers must be used before copper deposition [1] [4]. Traditional barriers have consisted of TiN or TaN to name a few. However, the trend in device scaling means that these materials will no longer meet the

requirements dictated by ITRS. A possible solution is the use of self-assembled monolayers (SAMs). A successful barrier layer must not only meet scaling requirements, but must also exhibit low resistivity, high resistance to elevated temperature, and compatibility with current fabrication processing [10]. In addition to the above requirements, the SAM must have good adhesion with the silicon or silicon dioxide surface and be able to increase the diffusion barrier to Cu. To prevent diffusion of Cu, it was discovered that molecular chain length and terminal group of the SAM ultimately determine the diffusion barrier height [2]. Longer chain lengths and aromatic ring terminal groups are favorable. SAMs in general are well defined and highly ordered, but only if the molecules can adhere to the substrate [11]. Therefore a standard RCA clean prior to SAM deposition should be performed to remove contaminants and silate the surface. Mitigation of copper diffusion and proof of good surface adhesion of porphyrin-based and silane-based SAMs has been shown by fabrication and testing of MOS capacitor structures and through AFM surface analysis [2] [11] [12] [13] [14]. The SAMs exhibit excellent step coverage and are easily deposited by vapor-phase deposition or by a wet chemical process. SAMs have been shown to be thermally stable up to 700 °C [15]. Metallated SAMs may be of interest due to the electronegativity of the metal ion. A metallated chemistry by definition is simply an organic compound in which a metal ion has been substituted.

Organic SAMs can be characterized by AFM, contact angle measurements, variable-angle spectroscopic ellipsometry (VASE), and capacitance-voltage (C-V) bias-temperature stress (BTS) tests. The contact angle for a SAM film should be high (>60 °) because of its highly ordered morphology causing a hydrophobic nature. The effectiveness of inorganic barriers is typically quantified using the BTS test. Soaking a MOS capacitor under a ±1 MV/cm electric field at a temperature in the range of 200 °C – 250 °C will cause mobile ions in the oxide to drift from the gate to a known position under positive gate bias, and then shift back under a negative gate bias [16]. This allows the mobile ion density to be quantified using (1), where N_m is the mobile ion density, ΔV_{FB} is the maximum change in flat band voltage between the zero stress state to positive stress state and positive stress state to negative stress state, C_{max} is the accumulation capacitance, q is elementary charge, and A is the gate area.

$$N_m = \frac{\Delta V_{FB} C_{\max}}{qA} \tag{1}$$

The BTS method allows mobile ions to be independently quantified from the total oxide charge density which consists of mobile, trapped, oxide fixed, and interface charge. Shift direction is independent of substrate type and only depends on the applied bias [16]. The total oxide charge N_{ss} is found using (2), where C_{ox} is oxide capacitance and φ_{ms} is the metal-semiconductor work function.

$$N_{ss} = \frac{C_{ox}(\varphi_{ms} - V_{FB})}{qA} \tag{2}$$

Only the mobile ion density will be of interest here. An organic SAM using the OHTPP chemistry will first be analyzed. Two inorganic barriers consisting of TiO_2 and Ni will then be characterized using the BTS method.

III. Experimental Procedure

The OHTPP solution was formed by dissolving 5,10,15,20-Tetrakis(4-hydroxyphenyl)-21H,23H-porphine in acetonitrile at 24 °C for a 0.15 mM concentration. Samples of 500 nm thermally grown SiO_2 over n-type <100> Si were either prepared by an RCA clean or a 15 minute piranha clean (20:1 H_2O_2:H_2SO_4) at 125 °C. This particular RCA clean started with a 10 minute bath at 75 °C in a 50:3:3 concentration of H_2O:NH_4OH:H_2O_2 to remove organic contaminants followed by a 5 minute deionized (DI) water bath. A 50:1 H_2O:HF dip at 24 °C for 30 seconds removes any oxide formed from the previous baths then another DI water rinse followed. The second portion of the RCA clean consisted of a 50:3:3 concentration of H_2O:HCl:H_2O_2 at 75 °C for 10 minutes to remove inorganic contaminants followed by a DI water rinse and spin-rinse-dry (SRD). The samples were immersed in the OHTPP SAM solution for 24 hours, then rinsed with acetonitrile, air dried, and stored in a dark container. Analysis by AFM, contact angle, and VASE followed directly afterwards.

Six different MOS capacitor types were then fabricated using new, high grade 6 – 7 Ω-cm Si <100> 6" wafers. One p-type wafer received a 50 nm (measured 47.3 nm ± 0.93 nm) dry thermal oxide growth and one n-type wafer received a 25 nm (measured 23.0 nm ± 1.27 nm) dry thermal oxide growth. Both wafers were coated on the topside with photoresist for gate oxide protection and then the wafers were backside implanted with P31 at respective dose and energy of 2×10^{15} cm^{-2} and 55 keV. The backside oxide was wet etched and the photoresist was then stripped in a hot solvent bath. The wafers were then annealed for 30 minutes at 1000 °C in N_2. The backside contact was completed by thermally evaporating 600nm of Al at 1 μTorr and then sintering for 15 minutes at 450 °C in N_2/H_2 for hydrogen passivation. The n-type wafer received a 60 nm (measured 57.8 nm ± 2.99 nm) Si_3N_4 film deposited by plasma-enhanced chemical vapor deposition (PECVD). Both wafers were then cleaved into quarters to produce a total of eight samples, six of which would be used. Varying gate stacks were then fabricated as shown in Fig. 1.

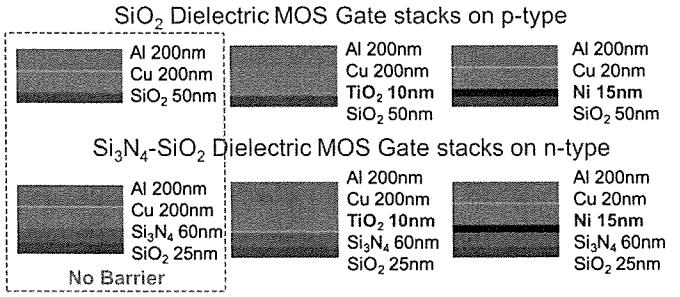

Fig. 1. Schematic of varying MOS capacitor gate stacks fabricated for analysis.

The TiO_2 was deposited by electron-beam evaporation at 0.6 μTorr. The Cu, Ni, and Al were all thermally evaporated at 3 μTorr through a shadow mask to create the MOS gate areas, which is shown in Fig. 2. Film thickness was taken using the tool thickness monitor with well-established tooling factors.

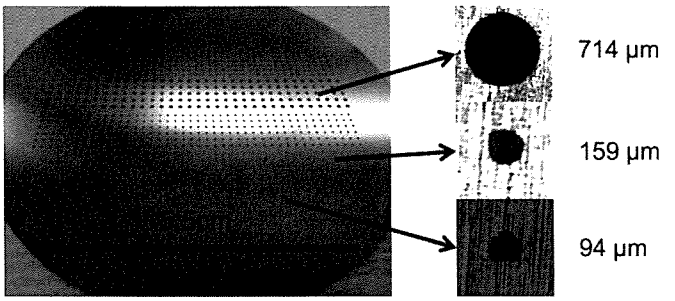

Fig. 2. Stainless steel shadow mask with a 0.005" thickness. The circular integrity of the cuts deteriorated as the diameter decreased, therefore the 714 μm diameter (0.004 cm^2) was chosen for MOS analysis.

BTS C-V testing was carried out using a Materials Development Corporation C-V test station with an HP4284A LCR meter and hot chuck with a dark box. The test signal was maintained at 1 MHz with a 50 mV amplitude. Each sample was measured before the BTS at 24 °C. The temperature was then ramped to 250 °C and the sample was soaked for 5 minutes at that temperature. During the ramp and soak, the sample was biased at 7 V. The sample was then cooled to 35 °C and a C-V plot was taken. The process was then repeated with a -7 V bias. The respective electric fields for 50 nm SiO_2, 10 nm TiO_2 on 50 nm SiO_2, 60 nm Si_3N_4 on 25 nm SiO_2, and 10 nm of TiO_2 on 60 nm Si_3N_4 on 25 nm SiO_2 were found to be, using the measured thicknesses, 1.48 MV/cm, 1.22 MV/cm, 0.87 MV/cm, and 0.77 MV/cm. The capacitor area was verified to be 0.004 cm^2 following evaporation through the shadow mask. Series resistance effects were deducted from the capacitance measurements since a backside contact was used with a 650 μm thick wafer. The p-type and n-type wafers had respective series resistances of 360 Ω and 80 Ω.

IV. Results and Analysis

Initial AFM results of the OHTPP SAM over SiO_2 appear to indicate good adsorption as shown in Fig. 3. However, after repeated processing of other samples following the same deposition process, the results were unable to be replicated as shown in Fig. 4a. An AFM of SiO_2 is shown in Fig. 4b for comparison. The repeated attempts appear to be just SiO_2.

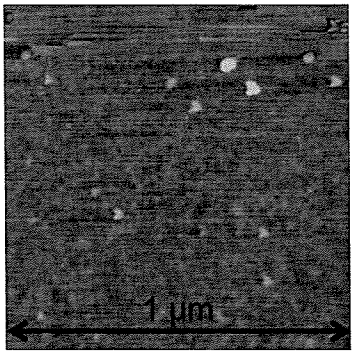

Fig. 3. Initial AFM of OHTPP SAM over 500nm thermally grown SiO_2 on Si appears to indicate that the SAM is present in comparison with other finds [11] [12] [2].

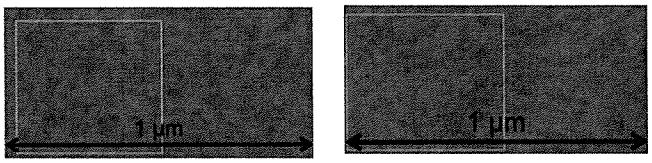

Fig. 4a. (left) AFM of a repeated OHTPP SAM deposition over a new sample of SiO_2 on Si appears to indicate that the SAM did not deposit. 4b (right) shows an AFM of SiO_2 for comparison.

Contact angle measurements reveal that this particular OHTPP SAM was not present over the SiO_2 film as shown in Fig. 5. If the SAM film was present, the contact angles would likely be greater than 60°. The measured contact angles in Fig. 5 appear to be over SiO_2. The piranha clean causes a more hydrophobic surface than the RCA clean, which leaves a dehydrated surface causing higher contact angles over the hydrophilic amorphous SiO_2.

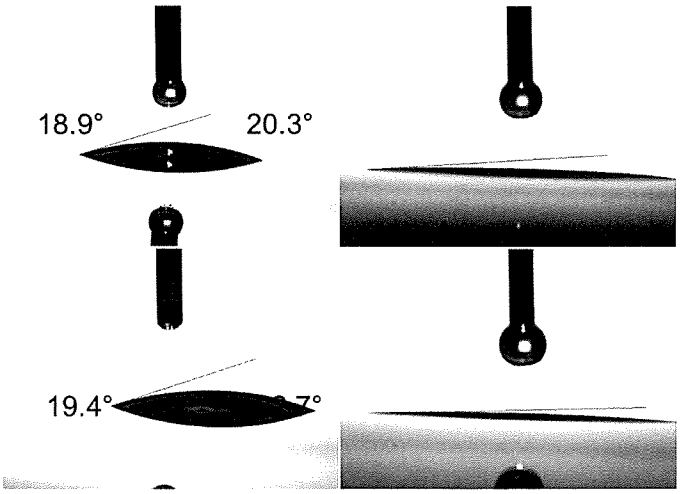

Fig. 5. Contact angle measurements using 1 μL of DI water over SAM and SiO_2 samples with varying cleans. Top left is OHTPP SAM over piranha-cleaned SiO_2. Top right is OHTPP SAM over RCA-cleaned SiO_2. Bottom left is piranha-cleaned SiO_2. Bottom right is RCA-cleaned SiO_2.

VASE measurements using a Woollam HS-190 initially found a 1.492 nm ± 0.0281 nm (mean-squared error (MSE) = 16.45) film present over the SiO_2 using a Cauchy model with coefficients of A = 1.45, B = 0.01 μm^2, and C = 0.00 μm^4, and k = 0. However, a repeated measurement resulted in 0.000 nm

± 0.388 nm (MSE = 186.4). Measurements with a non-zero mean were unable to be obtained again in different sample locations and with different samples using an identical deposition process.

BTS results for the MOS capacitor structures of Fig. 1 are shown in Fig. 6 and Fig. 7. The TiO_2 and Ni samples on p-type Si show large flat band shifts of 15.5 V and 11.8 V respectively. The Cu on SiO_2 on p-type only shifts 2.07 V. Flat band shifting with the Si_3N_4 dielectric is severely mitigated. The TiO2 sample on n-type Si shifts 0.93 V while the Cu and Ni samples shift only 0.09 V and 0.05 V respectively.

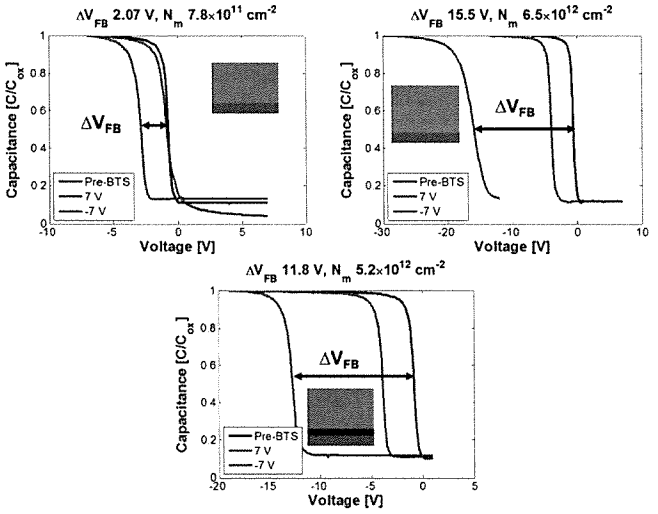

Fig. 6. C-V BTS results of MOS samples on p-type Si. Top left shows the Cu on SiO_2, top right shows the Cu on TiO_2, and bottom shows Ni on SiO_2.

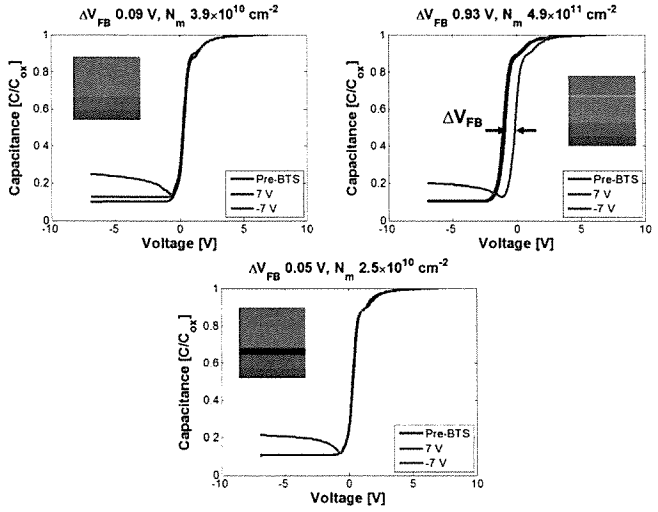

Fig. 7. C-V BTS results of MOS samples on n-type Si. Top left shows the Cu on Si_3N_4, top right shows the Cu on TiO_2, and bottom shows Ni on Si_3N_4.

V. Conclusions

The OHTPP SAM did not successfully adsorb to an SiO_2 surface with the proper preparation and deposition steps. Therefore this particular chemistry would not be ideal to use as a Cu barrier. Other chemistries such as allyltrichlorosilane and trichloro(octadecyl)silane may prove to be more successful than the OHTPP SAM. However, these chemistries pose extreme health hazards and caution would have to be taken during processing. Despite this, the deposition process of organic SAMs is very simplistic and would be ideal to implement for a photovoltaic metallization process.

The BTS results showed that TiO_2 and Ni would be poor choices for a Cu barrier film over SiO_2 due to the high density of mobile ionic contamination present. Possible causes may be ionic interaction with the Cu. However, further analysis with other material combinations should be done to investigate this. Mobile ions were severely hindered over the Si_3N_4 film. Only TiO_2 showed a fairly significant shift. However, it would be feasible to conclude that Cu and Ni could be safely deposited on solar cells over Si_3N_4 while using a conventional NiSi barrier over Si.

Oxide charges may have been reduced with this process flow by performing the gate oxide growth before the Al backside contact rather than as the first step. This would lessen the probability of introducing contaminants and charge. The photoresist used as a topside protectant may have also introduced some injected charge or ionic contamination. An RCA clean was not performed in this process because the wafers were pulled from factory-new box. However, one should ideally be performed directly before the gate oxide is to be grown. The furnace tube should also be cleaned with TransLC to mitigate the possibility of any contamination during oxide growth. Since all wafers were processed with consistency, the flat band shifts and mobile ion densities found from C-V analysis should be considered valid and accurate.

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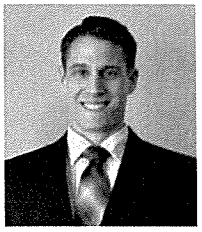

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