Optimization of ALD High-K Dielectrics via C-V Analysis

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Abstract— **As device scaling is an ever present concern in semiconductor manufacturing, the need for thin, conformal films with which to fabricate these devices is paramount. One technology that appears prominently placed to fill this need is Atomic Layer Deposition. This work presents a study on atomic layer deposited alumina (Al_2O_3), hafnia (HfO_2), and silicon dioxide (SiO_2) as dielectric materials characterized using capacitance-voltage (CV) analysis. MOS capacitors were fabricated utilizing various combinations of alumina or hafnia and silicon dioxide as an interfacial layer. Each dielectric film was characterized optically to determine the thickness, and then CV analysis was performed on each device. The results showed that the dielectric and interface quality of Al_2O_3 on bare silicon was superior to HfO_2 on bare silicon. However the performance of Al_2O_3 devices dropped with the addition of interfacial SiO_2, while the performance of the HfO_2 devices was greatly enhanced. The treatment that had HfO_2 with a monolayer of interfacial SiO_2 on silicon produced the best results.**

I. NTRODUCTION

ATOMIC Layer Deposition (ALD) is a thin film deposition method that employs alternate saturative surface reactions to lay down an extremely thin film layer with great precision and uniformity. Developed and introduced as Atomic Layer Epitaxy (ALE) in 1970's in Finland [1], it was originally designed to be used to make thin film electroluminescent flat panel displays. Having successfully fulfilled its purpose in this task due to its high dielectric strength and uniformity, it was soon applied to epitaxial compound semiconductors, but with mixed success; although there has been moderately extensive research performed in the field, it has yet to find its way into commercial applications.

That said, one of the ever present concerns in the semiconductor industry is device scaling, and as the limitations of current process technology start to catch up with the advances, interest in ALD as the next process enhancement is growing.

ALD itself is a conceptually a straightforward process that can, at its simplest, be broken down into four steps: 1) exposure of the first precursor, 2) purge of the reaction chamber, 3) exposure of the second precursor, and 4) purge of the reaction chamber. This process is then repeated until the desired film thickness has been achieved.

The first precursor exposure serves to lay down the primary film that will be exactly one monomolecular layer thick, as only the atoms in contact with the substrate will bond firmly, while the other precursor molecules will be removed by the following purge. Each subsequent exposure reacts with the previous layer, liberating the necessary ligands to produce the desired solid. After that another purge clears all excess molecules away and readies the surface for the next precursor exposure. An example of this process is shown schematically in Fig. 1.

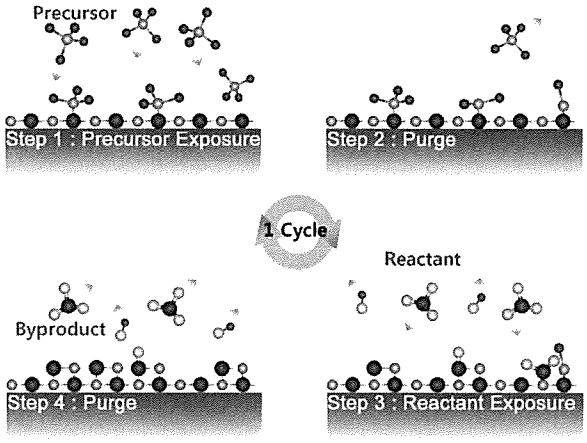

Fig. 1: One cycle of an atomic layer deposition. [2]

Although the process can get significantly more complex depending on the chemistry involved, the advantages of using an ALD system remain relatively constant. The primary advantage obtained from using ALD over other systems is the level of control it provides regarding film thickness. Because the film growth is self-limiting, each deposition will produce exactly the same film thickness. This results in a perfectly linear growth that is dependent solely on the number of deposition

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cycles performed. It should be noted that while the growth rate will always be linear, the rate is determined by the surface density of reactive sites that is produced from the first cycle when the surface is converted from substrate to film.

The other main advantage to a self-limiting process is uniformity. Because there will be a certain number of reactive sites available, once those sites have been filled no more reactions will take place and any excess material will be purged away. That also means that the film growth is not dependent on the amount of precursor exposed; as long as there is enough precursor to saturate all reactive sites the growth will be uniform.

Despite this impressive list of advantages, it is important to note some of the major limitations of ALD as well; primarily time. Because ALD is an iterative process that frequently requires many process cycles, and because the growth rate can be controlled but only to an extent, it can take a prohibitive amount of time to build up the desired film thickness. That said, as devices continue to scale smaller and smaller this becomes less of an issue. As the desired film thickness goes down, so does the time required to grow that thickness, which makes ALD a more and more viable option.

The other main limitation is simply a lack of process refinement for a variety of materials. Because semiconductor manufacturing has evolved to include more than silicon, before any manufacturer would attempt to run an ALD process it must be determined how the fabrication of materials such as compounds or irregular metal layers respond to the ALD process.

II. EXPERIMENTAL SETUP

Rochester Institute of Technology does not presently have an ALD system, but hopefully will in the future, and when that comes about it would be useful to have basic characterizations of some common films from an analogous tool as a starting point. To that end, the goal of this project was to characterize atomic layer deposited alumina, hafnia, and silicon dioxide as dielectric materials through capacitance-voltage (CV) analysis.

Starting with bare, four-inch silicon substrates, five different process splits were conceived: Al_2O_3 on bare silicon, Al_2O_3 with an interfacial SiO2 layer on silicon, HfO_2 on bare silicon, HfO_2 with an interfacial SiO_2 layer on silicon, and HfO_2 with an interfacial monolayer of SiO_2 on silicon.

These five process splits were designed so that the basic single film recipes could provide a comparison between Al_2O_3 and HfO_2 characteristics, while the high-K dielectrics on top of SiO_2 would theoretically demonstrate the benefits of an interfacial layer and how each high-K film responded, and the monolayer SiO_2 film would allow for an examination of the effects of dielectric stack thickness.

All of the dielectric ALD was performed on the University of Rochester Nanolab's Cambridge Savannah 200, with a target thickness for each individual film, except the monolayer, of 100Å.

Before processing continued the dielectric films underwent an optical characterization where they were subjected to a Variable Angle Spectroscopic Ellipsometer (VASE) thickness measurement, which relies on the optical properties of a film to repolarize an incident light ray. By tracking the phase and intensity change between the incident and reflected light ray, these measures can be compared to theoretical models for various film combinations and iteratively optimized to determine the most likely film thicknesses. Fig. 2 shows an example of the phase angle measurements; delta and phi are two variables that are compared to the theoretical models to determine film thickness. Each of the individual films used for this experiments measured between 75Å and 85Å, which is below the target thickness, but acceptable.

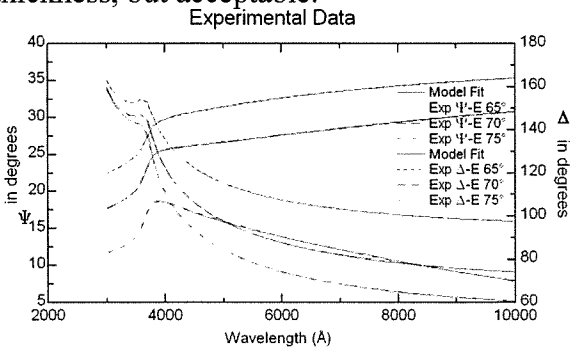

Fig. 2: VASE phase change measurements for Al2O3 on Si.

Once the dielectrics were deposited and optically characterized, roughly 2000Å of aluminum was thermally evaporated to serve as the contact metal, and it was subsequently patterned and etched to define the capacitors.

After fabrication, CV analysis was performed on capacitors from each process split. Multiple

frequencies were tested for each device so that the frequency response could be examined and compared from one device to another.

III. RESULTS

The first set of capacitance measurements compared are Al_2O_3 on bare silicon to Al_2O_3 on silicon with an interfacial SiO_2 layer as shown in Fig. 3 and Fig. 4.

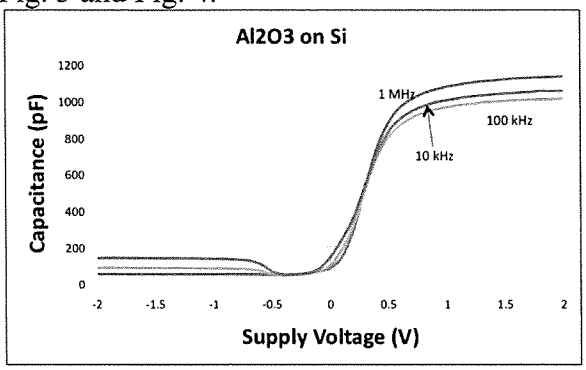

Fig. 3: CV curves for Al_2O_3 on silicon at 1 MHz, 100 kHz, and 10 kHz. Accumulation Capacitances: 1 MHz – 1130 pF, 100 kHz – 1010 pF, 10 kHz – 1050 pF.

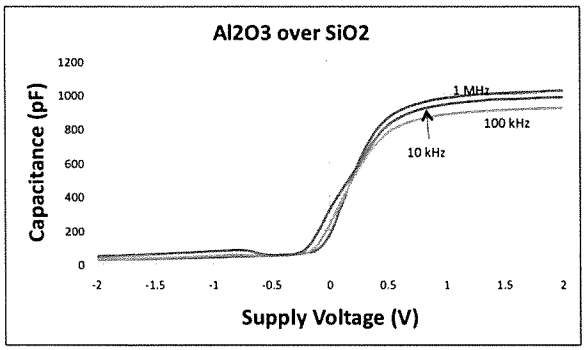

Fig. 4: CV curves for Al_2O_3 with an SiO_2 interfacial layer on silicon at 1 MHz, 100 kHz, and 10 kHz. Accumulation Capacitances: 1 MHz – 1020 pF, 100 kHz – 920 pF, 10 kHz – 985 pF.

Examining these two figures it is apparent that both process splits yielded functioning capacitors with fairly strong characteristics, however at all three frequencies the flatband capacitance was higher for Al_2O_3 on bare silicon than for Al_2O_3 with an interfacial SiO_2 layer. This means that although the interfacial layer may have provided some benefit, it was not significant enough to outweigh the decrease in capacitance that occurred as a result of having a thicker dielectric stack. Further experimentation could include the use of a monolayer of SiO_2 under the Al_2O_3 to get a better idea of how much the interfacial layer is actually boosting performance, if at all.

Fig. 5, Fig. 6, and Fig. 7, below, show the characteristics for each of the HfO_2 process splits at 1 MHz, 100 kHz, and 10 kHz.

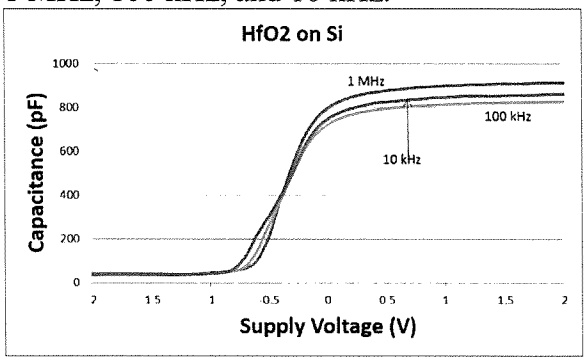

Fig. 5: CV curves for HfO_2 on silicon at 1 MHz, 100 kHz, and 10 kHz. Accumulation Capacitances: 1 MHz – 912 pF, 100 kHz – 862 pF, 10 kHz – 827 pF.

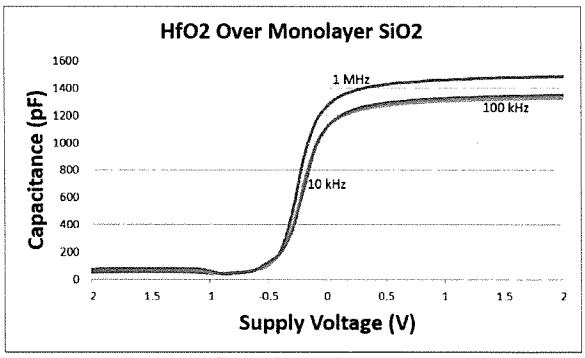

Fig. 6: CV curves for HfO_2 with a monolayer SiO_2 interfacial layer on silicon at 1 MHz, 100 kHz, and 10 kHz. Accumulation Capacitances: 1 MHz – 1490 pF, 100 kHz – 1330 pF, 10 kHz – 1350 pF.

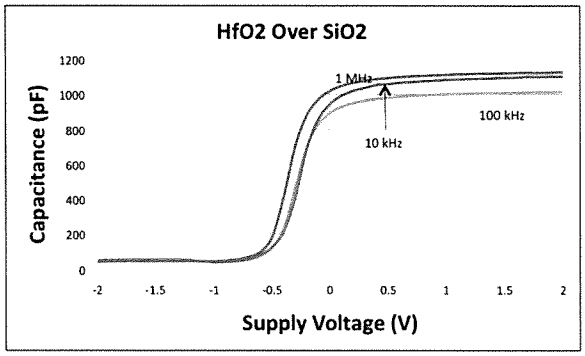

Fig. 7: CV curves for HfO_2 with an SiO_2 interfacial layer on silicon at 1 MHz, 100 kHz, and 10 kHz. Accumulation Capacitances: 1 MHz – 1130 pF, 100 kHz – 1010 pF, 10 kHz – 1100 pF.

In the HfO_2 process splits it is again apparent that all devices were operational, however in comparing HfO_2 on bare silicon to HfO_2 over an interfacial oxide, the inverse of the trend noted with Al_2O_3 is

apparent; where in Al_2O_3 the capacitance decreased when an interfacial oxide was added due to the increase in thickness, in HfO_2 the benefits of the interfacial layer appear to be more significant as the capacitance increases fairly significantly when an interfacial SiO_2 layer is added.

The next comparison to note is between Fig. 6 and Fig. 7. Here the effects of a monolayer interfacial layer are compared to the effects of a full ~80Å interfacial layer, and as predicted the monolayer maintains the benefits of an interfacial layer but cuts down on the dielectric stack thickness which further increases the flatband capacitance.

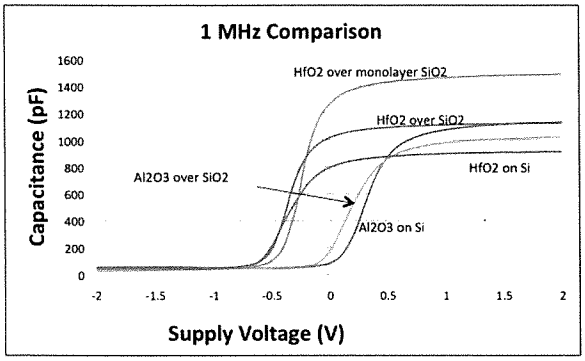

Fig. 8: CV curves for each process split at 1 MHz frequency. Accumulation Capacitances: Al2O3 on Si – 1130 pF, Al2O3 over SiO2 – 1020 pF, HfO2 on Si – 912 pF, HfO2 over ML SiO2 – 1490 pF, HfO2 over SiO2 – 1130 pF.

Fig. 8 is a comparison of one device from each process split tested at 1 MHz frequency, which allows for a comparison between the Al_2O_3 based devices and the HfO_2 based devices.

Not surprisingly as HfO_2 is known to have interfacing issues with silicon, the basic Al2O3 on bare silicon device outperformed the HfO_2 on silicon device by more than 200 pF. However where this basic process split was the highest performing for Al_2O_3, it was the lowest performing HfO_2 process. So as an interfacial SiO2 layer was added the accumulation capacitance of the Al_2O_3 device dropped by 110 pF while the HfO_2 device's accumulation capacitance rose by 218 pF, and reducing the dielectric stack thickness by using a monolayer interfacial oxide boosted the accumulation capacitance by another 360 pF.

IV. CONCLUSIONS

With the goal of providing a base characterization for the main high-K dielectric ALD films, this project proved very successful as each dielectric film yielded functioning devices that demonstrated predicted behavior.

If the option is between a single Al_2O_3 film and a single HfO_2 film the Al_2O_3 outperformed the HfO_2 due to the issues that HfO_2 has interfacing with bare silicon. However if an interfacial oxide is process permissible, in the case of HfO_2 it was determined that the benefits of having an interfacial SiO_2 film outweighed the drawbacks of having a thicker dielectric stack but the capacitance was greatly dependent on the thickness of the SiO_2 layer, so utilizing a monolayer of SiO_2 could further improve the results. In the case of Al_2O_3, adding an interfacial oxide actually decreased performance, but it is conceivable that if the interfacial layer were thinner it could be beneficial to the process.

Further experimentation would include the use of a monolayer interfacial oxide in the Al_2O_3 process, as well as further experimentation into stacks using both Al_2O_3 and HfO_2 along with other high-K dielectrics. However for the time being this examination will provide a solid starting point for anyone interested in enhancing or building a process with thin film ALD.

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