Power Reduction in a Microprocessor (May 2010)

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Abstract—**The concept of power reduction is a growing concern in IC design. This article contains the steps taken to redsign a 4-bit microprocessor for lower dynamic power. Measurements are performed of initial power and power consumption after applying new designs. The major reductions for this μP come in the form or logic reduction, transistor stacking, pulse generated latches and width reductions and modifications. Overall the outcome shows a significant amount of energy reduced and the project successfully explored power consumption considerations.**

Index Terms—**Netlist, Flip-Flop, Microcontroller, Microprocessor**

I. Introduction

THE past decade contains changes to many areas of consumer electronics. During those years power management has become an increasingly important factor. Demand increases for higher performance and longer battery life. Power consumption of servers and electrical overhead for companies is becoming a sizable factor in a lean focused business world. As these aspects grow in importance, device density is also rising and with it the temperature density. The understanding and implementation of power reduction techniques can provide an edge for product and design engineers and show a fusion of microelectronic, electrical, and computer engineering. The two main aspects of power reduction are static and dynamic. This project focuses on the later. It analyzes the dynamic power consumption of each circuit in a 4-bit microprocessor (μP). It explores some of the most popular techniques of power reduction, and then implements select techniques on the 4-bit μP for optimum efficiency. This processor is taught in RIT's VLSI design course as an introduction to processor architecture and is presently being fabricated by RIT's graduate students.

II. Theory

A. Dynamic Power

The fundamental idea behind dynamic power reduction is to minimize switching activity power. A diagram of a CMOS inverter is shown in Figure 1 with the upper rail to ground path highlighted. In terms of switching activity power all CMOS logic gates behave similarly to the inverter; when the output changes a momentary connection between the upper rail and ground is established. Some techniques to reduce this switching power are clock gating [3] [6] [8], voltage rail reduction [2] [7], width scaling [2] [7] [9] [10] [11], and logic minimization [2] [4] [5] [12]. After analyzing components of the μP a few of these techniques are not very effective. The 4-bit μP already utilized a form of clock gating instead of feedback loops which would have consumed more power. The symmetry of most sub-circuits limits the advantage of width scaling on non-critical paths. This similarly applies to power scaling, as power would be reduced on small width transistors. This conclusion guided the project towards other areas.

B. Logic Minimization

In most μPs the control unit is a well established area of high power consumption. Figure 2a shows a piece of the original PLA design of the μController. The majority of power consumption of RIT's μP is from the microcontroller (μC). The original design was a PLA using over 475 transistors.

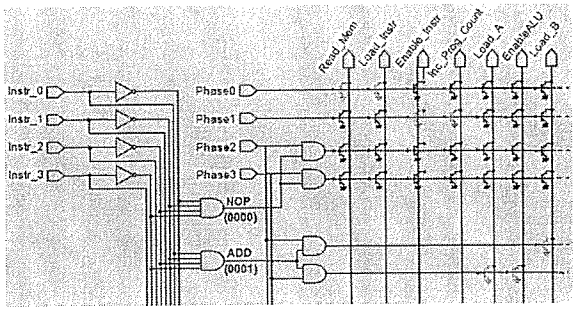

Fig. 2a Schematic diagram of a μC done using a PLA, more than 475 transistors.

Figure 2b shows a portion of the low power μC using just under 180 transistors [12]. This design is based off of a hardwired design. The second largest area of power consumption lies in the flip-flops (FFs) of the μP.

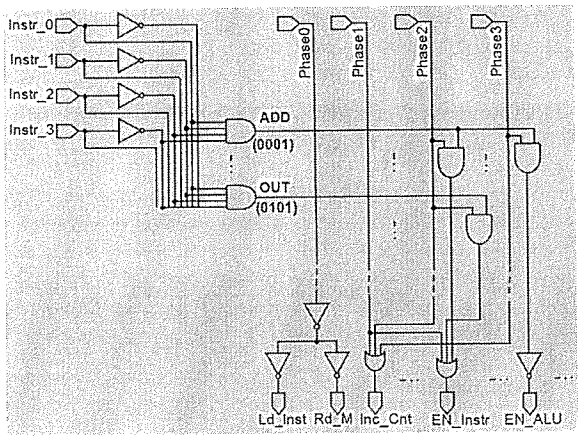

Fig. 2b Schematic diagram of a μC done using hardwired logic, less than 180 transistors.

Figure 3a shows a diagram of a transmission gate flip-flop which is the original design for the registers [1]. The FF is the building block for all the sub-circuits of the μP, therefore minimizations here are multiplied throughout the whole processor.

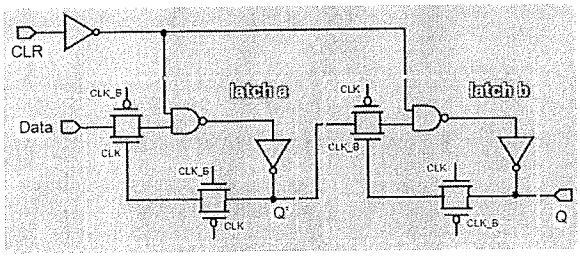

Fig. 3a Schematic diagram of a transmission gated flip-flop.

Figure 3b is a low power FF with a redesigned latch [4]. Fig 3a requires two latches for a FF and 8 latches for a 4-bit accumulator while Fig 3b uses one pulse generator and 4 latches for the 4-bit accumulator.

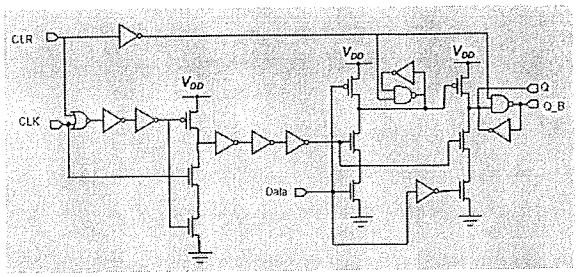

Fig. 3b Schematic diagram of a single edge triggered flip-flop.

The reason why this latch design uses lower power is because of the two NMOS gates on the pull down network. This is called transistor stacking and is a well known technique for power reduction. The idea behind it lies in the C_{int} which is located between the two NMOS that gets charges to a voltage just above ground. This raises the Vs for the 2nd NMOS transistor causing Vsb to be large which in tale increases the Vt of that 2nd NMOS meaning lower power consumption. It also minimizes DIBL because one of the NMOS has a very small Vds across it and therefore less DIBL while the other NMOS has much more Vds but less than if it were the only transistor in the pull down network.

III. Data Collection

In order to collect this data the schematics in Mentor Graphics had to be converted into some format that would allow them to be used on the Synopsys tools. This was a large drawback and it took a while to figure out that netlists would be the best way. The Synopsys program being used is called Nanosim. This program is used to test many aspects of a circuit including the power consumed, both static and dynamic. It required a netlist and model file. The model file used came from Arizona State University and it was 180nm. That was the largest I could get on the ASU website. The original plan was to use Fuller's model files but at the start of the project there were so many unknowns and such large difficulty with netlists that anything to make the project work smoother was welcomed.

Creating the netlists was difficult. The problem was that the netlist that was created using a combined version of Design Architecture and IC Station was not able to fill in all the transistor sizings when it made the netlist. This meant that not only did transistor names have to be changed from CMOSP to PMOS but the W and L sizings were not present. This meant that knowledge of exactly what the schematic had in it was extremely necessary. For larger files this became a huge drawback since small errors could lead to unknown functionality and the modifications were very time consuming. Ideally the combined version of DA and IC station would be able to create the netlist and it could be directly tested in Nanosim within 2 minutes. There were also a few modifications that all netlists will need which were the instructions for Nanosim, telling it what parameters to test.

Another time consuming piece was the creation of the vector files which required putting in every single input with the clock and not overlapping signals on their edges to avoid strange occurrences. The vector files had to be kept the same for testing the low power and regular designs because dynamic power is strongly related to switching activity which will change when the μP does different tasks. Pearson's test for the μP was used to analyze the power consumed by all of the sub-circuits. The whole analog simulation of the entire μP as a one unit was not performed.

IV. Results

The power analyses were done using Nanosim, a Synopsys tool. Difficulty was faced when migrating circuit designs between Mentor Graphics and Synopsys. The model file used is from Arizona State University [13]. It is a 180nm model file and therefore has more dynamic than static power. If a model file in the sub 100nm region were applied static power reduction techniques would have been important, like power gating.

There was a large mistake that had to be corrected in the project the weekend before it was due. The sizing for the transistors was off for the original design meaning it consumed more power than it actually did if sized correctly. This lead to the assumption that the low power latch was better than it actually was.

After resizing the original design new values were obtained and it was realized that the Transmission Gated FF is one of the most low power designs out there. The sizing of the rising edge pulse triggered FF was using up much more power when using the 2.5:1 sizing for PMOS widths to NMOS widths. Later on it was noticed that changing the transistor widths in the latch made significant reductions to the dynamic power. It was determined that the widths were not large enough to charge the 100fF output loads on the device and therefore were spending too much time in transition which is where dynamic power consumption comes from.

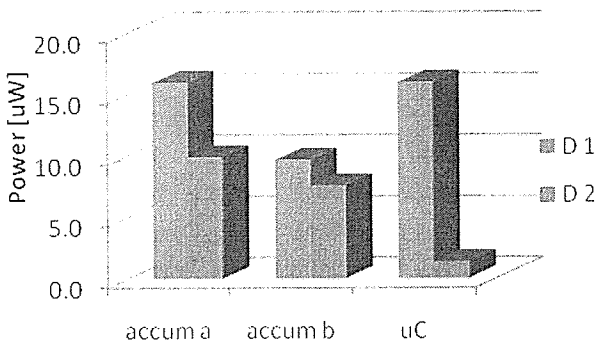

Fig. 4 Graph comparing select initial and low power results. Design 1 = initial, design 2 = low power.

As depicted in Figure 4, there is significant difference in the dynamic power (P_{dyn}) results of the original 4-bit μP. Overall the new designs for the 4-bit microcontroller consumed less dynamic power. Although many of the well known power techniques were not efficiently effective and therefore not used, logic minimization was strongly effective and lead to a deeper understanding of circuit level analysis. The project was able to bring together backgrounds in microelectronic, electrical and computer engineering for a common interest of μP power reduction.

V. Conclusion

The project was a fantastic opportunity to learn more about circuits and experience the application of low power techniques. Although only two main power reduction techniques were used the reduced power logic circuits contained power reduction techniques in them like the stacking that was in the latch. There were initial rough times when learning how to create netlists and vector files and learning about the major effects of sizing the transistors, but after this a smooth understanding of the design was obtained. Even so, this project only touched upon the tip of the iceberg for μP design with low power considerations.

Acknowledgment

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