Fabrication of Fully Isolated nFETs using Oxidized Porous Silicon

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Abstract—**SOI (Silicon on Insulator) technology is an option in improving device performance as smaller devices run into scaling challenges. The devices for this study were fabricated using a FIPOS (Fully Isolated Porous Oxidized Silicon) process, which results in localized SOI active regions. The oxidation of electrochemically etched porous silicon (PSi) has demonstrated success in the formation of device quality localized SOI for CMOS applications [1,2]. The formation of PSi can be done selectively by controlling the Fermi level in areas to be etched or not etched, which is typically done by adjusting the level of doping [1]. An alternative method is to introduce a reversible donor species such as protons [2] or fluorine (this work) for the selective formation of islands of crystalline silicon surrounded by porous silicon. Implanted fluorine in silicon has demonstrated a donor effect upon annealing at low temperature (600°C), which is reversible as the fluorine outdiffuses during higher temperature annealing (1000°C). This technique has been used to form crystalline silicon active regions with thickness less than 200 nm completely surrounded by oxidized porous silicon [3], shown in figure 2. This study involves the fabrication and characterization of nFETs on the active areas to investigate the electronic integrity of the silicon device regions.**

Index Terms—Insulator, porous, fluorine, electrochemical.

I. Introduction

THE basic FIPOS process flow is illustrated in figure 1. A thin screen oxide (50 nm) was grown on p-type 5-10 Ω-cm starting substrates, and a low-dose high-energy boron implant was done to produce a higher concentration buried layer for SOI thickness control. This buried layer was activated at high temperature (1000 °C). The screen oxide was then replaced with a silicon nitride layer deposited via LPCVD, followed by a high-dose fluorine implant. Active lithography (clear-field) was done to pattern the nitride layer, and a high dose boron implant was done in the isolation regions. The nitride was etched via RIE, and the photoresist was removed. An anneal was then done at 600 °C in N_2 for 2 hrs which restored the silicon lattice, resulting in fluorine-rich active areas and nearly full activation of the boron in the p+ isolation regions due to the fluorine preamorphization [4]. Electrochemical etching was then done to form porous silicon over the interconnected p-type regions, using a 4:1 HF:IPA mixture and a constant current density of 10mA/cm^2 for 10 minutes. Leaving the wafers in the HF-electrolyte for an additional 2 minutes ensured complete removal of the nitride masking layer. A multi-step thermal process was then performed: 300 °C for 1 hr in O_2; 1000 °C for 1 hr in O_2; and 1100 °C for 4 hr in N_2. This process completely oxidized the PSi regions, and restored the crystalline silicon islands back to the original p-type and resistivity.

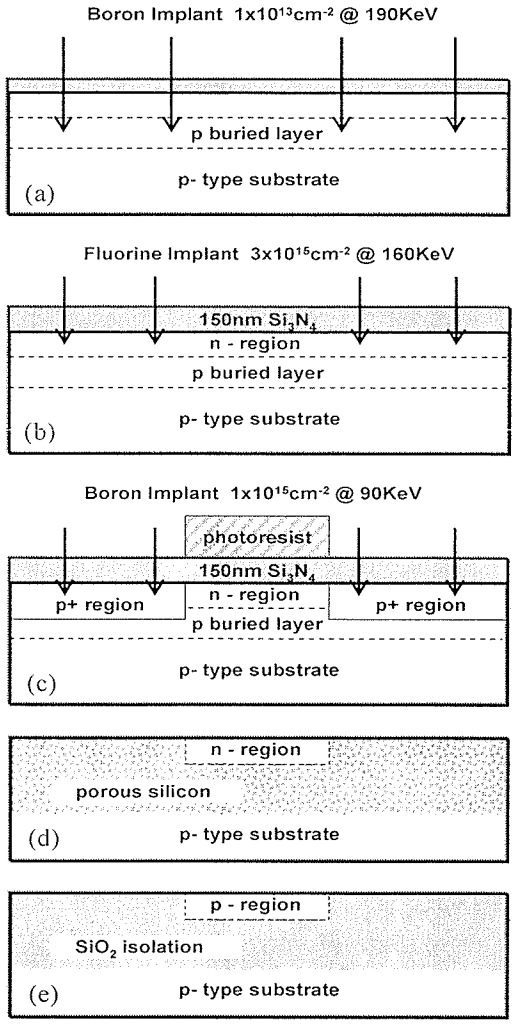


Figure 1. Process sequence for the fabrication of fully isolated crystalline regions, using fluorine for suppression of electrochemical formation of Psi.

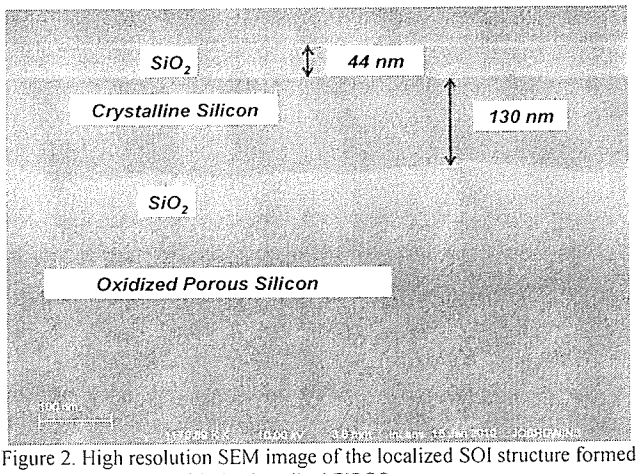


Figure 2. High resolution SEM image of the localized SOI structure formed with the described F!POS process.

II. EXPERIMENTAL

This work involved certain modifications of the process in order to investigate the influence of electrochemical etching parameters and oxidation annealing conditions, and to overcome integration challenges. A backside p+ implant of $1x10^{15}cm^{-2}$ $^{11}B^{+}$ was done for the electrode contact for the anodization process. Aluminum was also deposited on the backside ensuring an ohmic contact. The pattern transfer for the localized SOI needed modifications to ensure a planar surface topology. This involved an oxide layer over the masking nitride, and a wet nitride etch using hot phosphoric acid. Anodization was done using current densities of $10mA/cm^2$, $15mA/cm^2$, and a two-step combination of $5/10mA/cm^2$. The oxidation-anneal was done at final anneal temperatures of 1100 °C and 1150°C.

III. RESULTS AND DISCUSSION

The oxide-nitride masking layer and wet nitride etch was successful in transferring the active region pattern from the oxide to the nitride for the anodization process. The backside B^{+} implant for the electrode contact and the backside aluminum for an ohmic contact ensured a well defined active mesa (Figure 3).

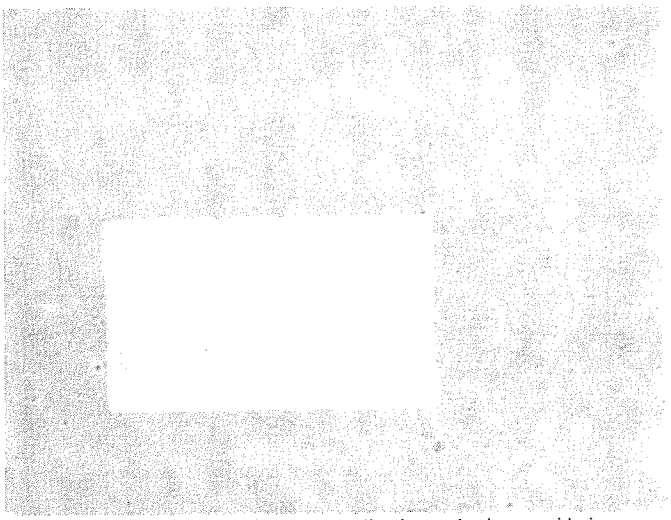


Figure 3. Silicon active region post anodization and prior to oxidation.

Following oxidation (Figure 4) a standard thin film transistor fabrication process was followed, resulting in finished transistors for testing (Figure 5).

Figure 4. Silicon active region post oxidation.

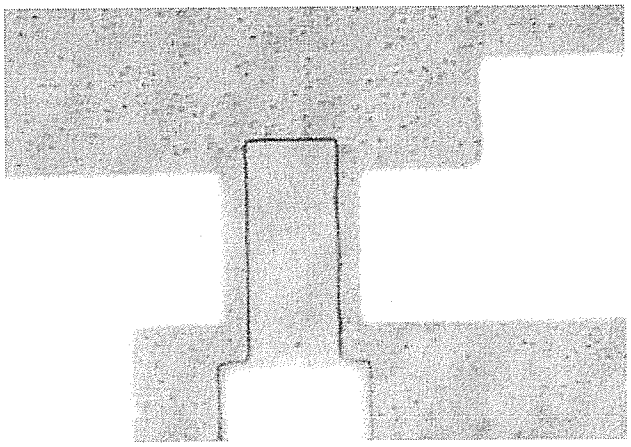
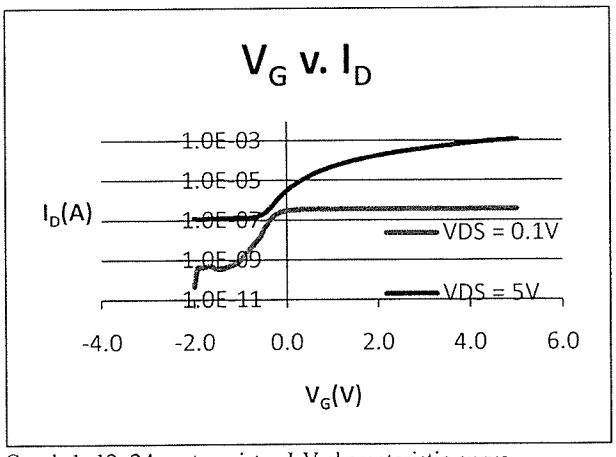


Figure 5. Finished 12x24µm transistor.

Visually the devices looked fine. Electrical testing showed that while there were a number of functioning devices, their performance was sub standard. The contacts were not fully etched, causing the drain current to cut off as the gate voltage was increased. The junctions were leaky, as the gate could not turn the device off (Graph 1).



Graph 1. 12x24µm transistor I-V characteristic curve.

IV. CONCLUSION

The process modifications made resulted in well defined silicon mesas. Functioning devices were fabricated, though their performance was not the best. Further studies will investigate process adjustments to reduce the number of implant steps, as well as different anodization settings.

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