# Scaling of Si/SiGe Resonant Interband Tunnel Diodes (May 2010)

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*Abstract*—**Resonant Interband Tunnel Diodes (RITD) with device sizes ranging from r=20μm to r=50nm (mask defined radii) were manufactured using an e-beam lithography and dry-etch process. The peak to valley current-ratio (PVCR) and peak current density ($J_{peak}$) of the devices were measured. The devices showed high series resistance, and currents and PVCR did not scale in a predictable pattern.**

*Index Terms*—**Esaki, Resonant Interband Tunnel Diodes, Scaling, Tunnel Diodes, Peak Current, PVCR**

## I. Introduction

THE tunnel diode was discovered by Leo Esaki in 1958. Since then the primary interest in industry has been the construction of tunneling field effect transistors (TFET), but if such devices are to be produced their size scaling properties need to be studied. A RITD is a simpler device than the TFET that can be scaled more easily in the lab. The interesting characteristic of such devices are that for some range of voltages, they show a negative differential resistance (NDR). The performance of these devices is characterized by their NDR, PVCR and $J_{peak}$. Several devices with mask defined radii ranging from 20μm to 50nm were produced using an e-beam lift-off lithography process, and dry-etching. The device areas were characterized using SEM imaging. Finally, the electrical characteristics of the devices were measured using a semiconductor parameter analyzer.

## II. Theory

RITDs work on the principle of quantum-mechanical tunneling. Briefly, quantum-mechanical theory states that electrons have both wave-like and particle-like characteristics. The wave-like properties of the electron allow it to tunnel through a thin potential barrier, as long as there are allowed states on the other side (i.e. the solution to the wave equation has a real part on both sides of the barrier). In an Esaki Tunnel Diode the p- and n- sides of the diodes are degenerately doped, and the Fermi levels are in the allowed band-states. The doping is engineered such that electrons in the conduction band are nearly aligned with available states in the valence band. The potential barrier is narrow (on the order of ~10nm). When a bias is applied to the device, more electrons from the conduction band start lining up with available states in the valence band, and tunneling current increases. Eventually, the electrons in the conduction band move past the available states in the valence band and the tunneling current decreases with increasing bias. This is the region where the IV curve exhibits NDR. When the conduction band edge moves past the valence band edge, no more tunneling can occur and the device starts behaving like a traditional diode.

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**Figure 1 Band diagram under zero bias**

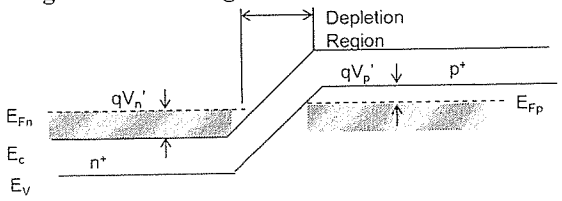



**Figure 2 Band diagram with increasing bias and increasing tunnel current**

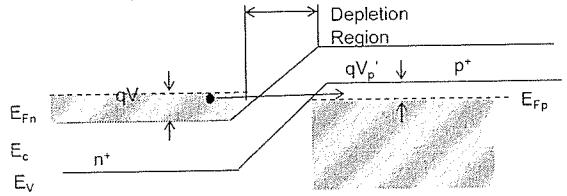
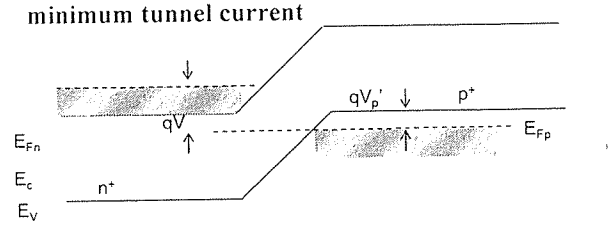



**Figure 3 Band diagram with increasing bias and minimum tunnel current**




## III. Procedure

Figure 6 illustrates the schematic diagram of the RITD structures investigated in this study. The intrinsic layer between the delta-doped planes consists of X nm of undoped Si and Y nm of undoped SiGe. The structure was previously fabricated using low temperature molecular beam epitaxy. The device was annealed at 800°C for 1 min on an AGC610 RTP furnace. Following anneal, a 2 resist-layer liftoff lithography process was performed. A layer of (nonphotosensitive) LOR5A was first deposited on the substrate. A layer of (photosensitive) PMMA was deposited on top of this. E-beam lithography using an Amray 1830 SEM and Nanoscale Pattern Generation Software (NPGS) was performed to create patterns

from 20μm to 50nm. 500nm of aluminum was evaporated on top of the PMMA. Following metal deposition, the pattern was developed in remover-PG, leaving aluminum circles of desired radii in the unexposed areas (liftoff process). The devices were then etched using a dry-etch process in a Trion etcher for 60 sec at a base pressure 68 mTorr, at 122W, and $O_2$:$CF_4$:$CHF_2$ flows of 5:20:40 sccm respectively. The metal stack acted as an etch-mask during the etch, creating the mesa structure shown in Figure 5. Since the mesa structure determined the final geometry of the device, SEM analysis was performed to determine the areas of the mesas. Following etch, 2000nm of BCB was deposited using a spin-on and etch-back process. The BCB served as an interlayer dielectric and planarizing layer. Following BCB deposition, a second aluminum metal layer was patterned using a liftoff process similar to that described above. The purpose of the second metal layer was to create large circular contacts to the (metal 1) layer below for easier probing.

**Figure 4 Device structure**

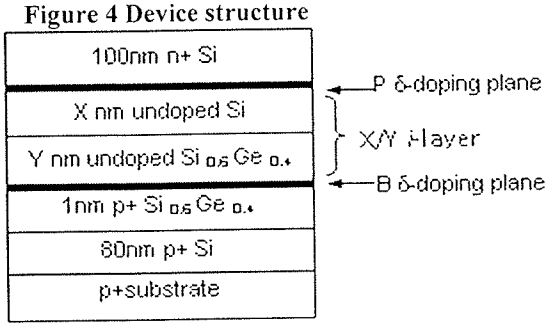



**Figure 5 Mesa**

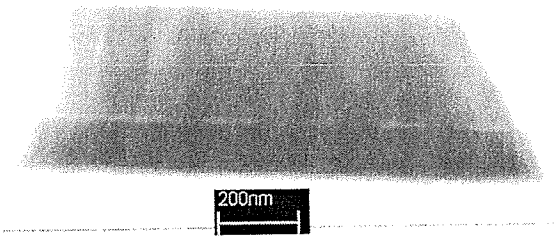
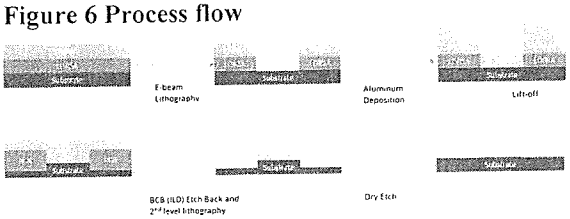



**Figure 6 Process flow**




## IV. Results/Analysis

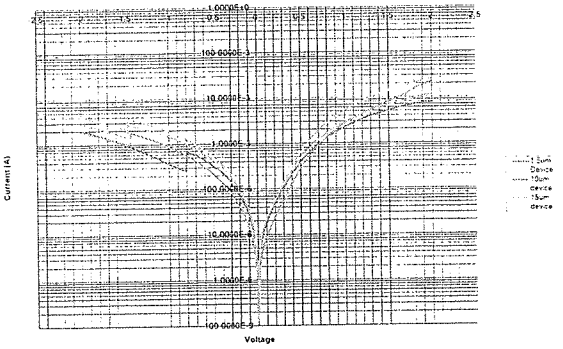
The etch performed after the Metal 1 lift-off process defined the geometry of the device. The mesa structure formed during this etch was examined under a SEM microscope and the device areas were characterized using the ImageJ program. Table 1 lists the junction areas of the devices.

**Table 1 Junction Areas**

| Masked Defined Radius (nm) | Masked defined Area ($nm^2$) | Actual Area ($nm^2$) |
|---|---|---|
| $20.0x10^3$ | $1256.64x10^6$ | $1087.02x10^6$ |
| $15.0x10^3$ | $706.86x10^6$ | 654.25x106 |
| $10.0x10^3$ | $314.16x10^6$ | 319.67x106 |
| $5.0x10^3$ | $78.54x10^6$ | 76.97x106 |
| $2.5x10^3$ | $19.63x10^6$ | 19.39x106 |
| $2.0x10^3$ | $12.57x10^6$ | |
| $1.5x10^3$ | $07.07x10^6$ | $6.77x10^6$ |
| $1.5x10^3$ | $07.07x10^6$ | $6.65x10^6$ |
| $1.0x10^3$ | $03.14x10^6$ | $3.98x10^6$ |
| $1.0x10^3$ | $03.14x10^6$ | $3.42x10^6$ |
| 900.0 | $02.54x10^6$ | $3.40x10^6$ |
| 800.0 | $02.01x10^6$ | $2.41x10^6$ |
| 700.0 | $01.54x10^6$ | $1.96x10^6$ |
| 600.0 | $01.13x10^6$ | $1.39x10^6$ |
| 500.0 | $7.85x10^5$ | $1.08x10^6$ |
| 450.0 | $6.36x10^5$ | $9.60x10^5$ |
| 400.0 | $5.03x10^5$ | $8.16x10^5$ |
| 350.0 | $3.85x10^5$ | $5.52x10^5$ |
| 300.0 | $2.83x10^5$ | $5.00x10^5$ |
| 250.0 | $1.96x10^5$ | $4.88x10^5$ |
| 200.0 | $1.26x10^5$ | $4.52x10^5$ |
| 150.0 | $7.07x10^4$ | $2.15x10^5$ |
| 100.0 | $3.14x10^4$ | $1.49x10^5$ |

Following SEM imaging, large devices were probed using a Keithly 4200 parameter analyzer.

**Figure 7 IV Characteristics post Metal 1**




The devices showed large series resistance. It is likely that native oxide formed on the Si during the anneal and lift-off process which is causing the increased series resistance. The devices do exhibit peak and valley currents, which suggests that tunneling phenomenon is taking place.

Following fabrication, all devices were tested using the Keithly 4200 Parameter Analyzer. Small devices failed to produce any IV characteristics at all, and large devices showed large hysteresis during forward and backward voltage sweeps and no discernible pattern in terms of current scaling/current density. Since no small devices yielded testable parts, and the IV curves of the larger devices were suspect, SEM cross-sectioning was performed on the devices. The cross-sections revealed that both Metal 1 and Metal 2 showed a considerable degree of peeling/warping and that BCB had migrated between the layers.

**Figure 8 Cross-section of completed device**

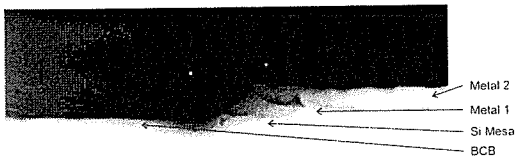
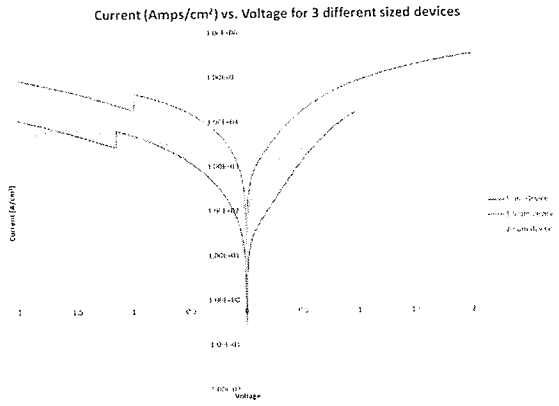




**Figure 9 IV Characteristic post Metal 2**




## V. Conclusion

A lift-off e-beam lithography and etch process was demonstrated that was able to produce physical devices with radii of around ~50nm. However, electrical testing showed that devices were not functional. Further failure analysis is needed to study why there is high series resistance post Metal 1 and why small devices did not yield at all.

## VI. References

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