MEMS Multi-Actuated Bridge Switch

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Abstract

A MEMS multi-actuated bridge switch is developed and created using the RIT sub-micron CMOS process as a way to create a high speed switch with good isolation, power consumption and low loss. The bridge was imaged using a SEM before and after the bridge release. Not much difference could be seen, prompting further investigation. There was a suspicious looking bump in the middle of the bridge that led us to believe that the TEOS sacrificial layer was buried underneath polysilicon. A cross-cut of the bridge was done where the bumps could be seen transversally. A highlight etch was done, confirming our suspicions that the mystery layer was TEOS.

During processing we realized that the mask for the sacrificial TEOS layer was the inverse polarity of what was needed. The TEOS layer width was also designed too thin, which made the etching process remove too much and making further steps overlap. Recreating this layer with a wider sacrificial TEOS and the correct polarity successfully managed to get the bridge to release. Further work would involve completing the switch and electrical testing now that the bridge release has been proven.

Key Words: analog, electrostatic, thermostatic

1. Introduction

The recent explosion in wireless communications has created a need for ultra-low loss switches. MEMS switches can offer a substantially higher performance than FET switches (isolation, power consumption, loss) with few drawbacks (switching speed, size).

A multi-actuated MEMS switch can correct some of these drawbacks. The combination of thermostatics and electrostatics helps keep the device low-power, while accelerating the switching mechanism when both actuators are on. Power consumption can be lowered even more by turning off the thermostatics and letting the electrostatics hold the switch in an on position.

2. Process

The design was created using the RIT sub-micron CMOS process. The thermostatics on top of the bridge would heat up, making the bridge sag, and lowering the gap between the electrostatics. These would then hold the bridge down, making contact and passing a signal through.

Figure 1 shows the top view of the bridge switch created. N+ implants are done to create the heaters, the electrostatics, and the signal lines. Figure 2 shows a side view of the bridge, detailing the placement of the electrostatic dielectric. The bridge was designed to be 100um in length, 10um wide, and about 1.2um in height.

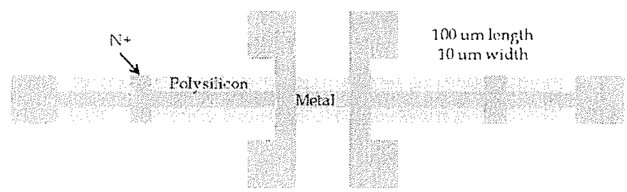

Figure 1 – Top View

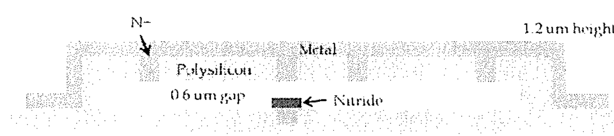

Figure 2 – Side View

The process designed starts with implanting a high dose of N+ on polysilicon layer to act as the bottom electrostatics and an extension for the signal line so the top section can make contact when the bridge sags down. Polysilicon is deposit on top of that, then etched away down to the implanted sections to create the bridge supports. The dielectric for the electrostatics is then deposit, nitride in this case, and etched to the desired shape. The sacrificial TEOS layer is deposit on top of this, and then etched back to reveal the polysilicon bridge supports. Another layer of polysilicon is put down to create the bridge. This is then implanted with another high dose of N+ to create the heaters, electrostatic, and signal

line on the top. Finally, the TEOS layer is etched away using a wet etch process to etch underneath the bridge, and the Al metal layer is put down.

3. Results

Towards the end of the process, before releasing the bridge, one of the wafers was selected to be cleaved and analyzed. This consists of SEM imaging to figure out if the bridge was shaped correctly, and if the bridge releases during the wet etching. Figure 3 shows the SEM image of the bridge pre-release. A suspicious bump can be seen running down the middle of the bridge. Figure 4 shows an image of the bridge after a 10 minute etch. We can see the top implants clearly, and the nitride layer poking out from underneath. There is also a shadowing of the suspicious bump running down the middle of the bridge.

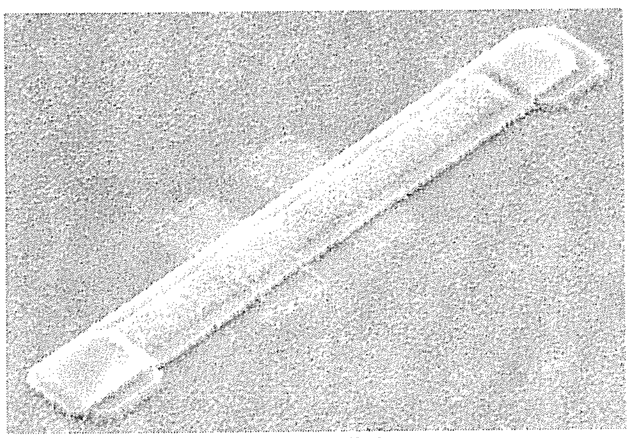

Figure 3 - Pre-Release

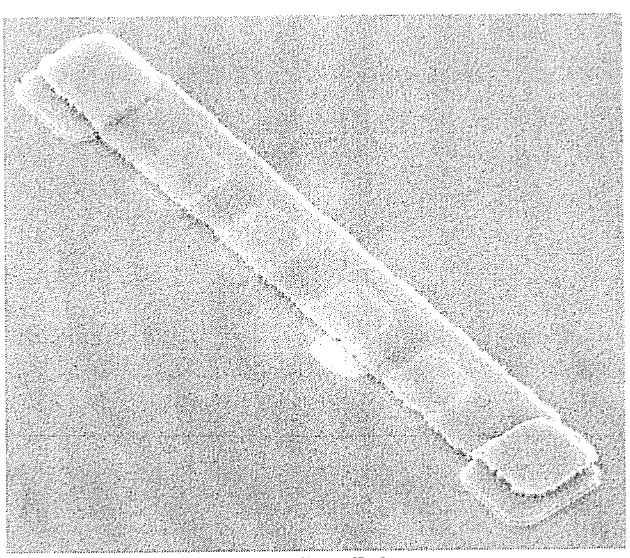

Figure 4 - Post-Release

A lateral image was done to find out if the bridge actually released, seen in Figure 5. Zooming in, Figure 6, shows no release, with the suspicious bump clearly shown.

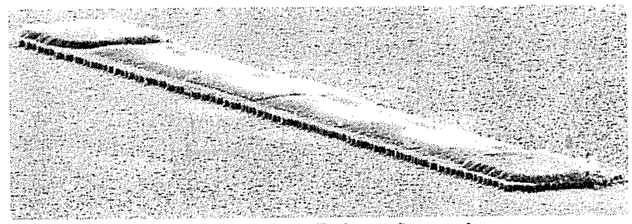

Figure 5 - Post-Release Lateral

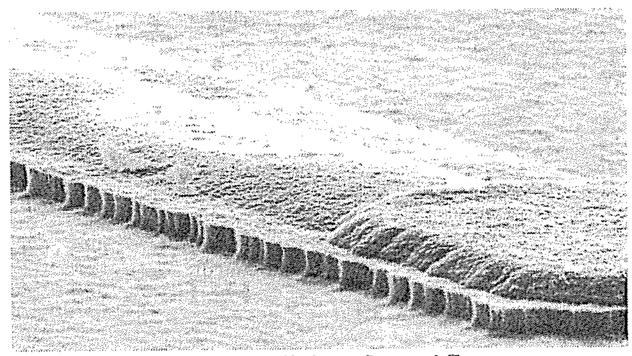

Figure 6 - Post-Release Lateral Zoom

4. Failure Analysis

The suspicious bump seen on the bridge in Figure 6 looked to be in place of where the TEOS should be. To test and confirm suspicions, cross-cuts of a bridge were taken. Figure 7 shows a cross cut before a highlight etch. There is a clear marking around the area that seems to bump up. A highlight etch was performed, creating a void in the area, as seen in Figure 8, and confirming the suspicions of the bump being a buried layer of TEOS.

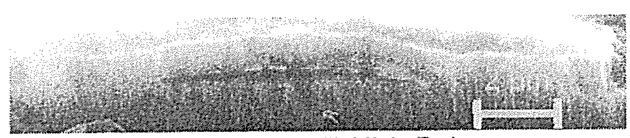

Figure 7 - Pre-Highlight Etch

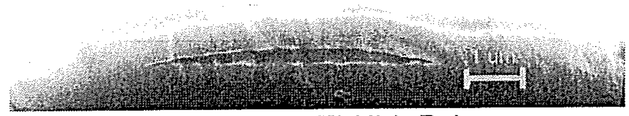

Figure 8 - Post-Highlight Etch

During the design process, the sacrificial TEOS layer mask was ordered as the inverse polarity needed. This caused the need to use negative resist, which performed worse as a protective layer during the following dry-etch to uncover the bridge supports. The negative resist etched much faster than expected, opening up the sacrificial TEOS to etching, making it too thin. The following polysilicon process buried the TEOS layer, creating the bump that is seen in the SEM images.

To be able to successfully release a bridge, the TEOS layer mask had to be remade. The mask's polarity had to be requested correctly so positive resist could be used. A wider TEOS sacrificial layer mask would also give more room for error, in case the etching went through the resist's protective coating, there would still be enough TEOS towards either side that the following polysilicon layer wouldn't bury it.

After processing wafers that were held back with the new mask, we could clearly see an improvement as shown in Figure 9. The difference between the TEOS and polysilicon layers clearly show.

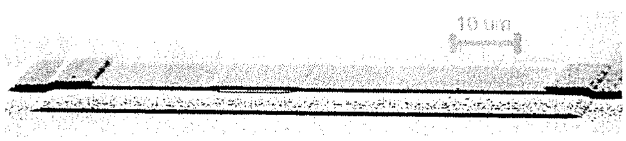

Figure 9 - New Mask Pre-Etch

The following figures show the bridge as the etch time progresses. Figure 10 shows a small amount of etching at the 10 minute mark. As we get to the 20 minute mark, most of the TEOS that surrounded the bridge is etched away, leaving the corners and the space underneath the bridge, shown in Figure 11.

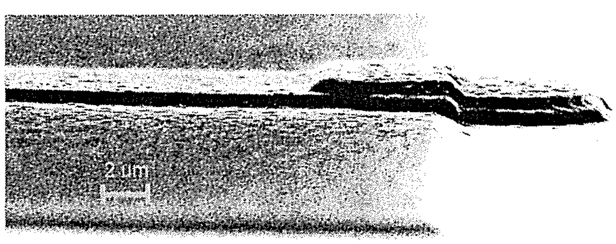

Figure 10 - New Mask 10min Etch

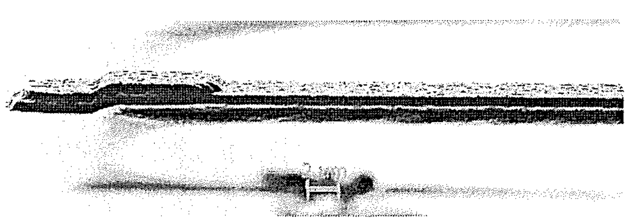

Figure 11 - New Mask 20min Etch

Finally, Figure 12 shows the released bridge at the 90 minute mark. The figure shows some sagging around the middle of the bridge. Figure 13 shows a closer view of the bridge support, and the void underneath the bridge, which signifies a good release, with a bit of sagging towards the middle.

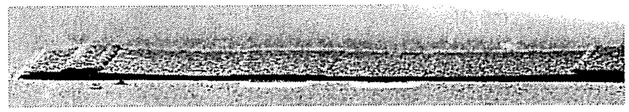

Figure 12 - New Mask 90min Etch

Figure 13 - New Mask Support Visible

5. Conclusions

With time running short, and having to reprocess the mask, we were not able to create the switch devices. Fortunately, we were able to successfully release the bridges and learned much in the process. The design space is one of the most important things to think about before creating masks and working on the process created. Things like overetching need to be taken into consideration when creating structures and depositing layers. During the lithography steps, the size of the alignment marks were a detriment, being too small making it very hard to align manually, especially with the dark field masks.

Future work could be done to the process, to hopefully make it better in some parts and finish the creation of the switches, since we proved that the released bridges could be made.

6. Acknowledgements

I would like to thank Dr. Lynn Fuller for advising on the project and his development of the RIT sub-CMOS process, Dr. Sean Rommel for directing and helping the Senior Design class, Thomas Grimsley for his quick turnaround on mask creations, the SMFL staff for helping with the use of the lab tools and keeping them in working order, Khamphone Inboune and Jeffrey Traikoff for their help with processing, the senior design class for their comments and help on the presentation and poster, and finally Christopher Phillips for proofreading all of my written works during this process.

7. References

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