Deep Submicron III-V on Si-based Esaki Diode

K.L. Johnson, S.L. Rommel, M. Barth, D. Pawlik, P. Thomas, *Rochester Institute of Technology*

Abstract—**Esaki tunneling diodes are reemerging as a viable technology option in helping to improve speed and performance of many high speed device applications. The revival of this technology may be linked to the development of new substrates available to research that allows for the fabrication of a device comparable to current silicon technology. Using a III-V on Silicon Substrate, it was demonstrated that it is possible to create working Esaki Tunneling Diodes.**

Index Terms—**Esaki Tunneling Diode, III-V, Silicon substrate**

I. Introduction

ESAKI tunneling diodes (ETD) were developed in the late 1950s and have been available commercially in small quantities from universities, research facilities, and companies with specializations in the technology since 1969[1]. With the adoption of a nearly exclusive silicon industry and the preference of CMOS structures in both research and industry, the technology for production of ETDs was all but abandoned in favor of the dominant silicon technology [1]. Much of the documented research concerning ETD technology dates to the 1960's and 1970's, with a more recent resurgence in interest in the last ten years. More recently renewed research in ETDs, particularly on III-V substrates, has created opportunities through which these devices may be included in mainstream technology as they catch up in speed and performance to current silicon technology. Through the adaptation of more conventional device fabrication, and the growth of III-V layers on silicon substrates, the drive to study and develop processing methods for this ETD technology has reemerged.

Able to operate at high frequencies, ETDs provide a robust method for creating logic circuits [3]. With a relatively low power consumption and condensed layout, the ETD provides a viable option to help reduce the footprint of devices in real-estate, as well as on the power grid. ETDs may also be used in signal processing, as well as high-speed gates and analog-to-digital devices, the speed at which they operate allowing for an accurate analysis and transmission of the signals. These characteristics are helping the device to reclaim a hold on research as options for the continued advancement of technology continues. The use of a fast device such as the III-V on Si-based ETDs provides an opportunity to continue speeding up device performance, while focusing the improvements on device design and materials, instead of the lithographic process explicitly.

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K.L.Johnson is a student with the Rochester Institute of Technology's Department of Electrical and Microelectronic Engineering, 82 Lomb Memorial Dr., Rochester, NY (e-mail: klj3604@ yahoo.com).

S.L. Rommel, M. Barth, D. Pawlik, P. Thomas are through the Rochester Institute of Technology's Department of Electrical and Microelectronic Engineering, 82 Lomb Memorial Dr., Rochester, NY.

II. Fabrication and Testing

A. Fabrication

The diodes presented were fabricated on a Gallium Arsenide (III-V) layer which was grown offsite by method of epitaxy on a silicon substrate [2]. The substrate and epitaxy layer were provided to the group by Amberwave, upon which a fabrication method was developed by Rommel, *et al.* Fig. 1 shows the undercut resulting from the Citric Acid etch pioneered in the specific process used to fabricate devices in this research. In previous processing by Rommel, *et al*, Sulfuric acid was used to etch the III-V layer, however the etch rate was extremely fast and difficult to predict, resulting in extreme undercut.

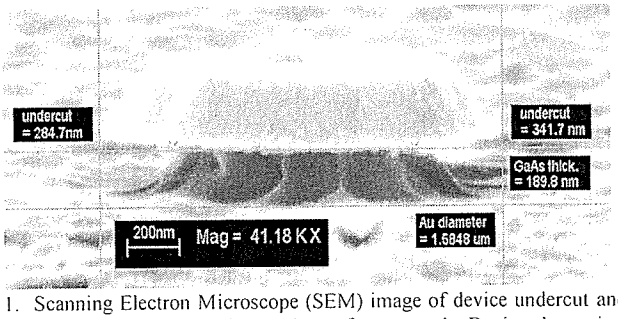

Fig. 1. Scanning Electron Microscope (SEM) image of device undercut and substrate topography taken at 84° to the surface normal. Device shown is a gold contact on top of an etched III-V layer.

The Citric acid etch was performed for 2.5 minutes, resulting in an average etch rate of 1.7nm/second. It was noted that the first 30 seconds of the etch did not result in any noticeable etching of the device when inspected under a Scanning Electron Microscope (SEM). Judging by the topography of the III-V substrate in Fig. 1 and the previously mentioned observation, it is possible that the resulting etch occurred quickly and near the end of the 2.5 minute process once the crystal structure began to etch. The resulting topography within Fig.1 shows that the crystal structure of the III-V material etched along the crystal structure of the material. The uneven surface as well as the wave-like pattern of the mesa created underneath the gold contact provided many challenges to the researchers during characterization of

the device. Two difference devices were studied using the SEM in two locations, and an average undercut of 257.725 nm was calculated using these device images. The largest observed undercut was 341.7 nm and the smallest was 147.7 nm. The contacts and underlying mesas were approximately elliptical in nature.

B. Testing

Fig. 2 details the Negative Differential Resistance (NDR) curves characteristic of the ETD behavior. In the reverse operation, the devices responded in a relatively similar manner of an open circuit. Once the devices enter the forward operation however, the curve demonstrated the NDR behavior that allows for it to quickly switch on and off, allowing it to operate at high frequencies. It was noted that any devices smaller than 700 nm at the location tested, did not appear to have mesas remaining under the gold contacts after the etch process, or during testing. It was usually possible to visually inspect the devices under a magnification of 10X or greater, and to note the presence or absence of the 1st level gold contact under the 2nd level gold contact. Even so, all mask-defined device sizes, from 20.0 um to 50 nm, were tested to verify behavior but open circuits were omitted from Fig. 2 in order to improve clarity of the graph.

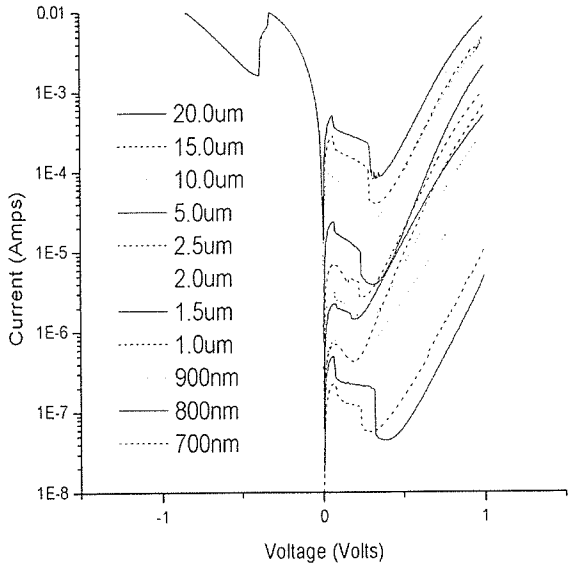

Fig. 2 Measured Current-Voltage characteristics of Esaki Tunneling Diode, measured on edge die. Reverse currents overlap, resulting in a single line.

Of the three locations on the processed piece which were tested, two demonstrated operational devices below the mask-defined size of 500 nm. Fig. 3 demonstrates the behavior of these two devices, and their location in relation to the exposure matrix used during the electron beam lithography steps. It is noted that the middle of the piece, as well as a corner both yielded working devices at 200 nm. A more thorough characterization of all die may yield more working devices at the 200 nm size or smaller. Due to time constraints, only three locations were thoroughly tested which included two edge die on opposite locations of the piece, and a location at the center of the piece.

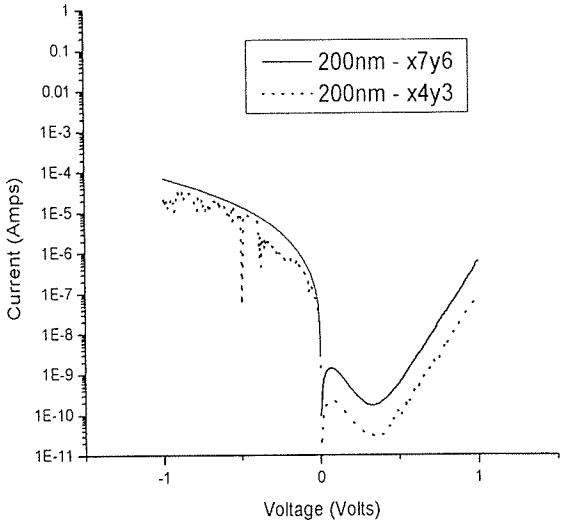

Fig. 3. Current-Voltage characteristics for smallest measured diodes.

Fig. 4 displays the peak current density of the devices through a comparison of the current versus the area of the devices. The areas of the diodes were calculated taking into account an average, observed undercut of 257.725nm. Many of the devices are elliptical, and the undercut is not uniform (as noted in Fig. 1), requiring an approximation of the current density. The topography of the etch made it difficult to determine an accurate area, therefore the current densities presented here are estimates. It is believed that the program and process used to determine the areas of the diodes may have been inaccurate, resulting in the observation of two trends within the single set of data. A modification of the method which improves accuracy of the mesa area approximation may yield more consistent estimates for the current density approximation.

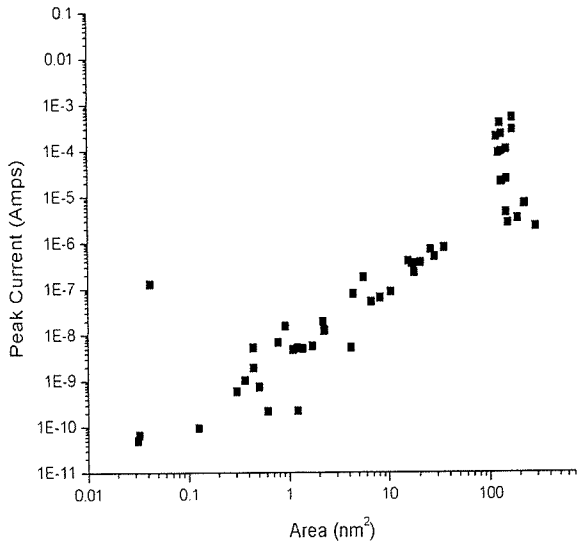

Fig. 4 Current versus Area curves of devices for peak currents calculated for devices.

III. Conclusion

The process of fabrication successfully resulted in yielding devices, which allowed for a general characterization of the ETDs developed. While the final current density calculations suffer errors resulting from method of analysis, the NDR curves provide promising data. It is conceivable from the information gathered, to suggest that it is possible to create working devices in the sub-micron range by intentionally controlling the undercut of the wet etch process presented here.

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Kelly L. Johnson (RIT'10) Johnson is a native of Rochester, NY, having attended Pittsford Sutherland High School and participated in Project Lead The Way, a program which led her to becoming an undergraduate student at the Rochester Institute of Technology.

She currently works in the Semiconductor and Microsystems Fabrication Laboratory as a student hire. She has had co-op experiences with Qimonda, Dr. Sean Rommel's research group, and ITT Space Systems Division. Her achievements on co-op include the Qimonda "On-The-Spot" award for emergency FDC response, and a paper accepted to the IEDM 2008 conference ("Record PVCR GaAs-based Tunnel Diodes Fabricated on Si Substrates using Aspect Ratio Trapping"). She also has participated in the 2008 Digital Rochester Bright Ideas contest, where she won the 1st place ASE Optics award for her idea "Easy Access to Implantable Health Data", and in the 2009 Undergraduate symposium, presenting on the topic "Circuit Simulations Using an Empirical Model of a GaAs Esaki Diode".