Mobility Comparison of Poly (3-hexylthiophene) based Organic Field Effect Transistors

Harry Zhiyuan Hu
Department of Microelectronic Engineering, 82 Lomb Memorial Dr., Rochester, NY 14623. Email: zxh9215 @rit.edu

Abstract-Poly (3-hexylthiophene)(P3HT) is the widely used in configuration of polymer solar cells. In order to correlate improvement in mobility with an improvement in power conversion efficiency of solar cell, organic field effect transistor (OFET) is investigated, which can easily extract mobility basing on I-V characteristic. Experiment shows that mobility of P3HT increase 290% after annealing. Also several experiments are done to diagnose larger deviation problem among chips to chips.

I. Introduction

The traditional method to determine the intrinsic charge transport and carrier mobility of crystalline organic semiconductors is the time-of-flight technique. Its weakness of this method is the requirement for special test structure and high speed electronic and/or optics. While this technique is rather accurate it requires high purity macroscopic- sized single crystals of the respective organic material. Since such mm-sized organic single crystals are often difficult to grow they have been produced and studied only for a small set of materials. This puts the method into the hands of specialists in a few laboratories. At present, the most common way to determine the charge carrier mobility of a given organic material is to extract this value from the device characteristics of an OFET. It should be noted, however, that the derived values depend critically on the details of the analysis. Moreover, it has been demonstrated that mobilities derived from field effect or I/V-measurements can differ substantially from the time of- flight mobilities. This fact reflects the influence of extrinsic properties mostly related to trap-states at the electrodes which have to be taken into consideration when determining intrinsic material properties.

II. Theory & Experiment

There are two most regular types of OFETs, with top or bottom contact geometry, shown in Fig 1. Lithography would be applied only on bottom contact device, thus the feature size can be up to a larger scale than top contact. This is very critical to OFET due its low mobility (0.0001~0.000001 cm^2/Vs). In addition, organic semiconductor spin-coating is the last layer of bottom contact device. This limits any time delay between organic materials coating and finally testing, which also avoid any possible factors influencing mobility during further manufacturing procedures. Basing on the goal of project, bottom contact will be a better option. Figure 2 shows the cross section and platform of transistors. Chip manufacturing step and specification also listed in Table 1. Compare to cross-section layout, an additional Nickel layer is applied to solve Gold electrode adhesion problem.

III. Result

In organic material, charge moving is more like hopping from trap to trap instead of moving as an excited charge. Hence, the mechanism of OFET is different from normal semiconductor such as Si, but the shape of the current-voltage (I-V) characteristics of OFET is similar to regular field-effect transistors (PFET) at gate bias voltages Vg higher than a threshold voltage Vt. Eq 1 shows the mathematical model using in this experiment. Since it extracting relative mobility, assuming with consistent contact resistance Rc in every device, this model should be acceptable even thought without involving Rc into consideration. At low drain voltage Vd, linearity of Id vs Vg (Fig 3) is more significant, so threshold voltage Vt is extracted at Vd= -1V by finding the x-axis intercept. Data shows the Vth is really consistent among various width-length ratios and different gate bias, thus the average Vt is used to extract mobility from Id vs Vd graph (Fig 4) with a add-in software in excel, by modeling the best fit line compare to theoretical value . Result shows higher gate bias has low mobility (Fig 5); unfortunately this shows a opposite trend of theory.

It is believed that annealing at glass transition temperature will change to the morphology of P3HT. A 10 minute 165 C annealing was applied. Without annealing the mobility of P3HT is 1.278E-4 cm^2/Vs and after annealing is 3.718 cm^2/Vs, which has 290% enhancement. This improvement may not truly present how morphology change, because contact resistance decrease too after annealing, which wasn't considered in our model. Another problem is 30% deviation among chips. This make those chips can't not be use to compare mobility of materials if their mobility difference is less than 30%. There are three possible reasons to cause this deviation. First one is bad contact resistance. Second is contamination at chip-cutting processes and last one will be bad connection between testing probe and metal contact. In order to eliminate the first possible factor, annealing was applied right after spin coating in order to release the tension also try to get a better interface between Au and P3HT. And result still showed 30% deviation. For second factor, a cleaning process was applied before spin-coating P3HT, but deviation only reduces to 25% which is still out of

expectation. Consequently the last factor may be the critical factor to cause this un-uniformity. P3HT has high resistance, so even just a little amount of P3HT between testing probe and Au contact, current will significant reduce.

IV. CONCLUSION

Mobility is successfully extracted from OFET device. Experiment shows that mobility of P3HT improved 290% due to morphology change, which achieved by annealing. Although contact resistance decrease also contribute this improvement, but the trend between mobility and morphology still be investigated. Finding a way to open a hole in P3HT layer in order to achieve a good contact between test probe and electrode will be future work of this project.

References

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[2] Kymissis, Ioannis, "Organic Field Effect Transistor" 2009, XII, 156 p. 85 illus., Hardcover ISBN: 978-0-387-92133-4

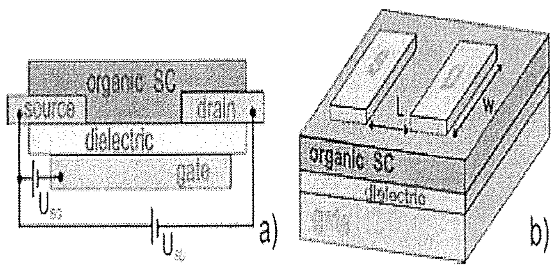

Fig. 1: Schematic layout of OFET with top (a) and bottom contacts (b)

$$I_D = \frac{W}{L}\mu \cdot C_I\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}, \text{ for linear mode,}$$
$$\text{if } V_{DS} \le V_{GS} - V_T \qquad (1)$$

Equation 1: model is used to extract mobility

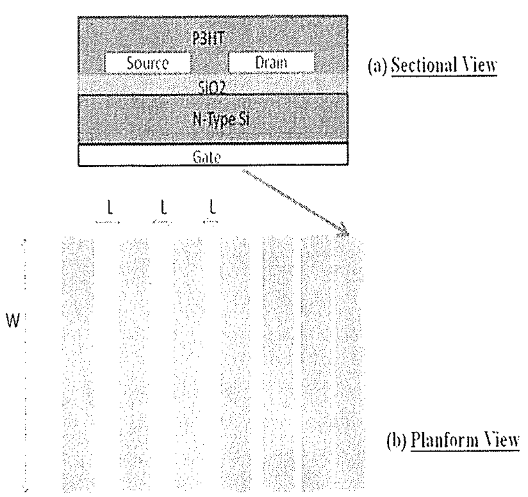

Fig.2: (a) cross-section view and (b) platform of transistors

Device Processing Step
• RCA clean: Standard Procedure
• Oxide growing: 100nm Wet Oxide (Recipe: Kooi1000A)
• Backside oxide etch: 3-4 min (1:10 HF)
• Backside Aluminum deposit : Al 200nm evaporation
• 400C Al sintering
• Gold Lift off (Ni 10nm adhesion layer Au thickness 150nm)
• Cutting into chip process
• Organic materials spin coating (P3HT/Chloroform 10mg/mL 150nm)

Table 1: Devices specification & Process Step

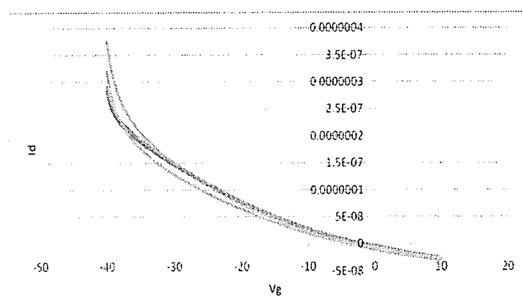

Fig.3: Id vs Vg graph, different line present different W/L ratio transistors

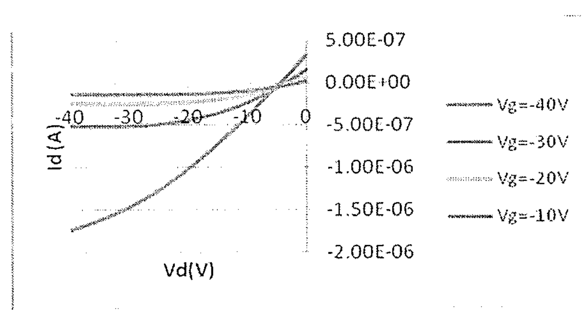

Fig.4: Id-Vd Characteristics at various Vg.

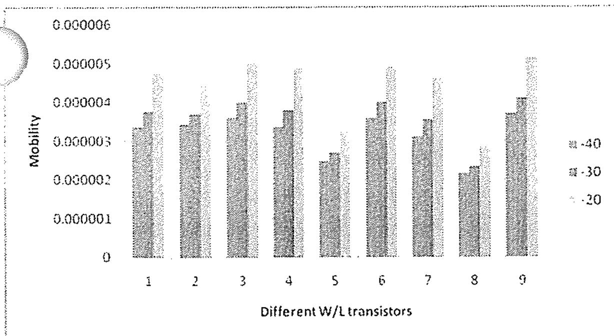

Fig. 5: mobility at various Vg for various W/L ratio devices