Metastable States and Leakage in PN Junction Diodes

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Abstract—**The low-temperature annealing kinetics of ion implanted silicon is a critical factor worthy of consideration when thin film crystalline silicon is processed on a low temperature substrate. Deep Level Transient Spectroscopy, Thermally Stimulated Current and Current-Voltage characteristics suggest that competition between Solid Phase Epitaxial Regrowth and dislocation loop formation is a critical factor in silicon implanted with P31 ions and annealed at temperatures ranging from 525˚C to 650˚C. Solid Phase Epitaxy dominates the kinetics of fully amorphized samples annealed at 525˚C, where shallow-level trap states dominate the reversed-bias leakage current of diodes. At low implanted doses (where the substrate is not completely amorphized) and at 650˚C, dislocation loop nucleation and growth seems to dominate annealing kinetics, resulting in the formation of a deep-level trap at .528 eV.**

Index Terms—**Ion Implantation, Metastable States, Shockley Read Hall (SRH) Recombination, Deep Level Transient Spectroscopy (DLTS), Thermally Stimulated Current (TSC)**

I. Introduction

A critical factor in the processing of semiconductor devices on low temperature substrates is the reduced thermal budget allowed for semiconductor processing. This is especially true of situations where defect states caused by previous processing steps must be annealed out, as is the case after the implantation of charged ions into the substrate in order to form a metallurgical junction.

The act of Ion Implantation generates massive numbers of point defects within the semiconductor. Annealing at elevated temperatures will reduce the number of defects present in the semiconductor due to ion implantation, but will also generate a new group of defects as point defects bond with impurities present in the lattice and with each other. The states generated as part of the Ion Implantation process as well as the states formed by annealing at elevated temperatures are called Metastable States because they lead to a higher energy state within the semiconductor crystal but require substantial input energy in order to dissociate.

Because of the lower allowed processing temperature, full annealing of all defect states may be impractical and time consuming at best or impossible at worst. If these states exist within the depletion region caused by ionization of impurity atoms at the metallurgical junction, they will lead to a leakage path for carriers within the junction and increase the current in the reverse biased mode. This increase in current will increase the power-consumption of devices fabricated in this manner and may also necessitate circuit complexity which would be unnecessary otherwise. The source of this leakage current is the phonon-assisted recombination of carriers at defect sites. This process was first observed and characterized by Shockley Read and Hall[1]. SRH Recombination is the dominant recombination pathway in indirect band-gap semiconductors and, as such, has been studied with a variety of analytical techniques such as Deep Level Transient Spectroscopy[2] (DLTS) and Thermally Stimulated Current (TSC)

The purpose of this study was to analyze the effects of dose and annealing temperature on the presence of metastable states in diodes fabricated on bulk p-type silicon at mid-range temperatures of 525˚C to 650˚C. These metastable states were analyzed using DLTS as well as through TSC measurements.

II. Theory

In an SRH Recombination event, the energy given off is transferred to the semiconducting crystal as a lattice vibration and momentum is not conserved. This contrasts with a Direct Recombination event, in which the energy given off is released in the form of a photon and in which momentum is conserved.

SRH Recombination is a four-pathway kinetic process in which electrons or holes may be either captured or emitted. Carrier capture by a trap state is a thermally independent process in which a trap captures a carrier and its charge state is adjusted to account for this trapped carrier. The kinetics of capture of holes or electrons may be described with the following equations.

$$c_p = \sigma_p v_p p \quad (1)$$

$$c_n = \sigma_n v_n n \quad (2)$$

In these equations, v_p and v_n represent the thermal velocity of holes and electrons, respectively. The terms p and n represent the carrier concentrations of holes and electrons and the terms σ_n and σ_p represent the capture cross-sections of an electron filled trap or a hole filled trap.

A trap state may also emit a carrier as part of a thermally driven emission process where the carrier currently trapped is freed and the trap state reverts to the opposite charge of the carrier emitted. The emission kinetics of holes and electrons are described as follows.

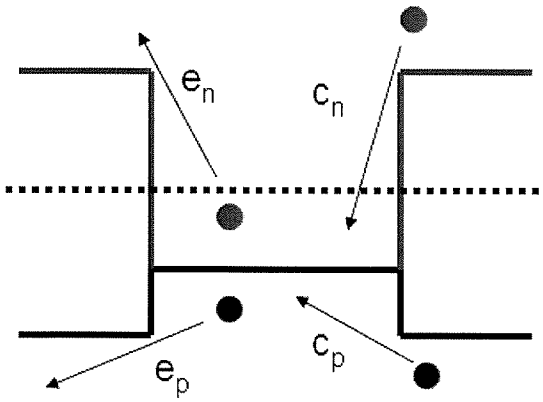

Fig. 1. A diagram of the kinetic processes associated with SRH Recombination for a p-type trap residing below mid-gap

$$e_n = \sigma_p N_C v_p e^{(-(E_C - E_T)/kT)} \quad (3)$$

$$e_p = \sigma_n N_V v_n e^{(-(E_T - E_V)/kT)} \quad (4)$$

In these equations, v_p and v_n represent the thermal velocity of holes and electrons, respectively. The terms N_v and N_c represent the density of states in the valence and conduction bands and the terms σ_n and σ_p represent the capture cross-sections of an electron filled trap or a hole filled trap. E_V and E_C represent the energy of the valence and conduction band edges while E_T represents the energy of the trap level emitting and capturing carriers. The Boltzmann Constant is represented as k and T is the temperature of the semiconductor.

It follows from the preceding description that trap states may exist in either a hole-filled configuration (p_T) or an electron-filled configuration (n_T). A hole-filled configuration may capture an electron or emit a hole and an electron-filled configuration may either capture a hole or emit an electron. Given the constraints listed above, the differential equations defining the transient characteristics of hole-filled and electron-filled trapping states may be described as follows where the variable t is the time associated with the transient process. It is important to note that these terms describe the kinetics of formation assuming a concentration of trap states equal to unity.

$$dp_T/dt = n_T(e_n + c_p) - p_T(e_p + c_n) \quad (5)$$

$$dn_T/dt = -n_T(e_n + c_p) + p_T(e_p + c_n) \quad (6)$$

In order to determine the true rates and the true transient concentration of trap states, the rates above and their associated concentrations must be multiplied by the true concentration of trapping states.

In the simplest case of SRH Recombination, only two charge states are permitted for a single defect structure, a neutral state and a positively or negatively charged state. In some cases, most notably for vacancies in semiconductors, it is possible for multiple charge states to exist past the neutral state. These cases represent dynamics which require far more complex analysis and will not be treated in this text.

Deep Level Transient Spectroscopy is a method of observing the transient characteristic of charging and discharging of traps within a semiconductor. This is

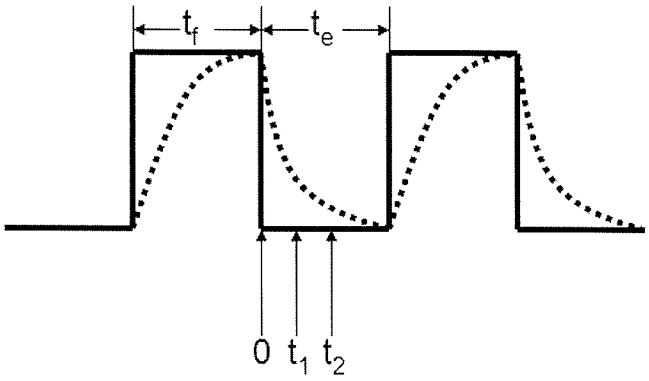

Fig. 2. A diagram of a DLTS transient. The solid line represents the voltages of the applied biasing and the dashed line represents the carrier transient.

accomplished by applying a time-varying voltage signal to the device structure. This signal can be sinusoidal, as in the case of a lock-in technique, or a square wave of variable duty cycle, as is the case in a boxcar differentiation technique. During boxcar differentiation, the signal is designed to bias the structure in such a way that traps fill during a short "filling" pulse (labeled hereafter as t_f) and then emit when the signal transitions to a much longer "emission" pulse (hereafter labeled t_e). For the purposes of modeling, this emission pulse may be assumed to be infinite.

Measurement of the charge transient occurs during the emission pulse, as it is typically dominated by thermalization of carriers from filled trap states. Boxcar differentiation is achieved by measuring the charge levels present within the semiconductor at two separate points, t_1 and t_2, in order to derive an expression for the discrete differential charge. In this situation, the filling pulse acts as a means of defining the initial concentration of trapped charge, the transient of which is observed during the emission pulse.

With these constraints in mind, the following expression for the observable decay in filled trap states over time may

be derived, where A is a thermally-dependant attenuation factor and F is a filling factor dependant on t_f and the temperature. C_0 represents the quasi-static capacitance of the structure and ΔC represents the transient response measured from t_1 to t_2.

$$\Delta C/C_0 = -(2N_T / N_A)AF[e^{-t_1 e_p} - e^{-t_2 e_p}] \quad (7)$$

The current in a PN Junction diode may be expressed using the ideal diode equation, where I_o is the base current, V is the voltage applied to the diode,

$$I = I_0(e^{V/nkT} - 1) \quad (8)$$

The base current, I_o, is the sum of the diffusion current, I_{diff}, and the recombination-generation current, I_{RG}. I_{RG} may be expressed as the product of the diode area, A, the intrinsic carrier concentration, n_i, the fundamental charge, q, and the rate of capture and emission from a hole or electron trap. If only hole states are assumed, this current may be expressed as the rate of capture and emission from a hole trap alone.

$$I_{RG} = dp_T / dt\,(1/2)qAWn_i \quad (9)$$

By invoking the depletion approximation for a PN junction diode, the capture rates for both electrons and holes may be neglected. Additionally, if the assumption is made that any trap states being measured exist more than .5 meV from the mid-gap, one of the two thermal emission terms may be neglected and I_{RG} may be re-expressed as follows, yielding an equation for measurement of Thermally Stimulated Current.

$$I_{RG} = (1/2)qAWn_i e_{p0} e^{([E_T - E_V]/kT)} \quad (10)$$

III. Experimental Method

P-Type silicon substrates with a measured resistivity equal to 10-25 ohm-cm were RCA cleaned and oxidized in an O_2 ambient for 40 minutes at 900°C in a Bruce 7670 Oxidation Furnace. This thermal processing resulted in the growth of approximately 100nm of SiO_2. Following this oxidation, these samples were patterned using positive photoresist and a shadow mask with openings ranging in circular dimension from 1mm to 4mm in diameter. Following exposure and development in TMAH, the resist was cured for 5 minutes at 150°C in order to harden the photoresist in preparation for ion implantation.

The open areas created by exposure and development were etched to a thickness of 100 Angstroms of SiO_2 in a 10:1 mixture of Buffered Oxide Etchant (BOE) and H_2O. The samples were implanted with the P31 isotope of Phosphorus at an energy of 75 KeV, a tilt of 7° and a rotation of 45° in a Varian 350D Ion Implanter. The implanted dose varied between samples from $1x10^{13}$ atom/cm^2 to $2x10^{15}$ atom/cm^2. The remaining oxide present over the implanted regions was etched away and the photoresist mask was stripped in acetone. Following an RCA Clean, samples were annealed in an N_2 ambient for 4 hours at two temperatures for each implanted dose, 525°C and 650°C.

After thermal annealing, samples were aligned by hand to the shadow masks used for patterning of the implant mask layer. A layer of aluminum approximately 200nm thick was deposited on the front and back sides of each sample in a CVC Glass Jar Evaporator.

The devices created were tested for Current-Voltage characteristics from voltages of 1V to -5V. All devices on each sample were tested and the average reversed bias current was analyzed at -1V reverse bias and -3.5V reversed bias. Following Current-Voltage testing, samples were analyzed with DLTS in a Sula Technologies Deep Level Transient Spectrometer over a temperature range of 80K to 400K using time delays of .1ms to 5ms. A filling pulse of .5V amplitude and an emission pulse of -1V to -3V were used. Two samples of interest annealed at 525°C with implanted doses of $1x10^{13}$ atom/cm2 and $1x10^{14}$ atom/cm2 were analyzed at -1V reversed bias using TSC over a temperature range of 1°C to 90°C.

IV. Results/Discussions

Current-Voltage analysis of the samples fabricated demonstrates that leakage current in PN Junction diodes fabricated by ion implantation depends strongly both on the annealing temperature as well as the implanted dose when annealing is performed at low temperatures. At both -1V reversed bias and -3.5V reversed bias, diode leakage was significantly reduced for samples annealed at 525°C for four hours in comparison to samples annealed at 650°C for four hours. Given the long time period over which annealing occurred, the difference in quality of diodes fabricated at these two separate temperatures suggests the formation of some metastable state at higher temperatures which causes degraded performance.

Analysis at -1V reverse bias indicates that diode quality is inversely dependent upon implanted dose when annealing at 525°C. This suggests that 525C is a sufficiently high temperature to induce Solid Phase Epitaxial regrowth (SPE) of damage resulting from Ion Implantation. In comparison, leakage current in diodes annealed at 650°C appears to be reduced with reduced implanted ion dose past a threshold of $1x10^{14}$ atom/cm^2. This suggests that metastable states which are contributing to the diode leakage form throughout the implanted region past this threshold.

Analysis of Current-Voltage characteristics at -3.5V indicates that leakage current depends on reversed bias voltage strongly at low doses, where current increases

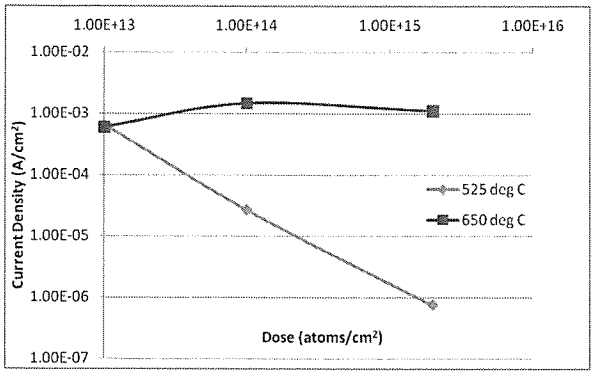

Fig. 4. Average leakage current at -3.5V reverse bias for samples annealed at 525˚C and 650˚C.

dramatically at higher bias. This suggests the presence of some metastable defect deeper from the metallurgical junction at lower doses both at 525˚C and 650˚C.

Current-Voltage analysis at -1V and -3.5V suggests the presence of dislocation loops or some other efficient recombination-generation source throughout the implanted region at an elevated temperature of 650˚C for high-dose implants. At lower doses, these dislocation loops manifest themselves at the end of range only. Annealing at a temperature of 525˚C does not provide sufficient energy to induce the growth of large numbers of extended defects throughout the implanted region. At higher doses, extended defects do not manifest themselves at all at 525˚C, suggesting that full amorphization allows SPE kinetics to dominate dislocation loop formation.

DLTS analysis of the samples fabricated did not yield any results. A scan from 80K to 400K revealed only the noise-floor of the instrument. This suggests that the damage causing the observed leakage is likely too shallow to be observed, either by remaining filled during the emission pulse or being closer to the metallurgical junction than three times the Debye Length. It is possible for the devices formed with lower implanted doses that the damage is too deep such that it exists in the flat-band region during biasing.

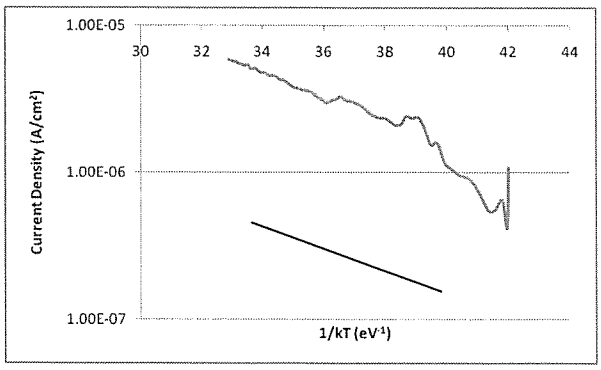

Fig. 5. Thermally Stimulated Current Analysis of a PN Junction diode implanted with $1x10^{13}$ P31 atom/cm^2. Analysis indicates two separate trap levels existing at .528 eV and .202eV.

TSC Analysis of a sample implanted with a dose of $1x10^{13}$ atom/cm^2 and annealed at 525˚C indicates the presence of two separate trap levels; one with an energy

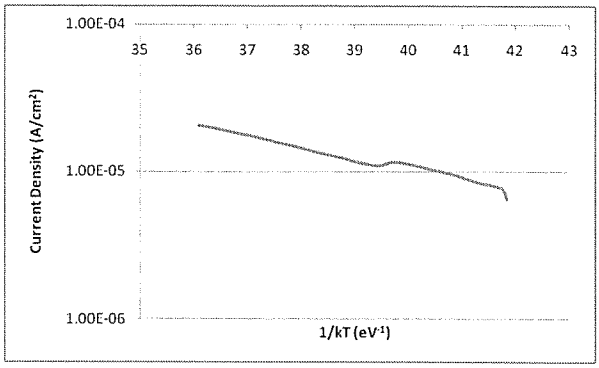

Fig. 6. Thermally Stimulated Current Analysis of a PN Junction diode implanted with $1x10^{14}$ P31 atom/cm^2. Analysis indicates two separate trap levels existing at.178eV.

.528 eV higher than the valence band and one with an energy .202 eV higher than the valence band.

TSC of the sample implanted with a dose of $1x10^{14}$ atom/cm^2 and annealed at 525˚C indicate a single trap level with an energy .178 eV higher than the valence band.

This corroborates Current-Voltage Data that suggests the presence of dislocation loops and improper SPE regrowth at lower implanted doses. TSC further suggests the presence of monovacancies or defect-impurity pairs at higher doses.

V. Conclusion

Current-Voltage and Thermally Stimulated Current analysis of P31-Implanted samples annealed at 525C and 650C indicate the presence of metastable states manifesting

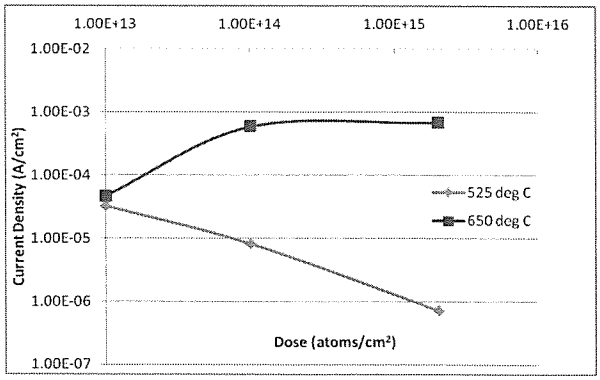

Fig. 3. Average leakage current at -1V reverse bias for samples annealed at 525˚C and 650˚C.

themselves as deep level (.528 eV) and shallow level (.202 eV and .178 eV) traps. Deep Level trapping seems to be caused by the presence of dislocation loops. In samples annealed at 650˚C, these dislocation loops are present throughout the implanted region for high implanted doses. This is not the case for samples annealed at 525˚C. For samples annealed at both 650˚C and 525˚C, dislocation loops manifest themselves at the end of the implanted range

only for low doses. This indicates that the kinetics associated with Solid Phase Epitaxy dominate annealing kinetics at 525˚C for fully amorphised samples while Dislocation Loop nucleation and growth can effectively compete with Solid Phase Epitaxy at 650˚C, even when samples are fully amorphized. The presence of Shallow Level Traps at both medium and light doses suggests that a perfectly crystalline state is not achieved when annealing at low temperatures and that monovacancies or vacancy-impurity pairs are still thermodynamically stable in the 525˚C to 650˚C range.

ACKNOWLEDGMENT

The authors would like to acknowledge the support Jayantha Senawiratne and Greg Couillard of Corning, Incorporated and extend their thanks for the assistance offered in performing DLTS measurements. The authors would also like to acknowledge the support of Chris Bailey and Steven Polly of the NanoPower Research Laboratory for the generous donation of their time and talent in assisting with TSC measurements.

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Patrick Whiting is graduating with high honors from Rochester Institute of Technology in May, 2009 with his BS in Microelectronic Engineering and MS in Materials Science and Engineering. Patrick has interned with Spectrum Devices Corporation designing Power BJTs and Power MOSFETs and with Corning, Incorporated analyzing defects caused by the implantation of Hydrogen and Helium in Silicon as well as developing testing strategies for analysis of the defects caused by Ion Implantation using Deep Level Transient Spectroscopy and Attenuated Total Reflection-Infrared Spectroscopy. His MS thesis is a continuation of the work performed while interning at Corning. He will attend the University of Florida in Gainesville in the fall of 2009, where he will continue his work in Ion Implantation under Dr. Kevin Jones.