4-Bit Microprocessor: Design, Simulation, Fabrication, and Testing

A.J. Ryan, G.O. Phillips, Dr. R.E. Pearson, Dr. L.F. Fuller

Abstract— **The work presented demonstrates the unique ability of Rochester Institute of Technology's Microelectronic Engineering department to design, simulate, fabricate, and test complex digital integrated circuits. Utilizing the resources available, the author would be the first undergraduate at RIT to successfully drive the creation of a microprocessor from design through fabrication to test. The microprocessor created is the most complex digital circuit ever fabricated at RIT. Fabrication was completed on three lots using the well-established RIT sub-μm CMOS Process. Functional CMOS transistors were demonstrated at the Metal 1 level, but complex digital integrated circuits were not realized beyond that.**

I. Introduction

This 4-bit microprocessor incorporates the use of two accumulator circuits (A & B), arithmetic logic unit (ALU), input register, instruction register, output register, phase generator, program counter, and NMOS PLA (microcontroller) properly integrated to create a functional microprocessor. Within these cells digital logic gates are used to create the lowest level of hierarchical building blocks. These digital devices include flip flops, data latches, full adders, inverters, multiplexers, NAND gates, NOR gates, transmission gates, tri-state inverters, and XOR gates to name a few. Simulation results verified the functionality of the circuit schematic design.

Once the circuit schematics (digital and analog) were verified to be functional through simulation, the microprocessor was laid-out (VLSI) using the Mentor Graphics software package in a hierarchical fashion. Layout versus schematic (LVS) checks were performed verifying each sub cell needed to create the complete 4-bit microprocessor.

Fabrication was completed on three lots (5 - 6" wafers per lot) using the well-established RIT sub-μm CMOS Process. Key process parameters include single work function technology, localized oxidation of silicon (LOCOS) isolation, low doped drains (LDD), sidewall spacers on the gate, two levels of metallization, and 13 lithography levels, with a minimum gate length of 2 μm.

Electrical testing and characterization showed functionality of NMOS and PMOS transistors at the Metal 1 level, but complex devices needing Metal 2 were not realized at the time of this writing. Characterization of the root cause is currently completed, and will be explained below.

II. Theory

A microprocessor can be thought of as the "brain" of a computer. All instructions that are to be executed are sent through the microprocessor first. The digital circuit schematic of the 4-bit microprocessor can be viewed below in Figure 5.

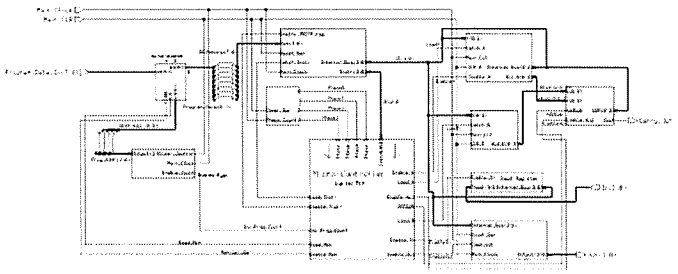

Figure 5: 4-Bit Microprocessor Schematic

The 4-bit microprocessor completed for this project includes SRAM (given), program counter, instruction register, phase generator, micro-controller PLA (given), accumulator A, accumulator B, ALU, input register, and output register.

The input ports include the main clock, main clear, program data in bus, and input bus. The two outputs include carry out, and the output bus.

All components must work together in the proper fashion in order for the complete processor to work. If any one component fails to work as expected, the overall device will fail to function properly.

The program counter is a 4-bit device that counts from 0000 to 1111. It monitors the address of the active instruction. Initially the PC is set to 0000, so the microprocessor starts at the first instruction of the memory. [1]

The SRAM program memory is an 8 by 8 bit memory array that stores the program. Each program line has an 8-bit format: the four most significant bits (MSB) are the instruction itself. The least significant bits (LSB) are the data attached to the instruction (if necessary). [1]

Accumulator A is a 4-bit register that stores the intermediate results computed by the microprocessor. Upon request (Enable A), the accumulator result is placed on the internal bus (IB). [1]

Accumulator B is similar to Accumulator A. It is mainly used to supply the number to be added or subtracted from Accumulator A to execute an addition or subtraction. Accumulator B is a 4-bit register. [1]

The ALU, or arithmetic unit, is a 4 bit device that performs the operation S=A+B (addition) or S=A+(not_B +1) (subtraction). [1]

The Input Register is a 4-bit register that gives the opportunity to transfer the data from the outside world into the microprocessor. [1]

The Output Register, another 4-bit device, transfers the contents of the internal bus to the outside world. Usually, this instruction is performed at the end of the program to display the result. The output register stored the output data on the falling edge of the clock. [1]

The Phase Generator is a 4-bit device that counts phase "pulses" in a fixed order. This device reacts to the clock, and each bit pulses high every fourth clock pulse, for duration of 1 clock pulse. [1]

The Instruction Register is an 8-bit register that stores the currently addressed contents of the program memory. [1]

The Micro-Controller is a programmable logic array (PLA). This device basically controls the entire microprocessor. Triggering from the phase generator this device loads and enables almost every other device in the 4-bit microprocessor with the instruction bits. The symbols with inputs/output labeled may be seen below.

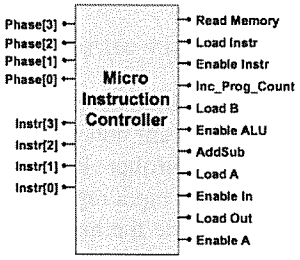

Figure 6: Micro-Controller PLA [1]

As stated above, all devices must be working in unison for the entire 4-bit processor to function properly. If any one given cell fails to function properly, the processor as a whole will surely fail.

III. Schematic Capture, Simulation, and VLSI Design

In order to properly digitally characterize a 4-bit microprocessor, the circuit schematic needs to be properly configured. This involved the schematic capture of each individual sub-component.

Schematic captures were performed using Design Architect from the Mentor Graphics Design Manager suite.

Once the gate level schematics were created (Design Architect), symbols were generated. The symbols were created to accommodate the inclusion of each component into a larger circuit. This allowed for the use of a hierarchical design. A hierarchical design makes troubleshooting much easier, as adjustments can be made the fly.

Once each component was schematically captured, they we digitally simulated in QuickSim II (Mentor Graphics). Tl was to verify functionality. In theory, if each sub-compone simulates as expected, the overall microprocessor w function as expected. However, naming issues and oth various minute nuances can cause the overall device function incorrectly or not at all.

Once all sub-components were simulated, their symbols we integrated into the whole 4-bit microprocessor schemat This included the use of busses and rippers, port's, wir and the symbols of each sub-component.

The complete processor was then simulated using QuickS II. A program was loaded into the SRAM device th controlled the behavior of the simulation. Simulation verifies that the input data is being properly delivered to t rest of the circuit. Simulation 2, verifies the over functionality of the complete 4-bit processor. Lastly, simulation of the student's choosing was to be run a evaluated for correctness. This completed the requiremer for the digital simulation of the 4-bit microprocessor.

As stated above, each individual sub-component w schematically captured and simulated to characterize t device.

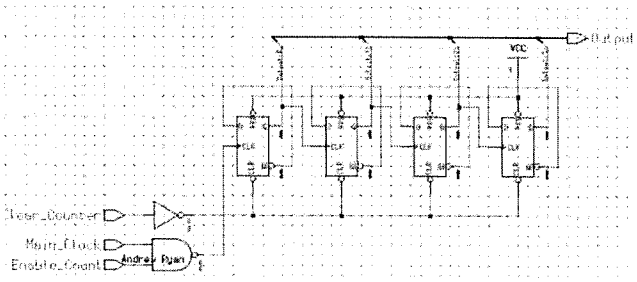

Figure 7: Program Counter Schematic Capture

Figure 3 shows the schematic capture of the progra counter. This schematic includes the use of a single tw input Nand gate, an inverter logic gate, and four flip-flops.

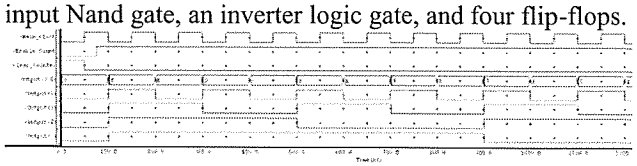

Figure 8: Program Counter Simulation

Figure 4 represents the simulated program counter. output bits respond to the enable count input pulsing high the falling edge of the clock. The output bus counts do from 16 in binary (F in hexadecimal) with each compl clock count. The individual output bits can be viewed at t bottom, and represent the "output bus" on a bit level.

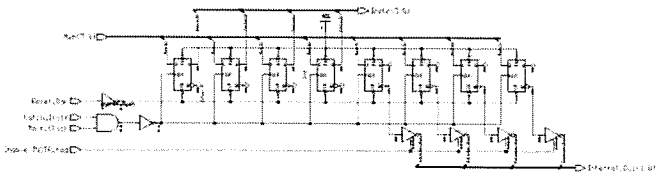

Figure 9: Instruction Register Schematic Capture

Figure 5, above, shows the gate level schematic of the instruction register. This included the use of two inverters, a single and logic gate, four tri-state inverters, and 8 flip-flops. The instruction register is an 8-bit device. The memory bus accounts for the 8-bits on the input side. The outputs include 4-bits dedicated to the instruction bus, and 4-bits to the internal bus (IB).

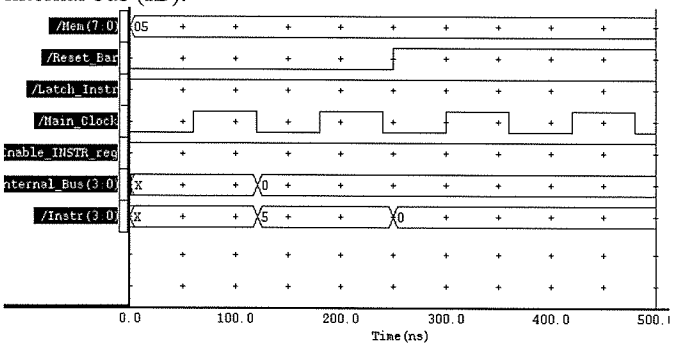

Figure 10: Instruction Register Simulation

Figure 6 represents the digitally simulated instruction register. With an input of "0 5", this device reacts to the falling edge of the clock signal. At the falling edge of the first clock pulse, a value of 0 is sent to the IB, whereas a value of 5 is sent to the instruction line. Both the instruction bus and IB are set to 0 when the reset is triggered.

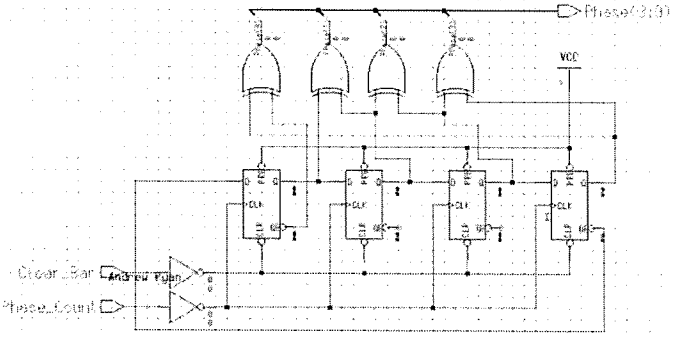

Figure 11: Phase Generator Schematic Capture

Figure 7, shows the schematic of a 4-bit phase generator. This device includes the use of two inverters, four xor logic gates, and four flip-flops. The preset inputs on the flip-flops are all tied high (VCC) on this device.

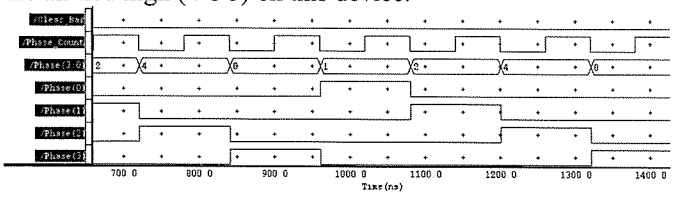

Figure 12: Phase Generator Simulation

Figure 8, shows the output waveforms from the digital simulation of the phase generator. This device shows that the output phase bus reacts to the falling edge of the clock. Starting with the least significant bit (phase 0), each output bit goes high for the duration of one clock pulse width, and then goes low, as the next bit is pulsed high for the duration of one clock pulse width. The output bus counts 1, 2, 4, and 8 in succession as the clock cycles through the pulses.

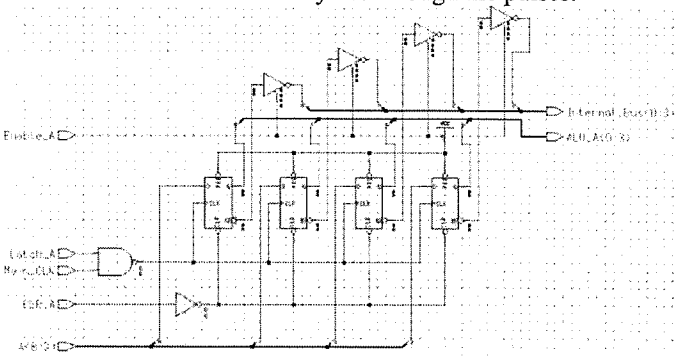

Figure 13: Accumulator A Schematic Capture

Figure 9 shows the circuit schematic of accumulator A. This device includes the use of a single tow-input nand gate, a single inverter, four tri-state inverters, and four flip-flops. This four-bit device sent four bits to the IB, and four bits to the ALU.

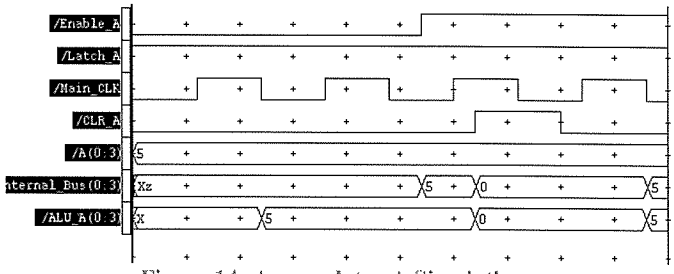

Figure 14: Accumulator A Simulation

Figure 10 shows the simulated output of accumulator A. When the input is loaded with a value of 5, and enable A held low, the ALU bit gets loaded with a value of 5 on the falling edge of the clock. When the Enable A input is pulsed high, the IB reacts by being loaded with the input value. Both output bits are reset to 0 when the clear input is pulsed high. With enable A held high and clear held low, both the IB and ALU busses are loaded with the value on the input bus.

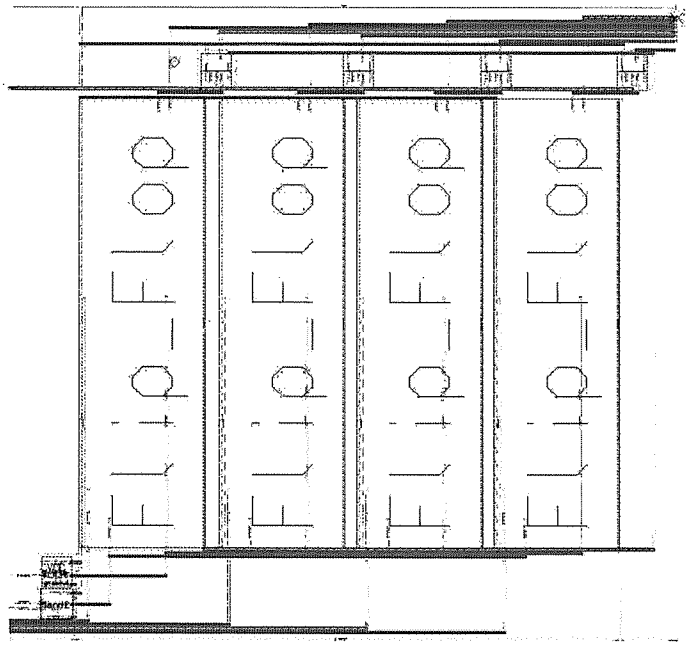

Figure 15: Accumulator A Layout

Figure 11 shows the layout of the Accumulator A circuit.

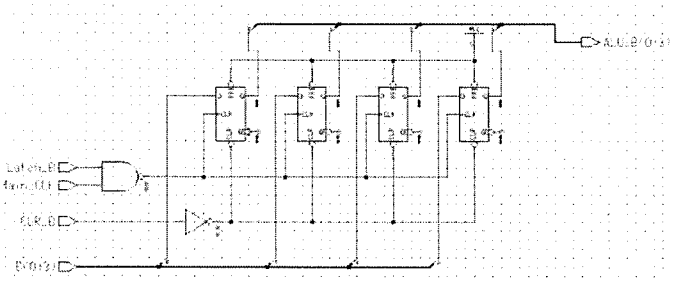

Figure 16: Accumulator B Schematic Capture

The schematic of accumulator B is very similar to that of accumulator A. Like accumulator A this device includes the use of a single two-input nand gate, a single inverter, and four flip-flops. This device outputs all four-bits to the ALU.

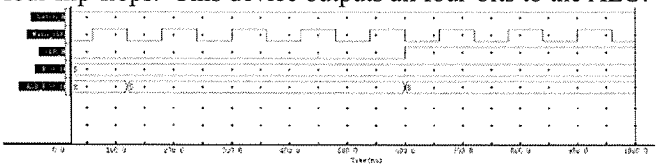

Figure 17: Accumulator B Simulation

The simulation of accumulator B shows that the device reacts to falling edge of the clock. With the input held at a value of 5, the output is loaded with the same value at the falling edge of the clock. The output is set to a value of 0 as the clear input is pulsed high.

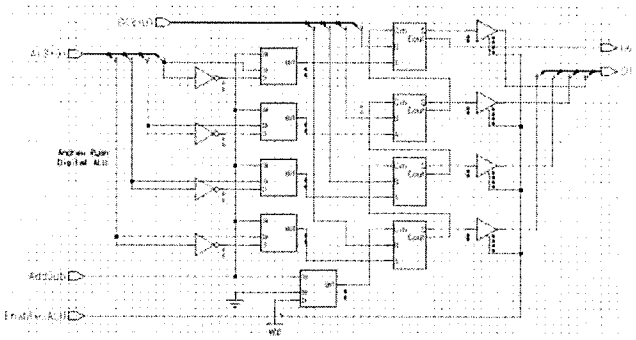

Figure 18: ALU Schematic Capture

Figure 14 shows the schematic capture of the Al (Add/Subtract) circuit. This rather complex device incluc the use of four inverters, five multiplexors (mux), four f adder circuits, and four tri-state buffers. This device tal the outputs of accumulator A and accumulator B and outp them to a single four-bit output.

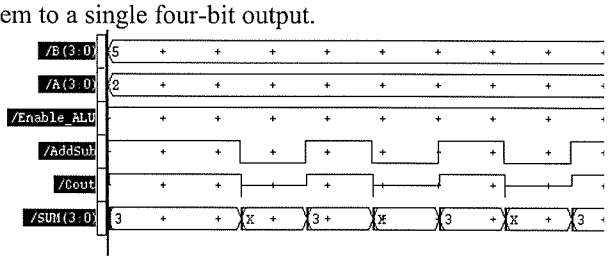

Figure 19: ALU Simulation

Figure 15 shows the output waveforms of the ALU circ When the AddSub input is high the device performs subtraction function (A from B). When the AddSub inpu held low the device is supposed to perform an additi function. This subtraction function is shown cleanly on Sum bus; however there seems to be a problem with addition function. This may explain the initial problems t were noticed with the ALU in the larger microproces simulations. Instead of reading a value of 7, a value of 'x shown. The fact that this device does not perform addition function explains why the overall device fails function properly on at the ALU bus. Update: this dev was fixed and the addition operation was restored to work order. This enabled the entire microprocessor to function desired. The high impedance seen on the Cout line v fixed as well.

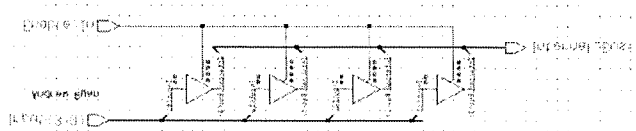

Figure 20: Input Register Schematic Capture

Figure 16 shows the schematic of the input register. T simplest component of the 4-bit microprocessor, this dev only includes the use of four tri-state buffer logic gates. T 4-bit device supplies the IB with 4-bits of data.

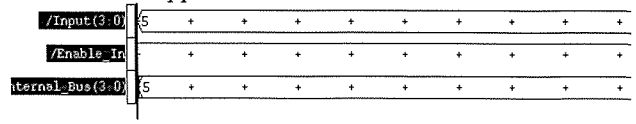

Figure 21: Input Register Simulation

Figure 17 shows the simulation of the input register. It's very simple. With enable held high, the output bus replicates the data loaded onto the input bus.

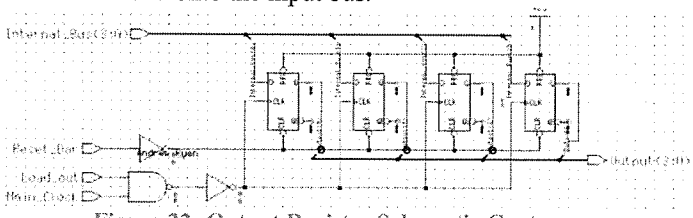

Figure 22: Output Register Schematic Capture

Figure 18 shows the circuit schematic of the output register. This device uses two inverters, a single two-input nand gate, and 4 flip-flops. The output of this device is the output of the entire 4-bit microprocessor. The input of this device comes from the four-bits of the IB. The inverter shown after the nand gate was removed by the end o the project. Figure 18 shows a rising edge device, whereas we needed the processor to react to the falling edge. Removing the inverter gate fixed this problem, and allowed the processor to function as desired.

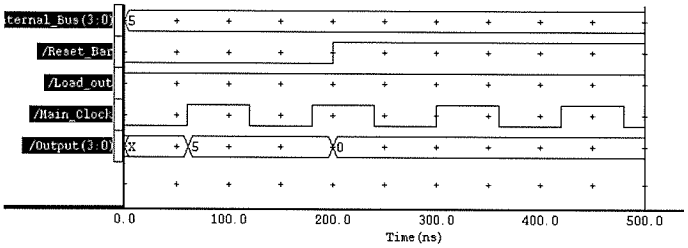

Figure 23: Output Register Simulation

Figure 19 shows the simulation of the output register. With the IB loaded with a value of 5, the device reacts to the rising edge of the clock. As explained above, this device was converted over to a falling edge device. This correction enabled the microprocessor to function properly. At the first rising edge (converted to falling edge), the output is loaded with the value seen on the input. The output shows that value, until the circuit is reset, at which point the output bus is loaded with a value of 0.

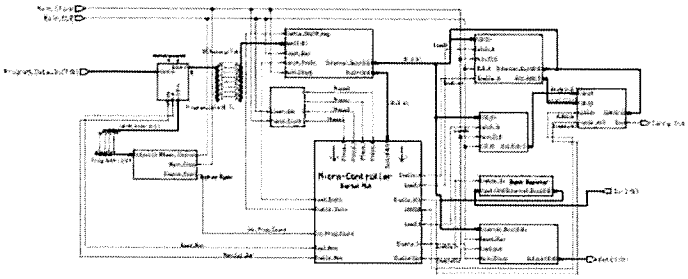

Figure 24: Complete 4-Bit Microprocessor Schematic Capture

Figure 20 shows the 4-bit microprocessor completely wired together. This includes all of the sub-components integrated together. The input ports include the main clock, main clear, program data in bus, and input bus. The two outputs include carry out, and the output bus.

This hierarchical design allowed for relatively easy troubleshooting of an individual sub-component, which would flow through all designs using that part. This is a novel idea, however it only works when you can access it. The problems encountered with this device were fixed, and the hierarchical design allowed for corrections to be made.

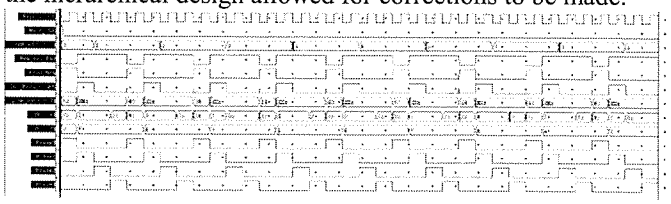

Figure 25: 4-Bit Microprocessor Simulation 1

Figure 21 shows simulation 1, performed to verify that the input data was correctly being delivered to the instruction register. All outputs reacted to falling edge of the clock signal. With each clock pulse the instruction register is loaded with the first value of the program data, at the same time the IB is loaded with the second value of the program data. As the phase bits count up, the SRAM address also counts up reacting every 4th pulse width of the clock.

Simulation 1 used a clock period set to 100. The main clear input was held at 5 at time 0, and pulsed down to 0 at time 10. The simulation was run for 3600.

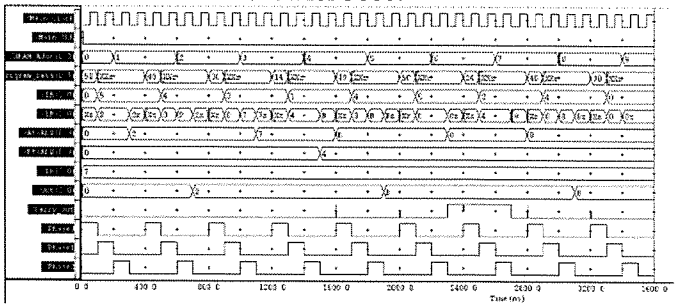

Figure 26: 4-Bit Microprocessor Simulation 2

Simulation 2, shown in Figure 22, shows the output of the overall circuit. First, the device performs an addition operation (5+2=7). Next, 4 is added to the output giving a value of B. B is then sent to the output line. Then, a value of 4 is subtracted from 'C', giving a value of 8. This is then sent to the output line. The device then goes into a state of 'No-Op'.

```
0/53;
1/17;
2/40;
3/2D;
4/40;
5/12;
6/26;
7/40;
8/00;
9/00;
A/00;
B/00;
C/00;
D/00;
E/00;
F/00;
```

Figure 27: Custom SRAM Program for Simulation 3

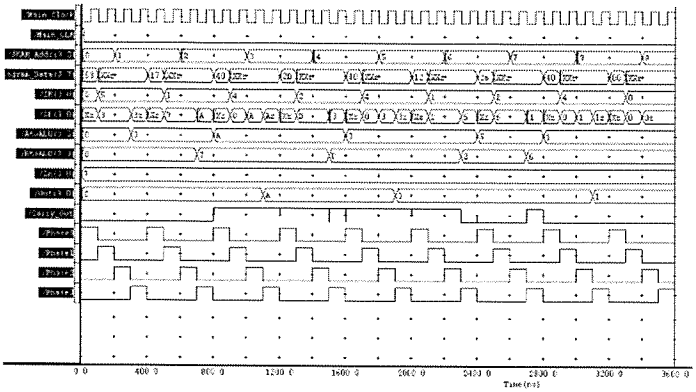

Figure 28: 4-Bit Microprocessor Simulation 3

Figure 24 shows the simulation of a custom instruction set, created by myself. First, using an LDA operation, the program data is loaded to the IR and IB. Next an addition operation is performed adding 3 and 7. The resulting value of 'A' is then sent to the output line. Next 'A' is subtracted from 'D' giving a result of 3. This is then sent to the output line. '3' is then added to '2' yielding a value of '5'. '5' is then subtracted from '6' yielding '1'. This value is then sent to the output line, before the device goes into a "No-Op" state. This custom simulation gave great insight to the overall operation of the 4-bit microprocessor.

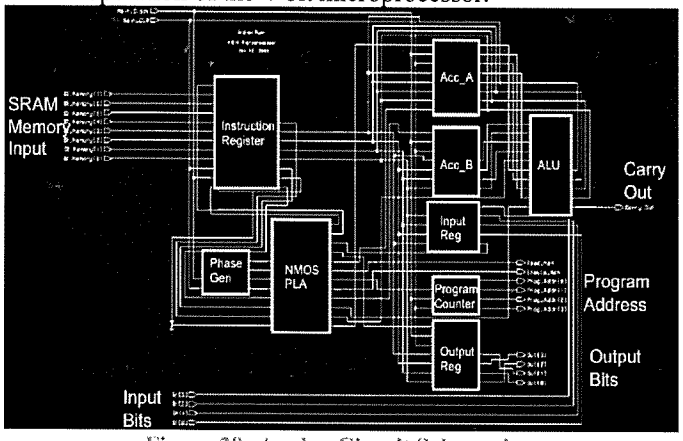

Figure 29: Analog Circuit Schematic

Figure 25 shows the analog version of the circuit schematic. This schematic also left the SRAM cell off of the schematic with additional input and outputs to compensate.

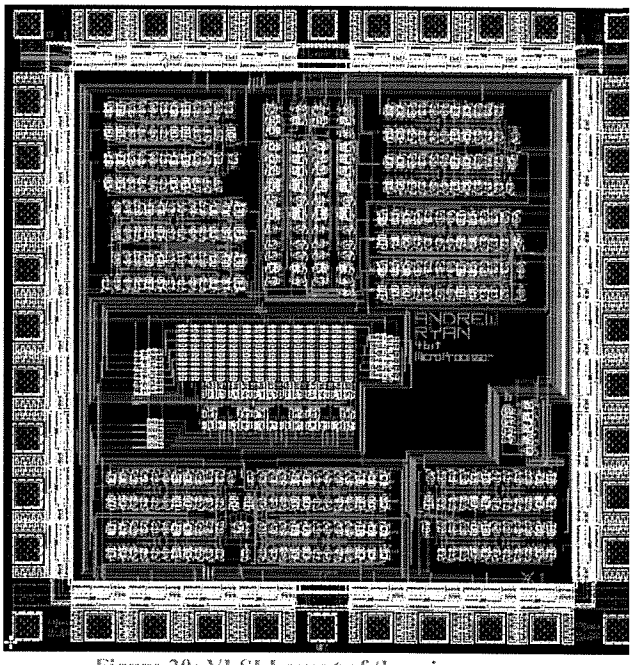

Figure 30: VLSI Layout of the microprocessor

Figure 26 shows the VLSI layout created from the anal schematic shown in figure 25. This layout is a floor plan how the microprocessor will look when fabricated on t silicon wafers. The layout was used to create the lithograp masks needed to fabricate the digital circuit.

IV. Fabrication

Fabrication was completed on three lots (Five 6" wafers p lot) using the well-established RIT sub-μm CMOS Proce This process was developed and characterized by Dr. Ly Fuller at RIT. Key process parameters include single wc function technology, localized oxidation of silicon (LOCC isolation, low doped drains (LDD), sidewall spacers on t gate, two levels of metallization, and 13 lithography leve with a minimum gate length of 2 μm. The complete proc flow can be viewed below in Figure 27.

Step No.	Process	Area	Comment
1	Scribe	Scribe	Wafer ID
2	4-Pt Probe	Metrology	Resistivity
3	RCA Clean	Wets	Particle Measurements
4	Pad Oxide	Diffusion	500Å Dry Ox
5	Pad Nitride	CVD	1500Å Nitride
6	Level 1	Litho	N-Well
7	Pad Nitride Etch	Etch	Plasma Etch
8	N-Well Implant	Implant	Phos, 150keV, 9.5E12
9	Resist Ash	Etch	
10	RCA Clean	Wets	
11	Well Oxide	Diffusion	5000Å Wet

			Oxide
12	Pad Nitride Etch	Etch	Hot Phos
13	P-Well Implant	Implant	Boron, 50keV, 2E13
14	Well Drive	Diffusion	1100°C for 10 hours
15	Well Oxide Etch	Etch	BOE
16	RCA Clean	Wets	
17	Pad Oxide	Diffusion	500Å Dry Ox
18	Pad Nitride	CVD	3500Å Nitride
19	Level 2	Litho	Active
20	Pad Nitride Etch	Etch	Plasma Etch
21	Resist Ash	Etch	
22	Level 3	Litho	P-Well Stop
23	Channel Stop Implant	Implant	Boron, 100keV, 8E13
24	Resist Ash	Etch	
25	RCA Clean	Wets	
26	Field Oxide	Diffusion	6500Å Wet Ox
27	Pad Nitride Etch	Etch	Hot Phos
28	Pad Oxide Etch	Etch	BOE
29	Kooi Oxide	Diffusion	1000Å Wet Ox
30	Blanket Vt Implant	Implant	Boron, 60keV, 7E11
31	Level 4	Litho	PMOS Vt Adjust
32	PMOS Vt Implant	Implant	Boron, 60keV, 2.6E12
33	Resist Ash	Etch	
34	Kooi Oxide Etch	Etch	BOE
35	RCA Clean	Wets	
36	Gate Oxide	Diffusion	150Å Dry Oxide
37	Poly Dep	CVD	6000Å Poly
38	Poly Dope	Diffusion	N+
39	Etch SOG	Etch	BOE
40	4-Pt Probe	Metrology	Sheet Resistance
41	Level 5	Litho	Poly
42	Poly Etch	Etch	Plasma Etch
43	Resist Ash	Etch	
44	Level 6	Litho	n-LDD
45	n-LDD Implant	Implant	Phos, 60keV, 2.5E13
46	Resist Ash	Etch	
47	Level 7	Litho	p-LDD
48	p-LDD Implant	Implant	Boron, 50keV,4E13
49	Resist Ash	Etch	
50	RCA Clean	Wets	
51	TEOS Dep	CVD	PECVD 4000Å
52	TEOS Anneal	Diffusion	
53	Sidewall Spacer Formation	Etch	
54	Level 8	Litho	N+ D/S
55	N+ D/S Implant	Implant	Phos, 60keV, 2E15
56	Resist Ash	Etch	poop
57	Level 9	Litho	P+ D/S
58	p+ D/S Implant	Implant	Boron, 50keV, 2E15
59	Resist Ash	Etch	
60	RCA Clean	Wets	
61	D/S Implant Anneal	Diffusion	
62	TEOS Dep	CVD	4000Å PECVD
63	Level 10	Litho	Contact Cut
64	Contact Cut Etch	Etch	BOE
65	Resist Ash	Etch	
66	RCA Clean	Wets	
67	Metal 1 Dep	Metal	0.75 µm Al (sputtered)
68	Level 11	Litho	Metal 1
69	Metal 1 Etch	Etch	Plasma Etch
70	Resist Ash	Etch	
71	TEOS Dep	CVD	4000Å PECVD
72	Level 12	Litho	Via
73	Via Etch	Etch	BOE
74	Metal 2 Dep	Metal	0.75 µm Al (sputtered)
75	Level 13	Litho	Metal 2
76	Metal 2 Etch	Etch	Plasma Etch
77	Resist Ash	Etch	
78	Sinter	Diffusion	
79	SEM, Electrical	Test	See if stuff works….

Figure 31: RIT Sub-µm CMOS Process [2]

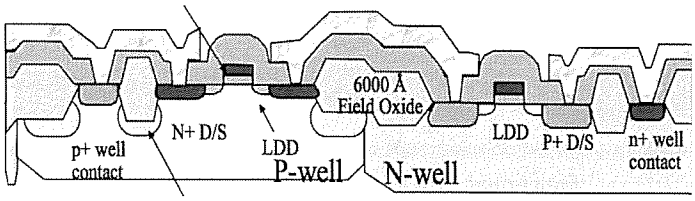

Figure 32: CMOS Cross Section [2]

Figure 28 shows the cross section of the CMOS devices. This project included many firsts for the RIT Microelectronic Engineering department. These firsts include the true implementation of a 4-level per plate lithography setup, and first use of the tiny chip I/O padframe and probe card. This circuit is the most complex digital IC ever fabricated in the SMFL.

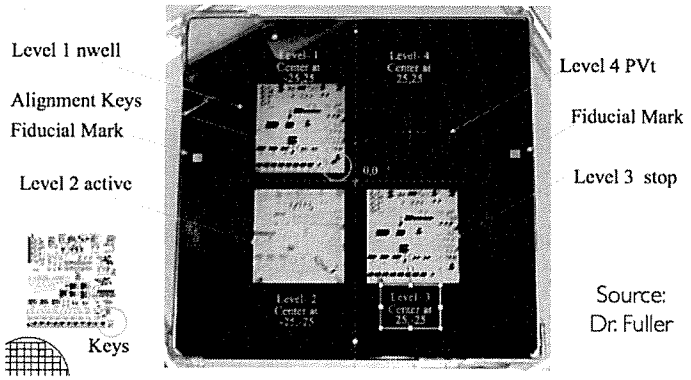

Figure 33: "Quad" Lithography Mask [2]

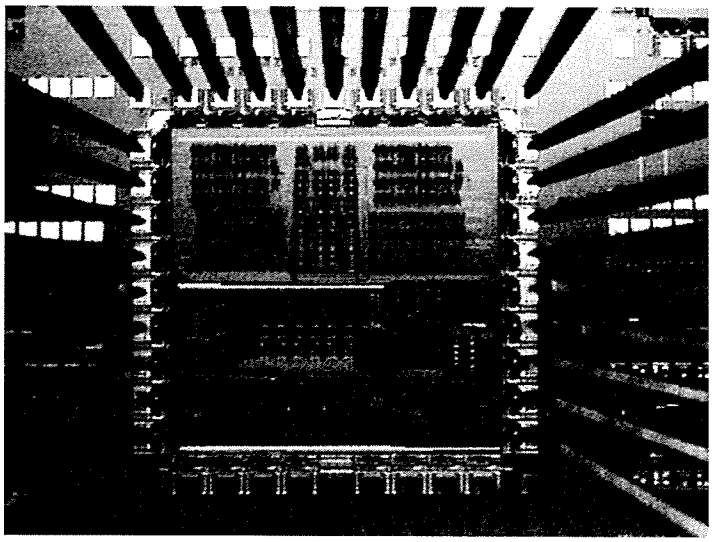

Figure 34: Fabricated Microprocessor with Tiny Chip Probe Card Test Setup

V. Results and Analysis

Functional CMOS transistors were demonstrated at the Metal 1 level.

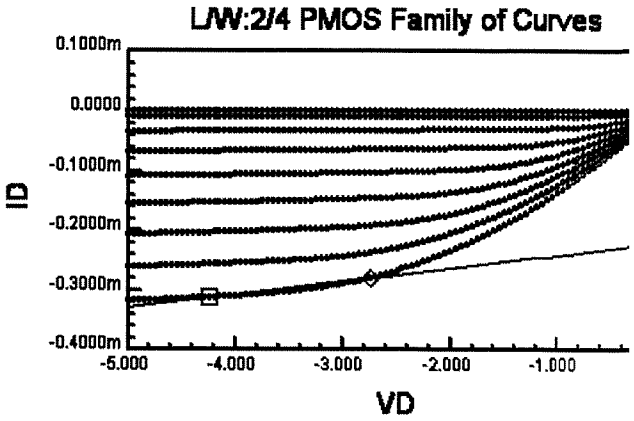

Figure 35: PMOS Family of Curves

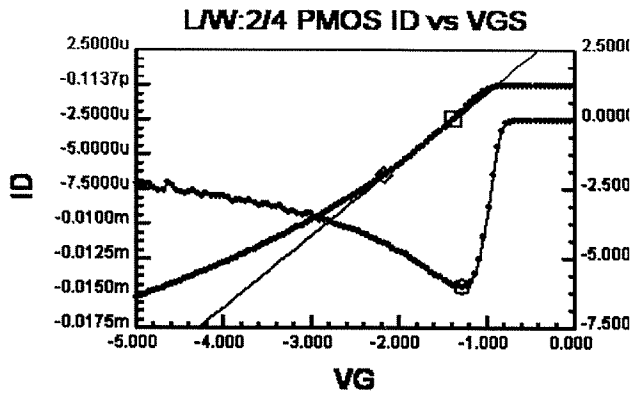

Figure 36: PMOS Id vs. Vgs

Figures 31 and 32 show the I-V characteristics of a 2 (L/W) PMOSFET. The family of curves shows a dra current of ~0.3 mA when 5 volts is applied to the gate saturation mode. The Id versus Vgs plot shown in Figure shows a threshold voltage (Vt) of ~ -1.2 volts. Also tak from this plot, the max transconductance was found to be 6.25 μS.

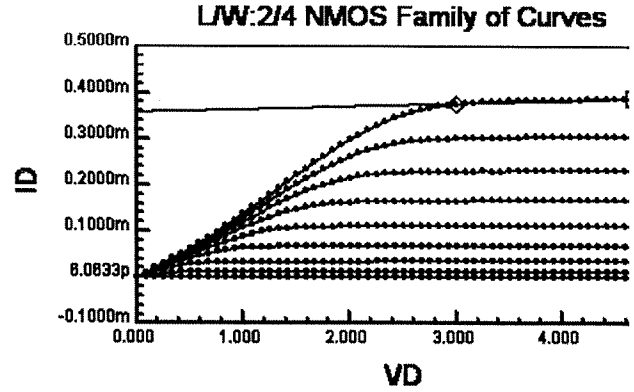

Figure 37: NMOS Family of Curves

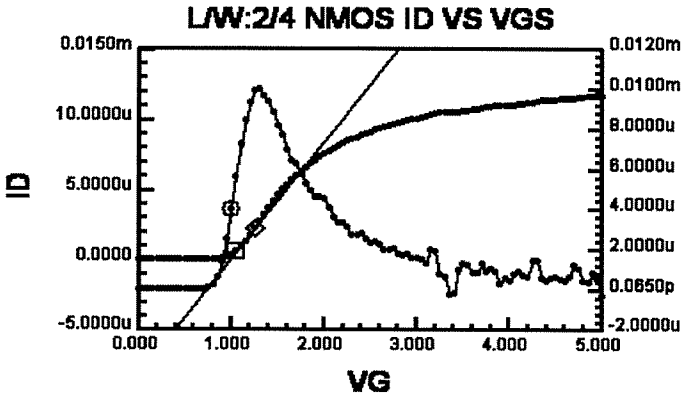

Figure 38: NMOS Id versus Vgs

Figures 33 and 34 show the I-V characteristics of a 2/4 (L/W) NMOSFET. The family of curves shows a drain current of ~0.4 mA when 5 volts is applied to the gate in saturation mode. The Id versus Vgs plot shown in Figure 34 shows a threshold voltage (Vt) of ~ 0.8 volts. Also taken from this plot, the max transconductance was found to be ~ 10 μS.

Scanning electron microscopy (SEM) was performed. Resulting images may be viewed below.

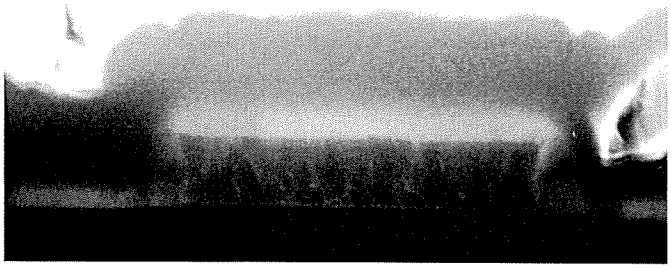

Figure 39: Transistor Cross-Sectional SEM

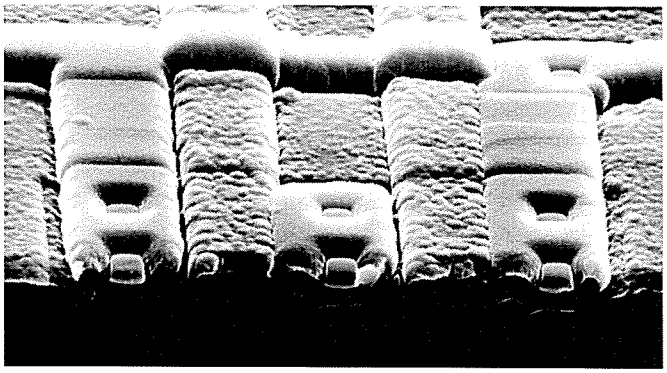

Figure 40: SEM of Contact Cut Fill

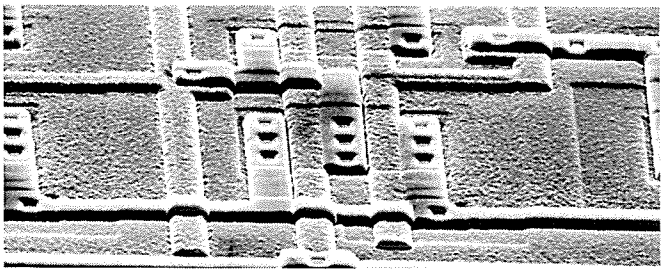

Figure 41: Angled SEM of CMOS Device

Beyond single devices, it was found through electrical testing that more complex integrated circuits were non-functional. An in depth look at the metallization process through electron microscopy was performed to try and pinpoint the root cause.

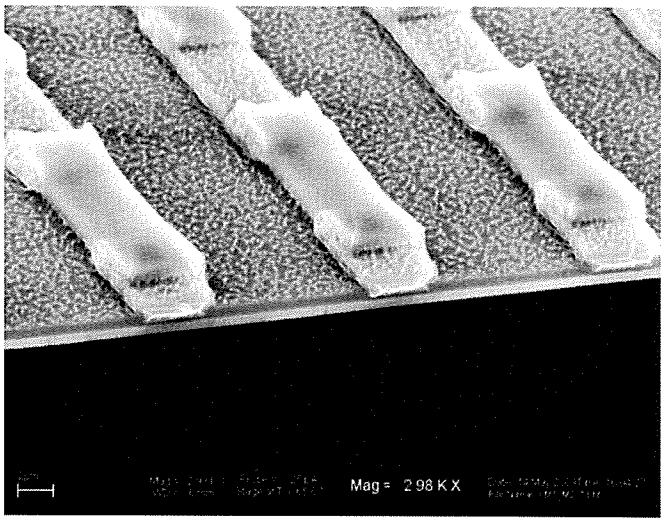

Figure 42: SEM of M1/M2 Topography in a Via Chain

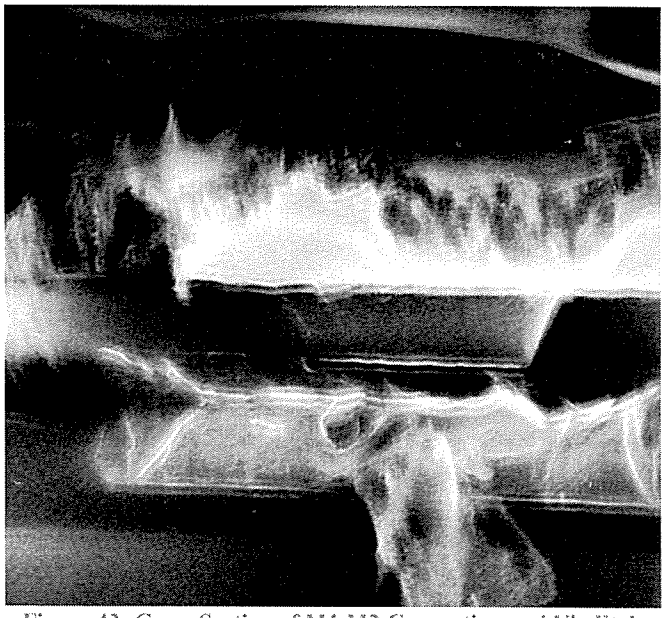

Figure 43: Cross Section of M1 M2 Connection and Via Etch

Initially believed to be an improper via etch, it was found that the root cause behind non-functioning devices needing M2 was due to oxidation of the M1 film. Post via etch, a 34 nm Aluminum Oxide (Al_2O_3) had formed prior to the M2 deposition. This may have formed during the photoresist ash process that uses an oxygen plasma at increased temperatures. This is clearly shown in Figure 39. This thin oxide is an insulating barrier between the M1 and M2 films. This forms a fairly large capacitor causing the devices to be non-functional under CMOS test conditions. The SEM's that were taken verify the highly probable reason as to why

devices needing M2 do not function. For future work, a sputter etch immediately prior to the M2 deposition would help mitigate this problem.

VI. Conclusion

The creation of working transistors and simple devices is a major milestone on the path to demonstrating complex digital circuits. The RIT Sub-μm process has been proven to be a robust technology that yields functional devices. SPICE models for this technology have allowed for the proper simulation and layout of the circuits. Although many obstacles have occurred during the fabrication process, skill based engineering has allowed for the rectification of most of the issues. Oxidation of the metal 1 film was found to be the root cause as to why devices needing metal 2 were non-functional. It is believed that utilization of a sputter etch prior to the metal 2 deposition would solve this problem. Although complex digital integrated circuits were not realized, the project is still widely viewed as a success. Insight has also been gained in many problem areas of the CMOS process, which can be improved upon in future projects. Much progress has been made towards the feasibility of complex digital circuits, such as a 4-bit microprocessor to be designed, simulated, fabricated, and tested to be functional at RIT.

Appendix

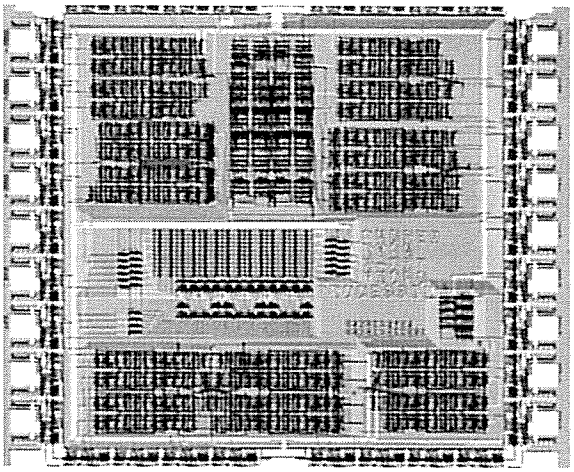

Figure 44: Microscope Image of Complete Microprocesso

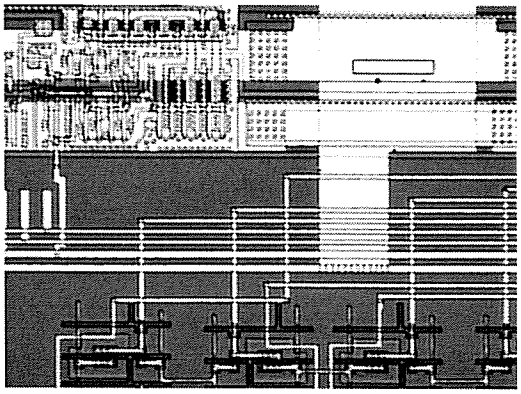

Figure 45: Microscope Image of Metal 1 and Metal 2 Trac

Acknowledgments

Dr. Robert Pearson for his knowledge and guida pertaining to the 4-bit microprocessor, as well as his V experience. Garret Phillips for his help in the fabricatior the devices. Dr. Lynn Fuller for his expertise in CM fabrication and his help with RIT's Sub-μm CMOS proc Dr. Sean Rommel for helping drive the project and keep deadlines. Andrew McCabe for allowing me to utilize previous VLSI layout work. Dave Pawlik for SEM w Tom Grimesly for mask creation. Sean O'Brien and the of the SMFL staff for help during the fabrication process tool training. Chris Shea for helping during the fabricat process and answering my questions. Finally, my fianc Annika Kuyt, for her support and understanding as to wh needed to spend endless hours in the Fab.

References

[1] 4 Bit Microprocessor Details, PowerPoint Presentations & V Correspondence, Dr. Robert Pearson, RIT Microelectr Engineering Department

[2] RIT Sub-μm CMOS Process Details, PowerPoint Presentations & Verbal Correspondence, Dr. Lynn Fuller, RIT Microelectronic Engineering Department