Etching for Dual Damascene Fabrication

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Abstract—**Dual damascene fabrication requires precise dry-etching. Two different methods were investigated: via-first and trench-first. It was found under conditions tested with that micromasking occurred, which was caused by damage to the resist. This caused the dielectric regions to be etched in the unmasked regions, as well as causing significant roughness. However, both etch techniques were found to have the capability of being used in a university dual damascene process.**

Index Terms—**Dual Damascene, trench, via, micromasking, copper interconnects, RIE etch**

I. Introduction

COPPER interconnects have revolutionized the semiconductor industry. Copper exhibits a 30% to 40% drop in the resistive-capacitive (RC) delay, when compared against aluminum. This is because the permittivity of copper is significantly lower than aluminum. This is shown in Equation 1. However, a significant problem with using copper is that it cannot be plasma etched. This problem was solved with the Dual Damascene process.

A Dual Damascene process involves several layers of interlevel dielectric (ILD) being etched to create a void where the copper can be deposited. The excess copper is then removed from the top through a method called chemical-mechanical planarization (CMP). There are two main components in a Dual Damascene: the via and trench. These are shown in Figure 1. The via acts as the connection between the metal 1 and 2 line. The trench is part of the metal 2 design, and connects to the via at the interconnects. The trench is generally wider than the via to allow for easier alignment. There are several different methods of creating a Dual Damascene. The two basic methods are a trench-first etch and via-first etch, which are shown in Figure 4. Both of these methods were investigated in this experiment. The metallization and CMP have already been successfully implemented at RIT, and therefore focus was placed on the etch component of the process [1].

Equation 1: Calculation of RC.

$$RC = \frac{\rho L^2 k_{ILD}}{t_{metal} t_{ILD}}$$

ρ= resistivity of interconnect metal
L= length of interconnect metal
t_{metal}= thickness of the metal
k_{ILD}= permittivity of ILD
t_{ILD}= thickness of ILD

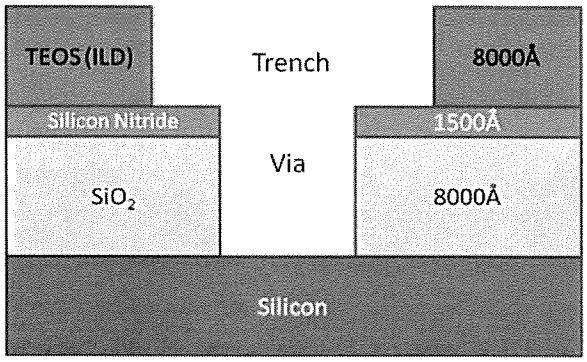


Figure 1: Dual Damascene Structure.

II. Previous Work

Keerti Kalia designed a via-first dual damascene at Rochester Institute of Technology in 2007 for Senior Design. Kalia was able to successfully deposit and adhere Copper, Tantalum, and Tantalum Nitride onto the dual damascene. In addition, CMP did show some promising results. Though there was some dishing and erosion, this should have been expected given the wide variety of pitch and bias dimensions.

However, the etch component had many more challenges. As shown in Figure 2, the via was significantly under etched. The via is only 15-25 percent of the depth that it was intended to be. In addition, the anisotropy is poor due to the use of buffered oxide etch (BOE), and possibly from the pressure being too high in the dry etch recipe, as shown in Figure 3. In addition, the silicon dioxide undercutted the nitride. Therefore, the focus for this experiment was focused on the etch component of the dual damascene process.

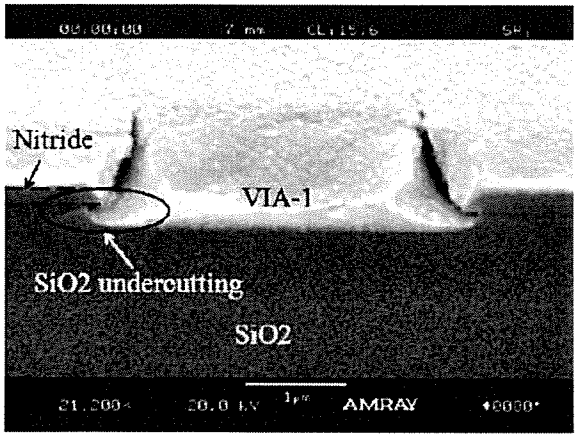


Figure 2: Kalia dual damascene structure showing SiO_2 undercutting of Nitride

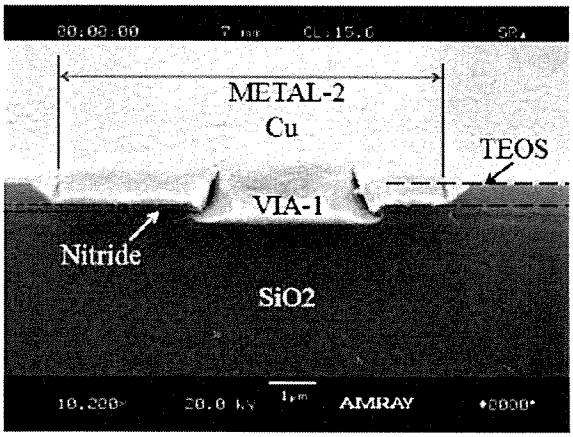


Figure 3: Kalia Dual Damascene Structure with 3um via and 8um trench.

III. Process Flow

The via-first and trench-first design both started with the same starting layers. A thermal oxide was grown to 8000 Angstroms for use as the bottom ILD. Then 1500 Angstroms of silicon nitride (Si_3N_4) was deposited through plasma enhanced chemical vapor deposition (PECVD). This was used as an etch stop between top and bottom ILD. Last, 8000 Angstroms of tetraethyl orthosilicate (TEOS) was deposited through PECVD. This served as the top ILD.

Method	Etch Step	Etch Times (min)
Via-First	Via (1st ILD)	11
	Nitride	1.083
	Via (2nd ILD)	11
	Trench	11
Trench-First	Trench	11
	Via	22

Table 1: Etch Times for vias and trenches

Nitride RIE Etch	
Power	200 W
Pressure	100 mTorr
SF_6	20 sccm
Etch Rate	1588 Å/min

Table 2: Nitride etch specifications

The via-first etch process starts with first level g-line lithography. The via mask has multiple different line and space dimensions for comparison of the varying etch rates. After photo lithography, the wafers are etched to remove the TEOS, nitride, and then thermal oxide.

TEOS/Thermal Oxide Etch	
Power	200 W
Pressure	70 mTorr
CHF_3	65 sccm
Ar	65 sccm
O_2	5 sccm
TEOS Etch Rate	814 Å/min
SiO_2 Etch Rate	350 Å/min

Table 3: TEOS/Thermal Oxide etch specifications

The recipes are listed in Table 1,2, and 3. The thermal oxide needed to be etched for a much longer period,

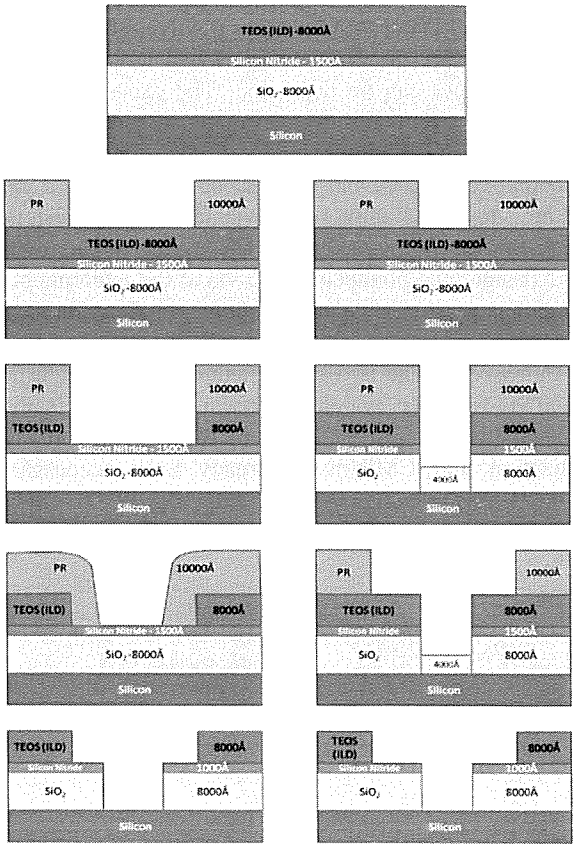


Figure 4: Process Flow Chart- Trench First (Right); Via First (Left)

since the etch rate is about half of the TEOS etch rate. In addition, the etch rate decreases at deep depths. Therefore, half of the thermal oxide needed to be etched. Then the wafers were ashed, and second level photo was performed. The trenches were then etched. This also etched the remaining thermal oxide in the process. The trench-first process performed the same lithography steps (though with different masks). However, the trench etch was first, and only etched through the TEOS. In addition, there was no nitride etch and the via etch was etched all the way through.

IV. Results

The vias were imaged through a SEM prior to second level lithography, and is shown in Figure 5 and 6. The etch appears anisotropic, and most of the dimensions get near or slightly pass the etch stop. The dielectric looks uniform and good quality. However, the resist is significantly damaged. Looking at Figure 5 closely, micromasking can be observed. In addition, in Figure 6 it is clear that TEOS was etched from the top down, and is much more prevalent with small biases

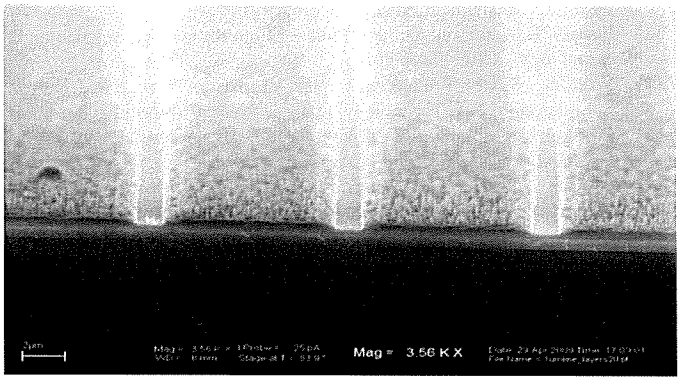


Figure 5: 1 um vias with photoresist on top of TEOS

and pitches. After the second level lithography for both the via and trench first processes, the film is highly non-uniform as seen in Figure 7 and 8. In addition, there is a high amount of surface roughness and it appears that a majority of the thickness of the TEOS has been etched down in the regions suppose to be protected by the TEOS.

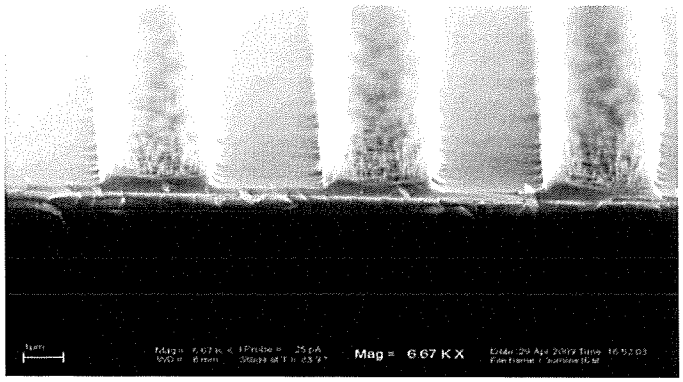


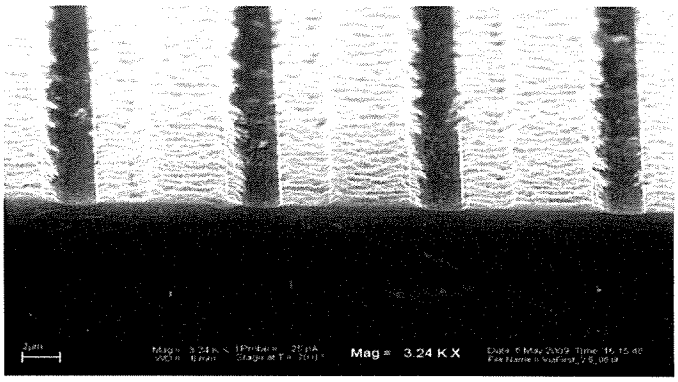
Figure 6: 3 um vias showing etching of TEOS from the top

However, the trench-first and via-first damascene did show the proper structure. In addition, they were relatively antistrophic in nature and significantly more than that of previous attempts. The micromasking problem seem to have etched away all the nitride

V. Recommendations

The main problem with the current design is micromasking is occurring causing the TEOS to pit, resulting in a non-uniform surface. There are five possible ways to correct this problem: reduce TEOS thickness, reduce power, change thermal oxide to TEOS, addition of a metal hard mask, and harden the resist through UV radiation and an extended hard bake.

Figure 7: Via-first Dual Damascene 2.5 um via and 5 um trenches



A. Reduce TEOS thickness

Reducing the TEOS thickness would shorten the etch time leading to a smaller amount of time the resist could be damaged. However, even if the TEOS was reduced to 4000 Angstroms, there would still likely be resist damage as the via depth would by 13500 Angstroms. Figure 5 shows that an 8000 Angstrom etch can cause resist damage. Therefore, this could not be the entire solution.

B. Reduce Power

Reducing the power will cause less ion bombardment of the resist reducing the possibility of thermal or chemical damage of the resist. However, the entire etch recipe would needed to be changed to keep the same anisotropy. In addition, the power is already quite low, and it is unknown if lowering the power would be enough to stop the resist damage.

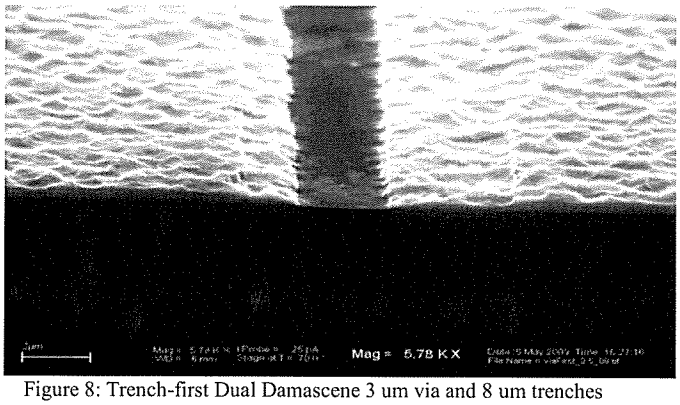


Figure 8: Trench-first Dual Damascene 3 um via and 8 um trenches

C. *Change thermal oxide to TEOS*

Changing the thermal oxide to TEOS would reduce the etch time as TEOS has a much faster etch time, and would greatly reduce the amount of damage that might take place. In addition, it would be more practical, since thermal oxide cannot be grown below the interconnect in a fully processed IC.

D. *Addition of a metal hard mask*

The addition of a hard mask is probably the best solution to the problem. The TEOS would not have damage, since it would be protected by a metal, preferably aluminum layer. Since Aluminum is more selective than resist it would allow for the possibility for deeper trenches and vias. Figure 9 shows the cross-section with an aluminum hard mask.

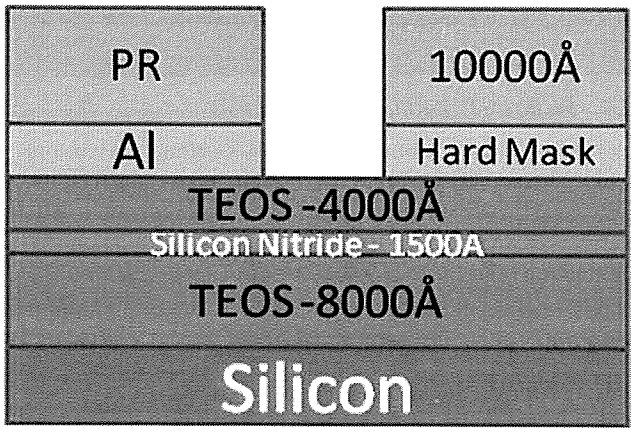


Figure 9: Cross of via etch with metal hard mask

E. *Harden resist through UV radiation and extended hard bake*

This process involves flood exposing the resist after it has already been developed for several minutes, and then baking it between fifteen minutes to one hour between 130-200 degrees C. This would allow the resist to be able to survive under higher thermal temperatures, and be able to endure under the high stress of the plasma. However, the method does not work for all resists, and does not work for all UV wavelengths. Generally the wavelength is around 224 nm, however, some do work for i-line wavelengths as well. In addition, it is much more difficult to strip the resist afterwards. Stanford and Berkeley both have tools that do this, however, they heat the wafer while it is being flood exposed and currently our university does not have this capability. However, there has been some research on this process without doing them simultaneously.

VI. Conclusion

Dual damascene fabrication requires a well defined etch process. Via-first and trench-first etch processes were completed. Under the recipes that were used micromasking occurred, and the underlying TEOS to become pitted and over etched. The surface roughness was great enough, that the wafers could not go through CMP. However, both etch techniques were found to have the capability of being used in a university dual damascene process.

Acknowledgment

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References

[1] Kalia, Keerti. "Cu Dual Damscene: Design and Fabrication". May 2007.
[2] Jiun-Yu Lai, PhD. "Mechanics, Mechanisms, and Modeling of the Chemical Mechanical Process" February 2001.
[3] Suzuki, Kazuaki and Smith, Bruce. "Microlithography: science and technology". CRC Press, 2007.
[4] Wolf, S. "Silicon Processing for the VLSI Era: Volume 4 – Deep-Submicron Process Technology". Lattice Press, California 2002.
[5] P. Singer, "Making the Move to Dual Damascene Processing," *Semiconductor International*, August 1997, p. 79
[6] Stanford Labmembers Semiconductor Nanofabrication Facility Home page.< https://spf.stanford.edu/SNF >. 5/01/09