Front Contact Grid Design for Terrestrial III-V Concentrator Solar Cells

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Abstract—**Photovoltaic devices can exhibit an increase in conversion efficiency as increasing power density is concentrated onto them. Design of the front contact grid is a major processing step that can govern the concentration at which the efficiency is at a peak. A series of equations provided by M. Green was used to design GaAs solar cells for concentrations of 1, 25, 50, 100, and 200 suns. The cells were processed and tested under a 1-sun calibrated AM1.5G spectrum, as well as a Large Area Pulsed Solar Simulator to measure device parameters under concentrated light. All devices—except the ones designed for 1-sun—exhibited increases in efficiency with increased concentration. Additionally, series resistance was shown to decrease with the increased concentration design.**

I. Introduction

In photovoltaic devices operating under concentrated illumination, short circuit current density (*Jsc*) increases approximately linearly with the concentration level, while open circuit voltage (*Voc*) increases as the natural log of *Jsc*. Efficiency is directly related to the product of *Jsc*, *Voc* and fill factor (*FF*), a term that incorporates the effects of series and shunt resistance (*Rs*, *Rsh*). Efficiency can therefore increase with concentration as long as the increases in *Jsc* and *Voc* outweigh the decrease in *FF* due to $Jmax^2Rs$ power loss [1]. Factors contributing to *Rs* include the resistance of the front contact grid fingers, the metal-semiconductor contact resistance, and the sheet resistance of the semiconductor material. *Rs* can be reduced by increasing the quantity of the grid fingers, however, this will also increase the power loss due to shadowing of the junction by the metal contacts. Martin Green provides a set of equations that describe the fractional power loss due to both the resistive mechanisms and shadowing based on semiconductor and process parameters [1]. Given the sheet resistance of the emitter, the resistivity of the grid fingers, specific contact resistance, and expected *Jsc* and *Voc*, a front contact grid can be designed to peak in efficiency at a particular concentration where resistive loss begins to dominate.

II. Theory

A model presented in Green [2] provides a series of equations (1-6) describing the various mechanisms of power loss that can be attributed to cell fabrication. Definitions of terms can be found in **Error! Reference source not found.**I. Some of the power losses are based on resistive loss, which in the case of (1, 2) can be reduced by increasing the width of the metal lines, or in the case of (3) by reducing the spacing between fingers. Other losses are due to the metal grid blocking radiation from penetrating the semiconductor and creating electron hole pairs, also known as shadowing. Shadowing losses are minimized by decreasing metal thickness or increasing finger spacing. Resistive losses must increase to decrease shadowing losses and vice versa. To mitigate the power losses, an iterative approach may be used to find local minima based on process limitations and material properties.

$$p_{rf} = \frac{1}{m} B^2 \rho_{smf} \frac{J_{mp}}{V_{mp}} \frac{S}{W_f} \tag{1}$$

$$p_{rb} = \frac{1}{m} A^2 B \rho_{smb} \frac{J_{mp}}{V_{mp}} \frac{1}{W_b} \tag{2}$$

$$p_{sf} = \frac{W_f}{S} \tag{3}$$

$$p_{sb} = \frac{W_b}{B} \tag{4}$$

$$p_{cf} = \rho_c \frac{J_{mp}}{V_{mp}} \frac{S}{W_f} \tag{5}$$

$$p_{tl} = \frac{\rho_s}{12} \frac{J_{mp}}{V_{mp}} S^2 \tag{6}$$

TABLE I: DEFINITIONS OF TERMS EQUATIONS 1-6

	Description	Unit
p_{rf}	resistive power loss, fingers	%
p_{rb}	resistive power loss, busbar	%
p_{sf}	shadowing power loss, fingers	%
p_{sb}	shadowing power loss, busbar	%
p_{cf}	resistive power loss, finger ohmic contact	%
p_{ctl}	resistive power loss, lateral emitter current	%
M	geometric term based on grid design	--
A	length of busbar; length of cell	m
B	length of finger; width of cell	m
ρ_{smf}	sheet resistivity of metal fingers	ohm/sq
ρ_{smb}	sheet resistivity of metal busbar	ohm/sq
ρ_c	specific contact resistance	ohm*cm2
ρ_s	sheet resistivity of emitter	ohm/sq
J_{mp}	current density at maximum power point	mA/cm2
V_{mp}	voltage at maximum power point	V
S	finger spacing or pitch	m
W_f	finger width	m
W_b	busbar width	m

III. PROCEDURE

Data from Transmission Line Measurement (TLM) pads on a GaAs *p-i-n* solar cell was used to determine the sheet resistance of the p-GaAs emitter and the specific contact resistance. Existing concentration measurements of *Jsc* vs Suns and *Voc* vs Suns of a GaAs cell was interpolated to determine reasonable current and voltage values at concentration levels of 1x, 25x, 50x, 100x and 200x. This information was used in conjunction with a BASIC program that iterated the aforementioned equations to converge on a grid spacing that balanced resistive loss with shadowing loss at each of the above concentration values. A mask set was created containing two of each cell type, as well as the current NPRL concentrator design.

Single junction GaAs soalr cells on GaAs substrates were grown by organo-metallic vapor phase epitaxy (OMVPE) at NASA Glenn Research Center using standard precursors including trimethylgallium, trimethylindium, arsine, and phosphine

The wafers were cleaned in acetone and IPA, preceding two layers of LOR-10A lift-off resist applied via spin-coating. The resist stack was capped with a layer of Shipley 1813 photoresist and the front side metal contact grid was patterned with a Karl Suss MA56 contact aligner. After development, the wafers were loaded into a KJL Nano38 thermal evaporator for p-type GaAs ohmic contact metallization consisting of a stack of Au/Zn/Au totaling approximately 2μm – the thickness of the LOR stack. The wafers were processed in Remover PG to dissolve the remaining lift-off resist, taking the rest of the evaporated metal with it.

The wafers were then coated with Shipley 1813 again and active areas are patterned around the top contacts. After development, the wafers were subjected to a wet chemical MESA etch to remove all material around the perimeter of the diodes. This etch is dual purpose: it defines the active area of the devices at $0.5cm^2$, as well as electrically isolate the cells from each other. GaAs was etched in 3:4:1 H_3PO_4:H_2O_2:H_2O and InGaP was etched in 5:1 HCl:H_20. The photoresist was stripped and the GaAs contact layer is etched using 1:2:40 NH_4OH:H_2O_2:H_2O. This is a slow but fairly anisotropic etch for GaAs which helps to prevent undercutting of the grid fingers.

The front side of the wafer was protected by a final coat of photoresist, and the wafers were loaded upside down into a KJL PVD75 thermal evaporator and n-type GaAs ohmic contacts of Au/Ge/Ni/Au were deposited. The devices were annealed in a tube furnace at 400°C for 5 minutes to create backside ohmic contacts.

Devices were tested using an Agilent B1500A Semiconductor Device Analyzer and a Newport 450W Solar Simulator with an AM1.5G filter for illuminated J-V plots at 1-sun. Prior to testing, the lamp was calibrated using a standard GaAs cell calibrated to the AM1.5G spectrum at National Renewable Energy Lab (NREL). This spectrum follows the ASTM E892-87 standard for terrestrial solar cell applications. After testing at RIT, the cells were taken back to NASA for concentration measurements on a Large Area Pulsed Solar Simulator (LAPSS). The devices were measured until there was a peak in the efficiency, however during analysis an error was identified in the determination of efficiency resulting in some devices not tested until a peak was reached. Efficiencies were calculated using a geometrical term derived from the $1/r^2$ intensity relationship between the light source and the cell.

IV. RESULTS

As expected, *Jsc* exhibited a linear increase with concentration (1), while the *Voc* exhibited an increase as the natural log of concentration (2).

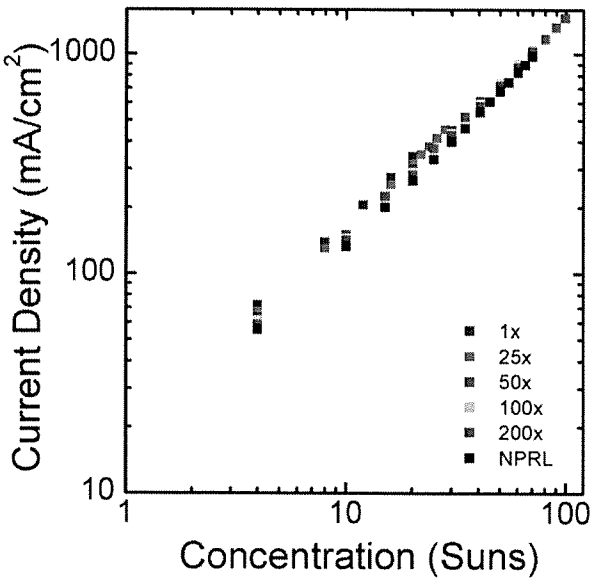

Fig. 1: Current density increases linearly with increased concentration.

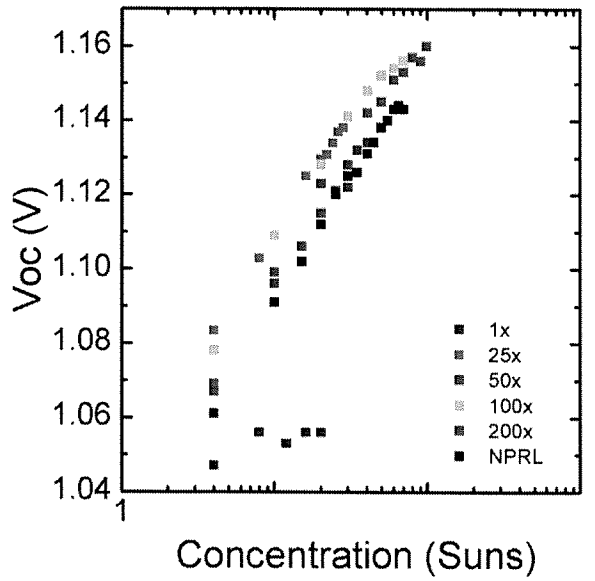

Fig. 2: Open circuit voltage increases as the natural log of concentration.

The fill factor for each cell type peaked before designed concentration, with designs for higher concentrations peaking after lower concentration designs (3).

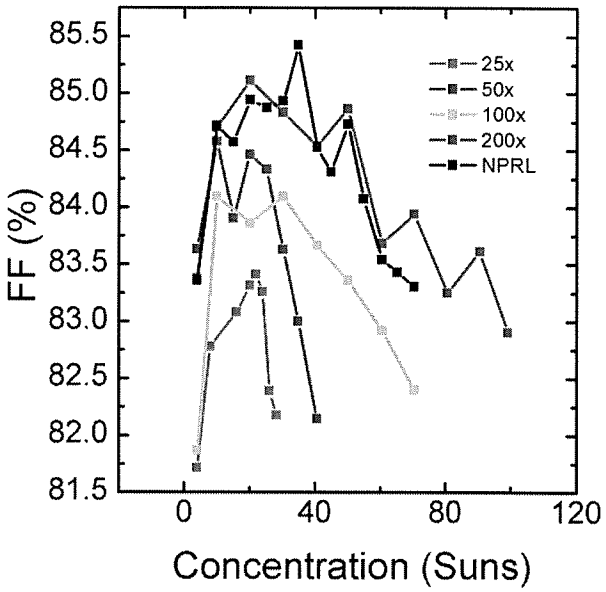

Fig. 3: Fill factor response of increased concentration.

Finally, the efficiency for each cell shows and increase with concentration, except the 1x design which peaked at a value less than or equal to one sun (4).

Table II shows the 1-sun efficiencies, as well as the highest efficiency observed for each cell type, as well as the percentage improvement over the 1-sun value. Table III displays what the concentration was for the efficiency peak, if any, for each device type as well as the measured series resistance of each.

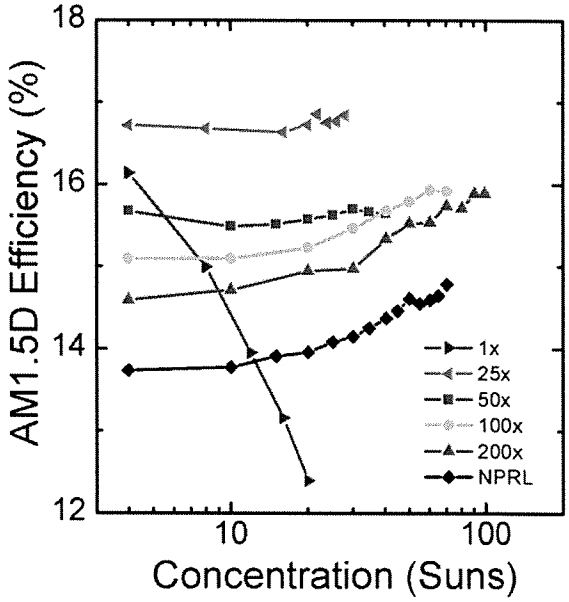

Fig 4: Efficiency response of increased concentration.

TABLE II: EFFICIENCY VALUES OF AT 1-SUN AND AT PEAK

Design	1-Sun Efficiency	Highest Efficiency Observed	Improvement Over 1-sun
1x	16.32%	16.32%	0.00%

25x	15.65%	16.86%	7.70%
50x	14.80%	15.70%	6.08%
100x	14.37%	15.93%	10.86%
200x	13.46%	15.89%	18.05%
NPRL	12.75%	14.78%	15.92%

TABLE III: CONCENTRATION AT PEAK EFFICIENCY AND SERIES RESISTANCE

Design	Concentration at Peak Efficiency	Series Resistance (Ω)
1x	<= 1x	3.1
25x	24x*	0.139
50x	30x	0.104
100x	60x*	0.086
200x	--	0.061
NPRL	--	0.085

ANALYSIS

Table II shows the 1-sun efficiencies, as well as the efficiency peaks, of the devices created. Not surprisingly, the 1x cell performed the best, with 200x the worst, at 1 sun. The shadowing loss of the cells designed for higher concentrations significantly impacted the *Jsc* at 1 sun. Under concentration, the 1x efficiency began to decrease immediately, while the 50x design peaked at 30x. The peak of the 25x and 100x designs may be 24x and 60x respectively, but higher peaks may be possible. The NPRL and 200x designs did not exhibit a peak within the range tested, though all new designs operated at higher efficiencies than the NPRL design. While a small offset in efficiency peak can be attributed a higher than expected emitter sheet resistance, the results indicate interpolating one design for Voc and Jsc values to create contacts designed for different concentrations.

Another method of designing cells can be found in [3]. This uses a distributed SPICE model incorporating many repetitions of both illuminated and grid-connected solar cell models. Each of these models represents a unit of approximately one square micrometer of the entire device. To accurately model the devices tested in this experiment, over 750 million individual circuit components would have been used. Severe shunting problems occurred while trying to scale this model to reduced complexity while (which also would have decreased accuracy). Ultimately, the model proved fruitless though work continues to find a viable means of simulating (and ultimately designing) future cells with the help of SPICE. This would remove the need to estimate the operating conditions of the maximum power point at the designed concentration, as these values would be determined numerically through the simulation.

By overlaying non-illuminated J-V with a Voc vs. Jsc plot, a lumped *Rs* can be found through the change in voltage between the two. The results**Error! Reference source not found.** show the cell designed for 1-sun has the largest resistance, while the 200x cell has the lowest, as would be expected based on the design.

V. CONCLUSION

Front contact grids were designed based on previously fabricated cell data, for 1x, 25x, 50x, 100x, and 200x concentration. For cells designed to operate at higher concentrations, an increase in efficiency was shown, but due to a miscalculation in efficiency not all cells were tested out to their efficiency maximums. Of the cells that did reach a maximum, only the 1x and 25x designs peaked near where they were intended to peak. The discrepancy was attributed to using extrapolated and interpolated data from one specific concentrator design to help create the range of designed used in this experiment. For this method to work properly, many designs need to be created, fabricated, and tested in iteration to determine a true optimal design.

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