Design & Fabrication of an 8 Bit ADC

Garret Phillips

Abstract— **MEMs devices at RIT utilize off chip circuitry to be properly utilized. This paper purposes an eight bit successive approximation analog to digital converter (ADC) to add to said devices as to simplify their operation. The ADC was designed and simulated using Mentor Graphics and Winspice software for the digital and analog components respectively. Lay out was then performed for the device as well as a simplified three bit version and various test circuits. Fabrication was done in the RIT SFML using RIT's Sub-μ CMOS process, which uses a 2μm gate length. Functional transistors and simple devices were realized. It was found that any device relying on Metal 2 did not work as desired as misprocessing post Via 1 etch left a 34nm barrier layer between the Metal 1 and Via 1 layer.**

I. I. INTRODUCTION

CURRENT MEMs devices exist at RIT, but require external circuitry to be properly utilized. The addition of an on chip analog to digital converter (ADC) would simplify the use of such MEMs devices. The construction of an eight bit successive approximation ADC has been purposed to meet this criteria. The ADC has been designed and simulated in Mentor Graphics and WinSpice software using RIT's Sub-CMOS 2μm technology. After layout and mask making, the device, along with a simplified three bit version and test devices has been fabricated in the RIT SMFL. The successive approximation architecture was chosen as the amount of analog circuitry is minimal, which is critical as the current BSIM 3 models for this technology lack proper testing. Figure 1 shows the block level diagram of the circuit.

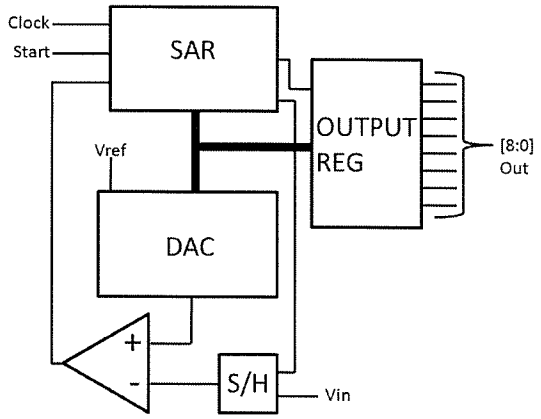

Figure 1: Successive Approximations ADC

II. THEORY

Analog to digital converters are useful in that they convert an analog signal to a digital signal, as the name implies. Although multiple architectures exist today, the successive approximation architecture was chosen for this application as it minimizes the amount of analog components needed. This was to enhance the success of the project as the device models for this technology have not been properly tested. Other ADCs were researched such as single or dual slope ADCs but were dismissed as the conversion rate was not seen as adequate for this application, despite their high resolution.

It can be seen (Figure 1) that the analog input is fed into a sample and hold circuit. When the Start pin goes low, this S/H circuit holds the current value of the input until the conversion is complete. The SAR then sends a digital word to the DAC to output one half the reference voltage. This voltage is compared against the analog signal and the comparator outputs a 1 or a 0 depending on which is larger. If the DAC voltage is larger the comparator outputs a 1 and bit zero in the SAR gets reset to zero. Bit one is then set to one in the SAR and output again to the DAC, which itself outputs a quarter of the reference voltage. If the analog signal is larger than the DAC voltage the comparator outputs a 0, which does not reset the current bit in the SAR. This happens eight times for the entire conversion to take place. The resulting SAR digital word eventually converges on analog input voltage. A graphical situation like the one just mentioned can be seen in Figure 2.

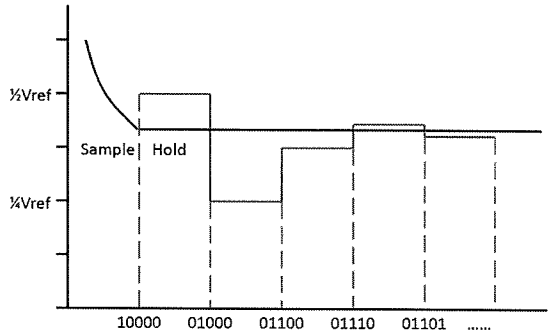

Figure 2: Ideal Operation

The digital portion of the design includes the SAR, and Output Register sub circuits. The main consideration of these components is the area taken in the final chip. The base layouts were taken from work performed in a previous class (EMCR 520). However, the area required was too large for the final design space, and modifications had to be made, especially in the SAR. Another constraint was to not route in polysilicon, as the sheet resistance is very high (>100 ohm/sqr). Any poly that was not over a channel was widened in attempt to reduce the overall resistance. Attempts to enhance yield was made by keeping far above minimum widths and lengths in geometries used, as well as including redundant vias and contacts where possible.

The analog portion of the design includes the Comparator, 8 Bit DAC, Sample and Hold, and Reference Buffers. Significant attempts were made to design for robustness as the models used were in question. The main thought was to keep the designs simple, staying away from unneeded circuitry that could ruin the device. The same two stage operational

amplifier was used for both the Comparator and DAC. This allowed more time to be focused on one design rather than two different ones. Further, the DAC architecture used was a simple 2R/R resistor ladder network. This was chosen for two reasons. First, for simplicity, as the output of the latter network in feed into a unity gain buffer (two stage amp). Second, the 2R/R values were chosen as it allows for designing resistors that are matched well together. The actual values of the resistors are not nearly as critical as the variation between them. This is important as the poly sheet resistance (poly resistors) has seen lots of variation over time.

Much time was devoted to the two stage amplifier as its performance is thought have a significant impact on the overall performance of the ADC. Two very important parameters were to design for a small offset voltage, as well as zero to five volt operation.

A capacitor module was needed for two of the analog sub circuits. One is necessary for the sample and hold input circuit, and the other is need for compensating an amplifier that utilizes negative feedback. The RIT Submicron CMOS technology does not include any such characterized element. Therefore, one constraint was to devise a suitable capacitor for both situations. It was found, due to area constraints, that n-type polysilicon over an nwell with gate oxide in between would be suitable for such capacitors. The thin oxide provides a high capacitance which minimizes the total area needed. Also, the applied signal will not reach below zero volts, so inversion of the substrate in not an issue. Substrate contacts were made with n+ regions in the wells. Although this equates to a high resistance at one terminal (low substrate doping), it was the best solution for this situation.

II. III. Results and Analysis

Figure 3 shows the results of the simulation for the ADC preformed in Accusim. It can be seen that the device is operating as expected and as described in the theory. That is, the DAC voltage converges onto the applied analog signal over time. Also shown is the serial data output, which is the inverted signal coming out of the comparator.

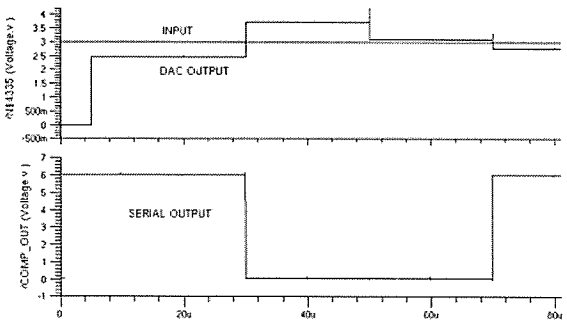

Figure 3: Simulation Results for ADC

Figure 4 shows the simulation results for the digital to analog converter. In this figure the input in the converter is swept from all zeros to all ones. It is seen that the corresponding output voltage is as expected, zero volts to five volts. Two different treatment combinations were performed for the poly sheet resistance, 30 ohm/sqr and 100 ohm/sqr. Figure 4 shows that both cases behave closely and as expected.

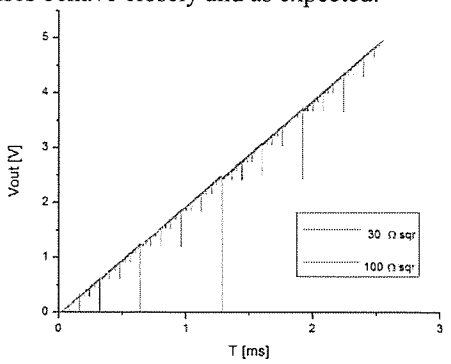

Figure 4: DAC simulation

Figure 5 is the same plot as Figure 4 but zoomed in to examine the DAC transition around 2.5 V output. The 30 ohm/sqr simulation is seen to have a worse response than the 100 ohm/sqr. This is shown through the linearity of the output as the 100 ohm/sqr does not drop as much as the 30 ohm/sqr.

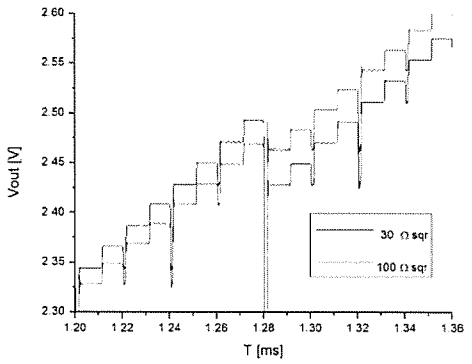

Figure 5: DAC simulation

Figure 6 shows the simulation results of the two stage operational transconductance amplifier (OTA). In this plot, but magnitude and phase of the device can be examined. It is found that the gain of the amp was 61.6 dB with a phase margin of 66^0. It must be noted that this is with the 'PMOS' compensation capacitor. This demonstrates that the amp is stable, even when used in the unity gain configuration. The bandwidth was also found to be 9kHz. It could be thought that these results are low and a better amplifier could easily be designed. As this might be the situation, timeliness and robustness were the leading factors during the design. It is seen that when the amp is used as a buffer (unity gain) the frequency can go into the MHz region. Also, when it is used as a comparator no compensation capacitor is necessary and the frequency response of Figure 6 is invalid.

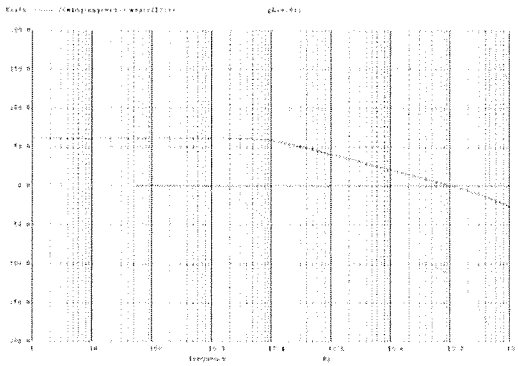

Figure 6: AMP simulation

Figure 7 shows the results of the comparator simulation. In this plot, one input is held at a constant voltage (2.5 V) and the other input has a small sin wave applied to it. The output shows the ideal response in that when the one input is larger than the other the output is at Vdd (6V) or when it is lower, the output is at 0V.

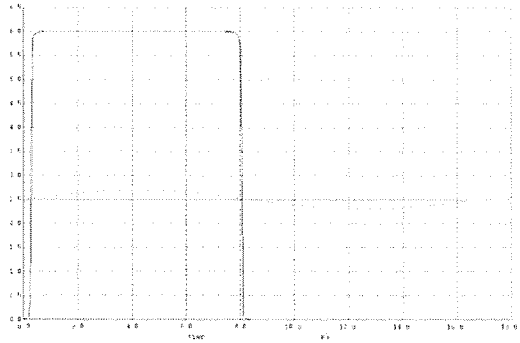

Figure 7: Comparator simulation

Figure 8 shows the comparator output during transistion between high and low state. From this figure it can be seen that there is about a 20mV offset at the output. That is, the output changes state when the inputs are 20mV apart. This is not ideal as the transition should occur when the inputs are equal, and could lead to a decrease in resolution. For this converter the 8 bits with a 5V references correlates to 19.5mV steps between increments. The 20 mV offset in the comparator could reduce the 8 bit resolution to 7 bits.

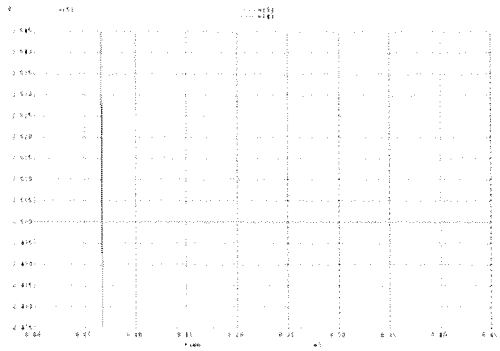

Figure 8: Comparator simulation

This device was then laid out using Mentor Graphics software. Layout for each individual component was performed on its own, but with the overall design in consideration. The placement of each component in the overall design was first decided before any layout took place. This way, when doing the individual layouts, these shape and area constrains could be taken into consideration. Figure 9 shows the layout of the entire chip as well as the simplified three bit version.

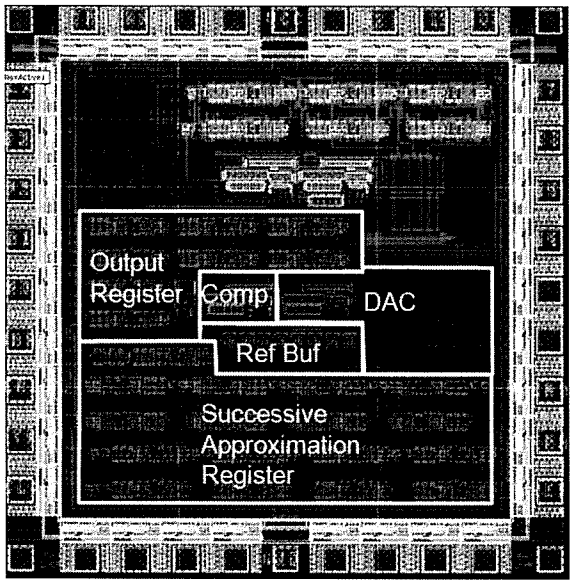

Figure 9: Entire Chip Layout

Many design considerations had to be accounted for during the layout phase of the project. The digital sub circuits such as flip flops were taken from a previous class (EMCR 520) but were modified to save space. Resistor matching was utilized in the DAC as well as the use of dummy resistors to ensure proper resistor values. Multiple fingers and interdigitation were also used in the two stage OTA for reduced parasitics and better matching.

This device was then fabricated using RIT's Sub-μ CMOS process at RIT. This single work function technology uses an etched gate length of 2μm. It features LOCOS isolation, Lightly Doped Drains, and two level metallization. The entire process has 13 level of lithography and a total of 78 process steps. Figure 10 shows a labeled SEM cross section of a fabricated transistor from this process.

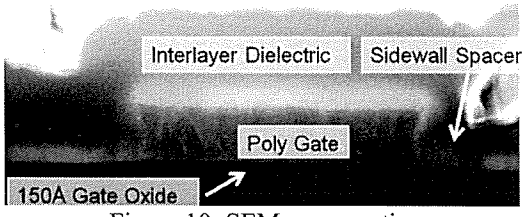

Figure 10: SEM cross section

Figure 11 shows a family of curves for both a PMOS and NMOS device. This demonstrates working transistors from the

processing performed. These results are as expected and match previous results found for this process.

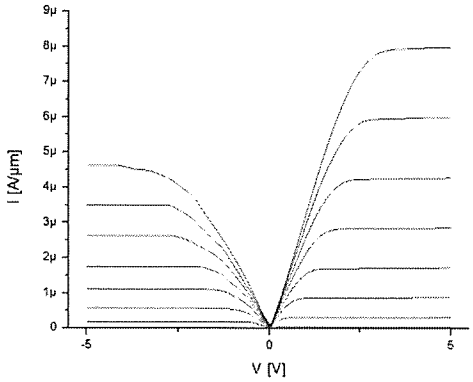

Figure 11: Family of Curves

Figure 12 shows the results of the reference buffer sub circuit. It is seen that this device behaves as intended in that when Vin is low, Vout is low, and when V in is high, Vout is at Vdd. It can be seen that the transition between the high and low occurs just above 3V which is higher than the ideal 2.5V, which could be caused by a mismatch in transistor sizing.

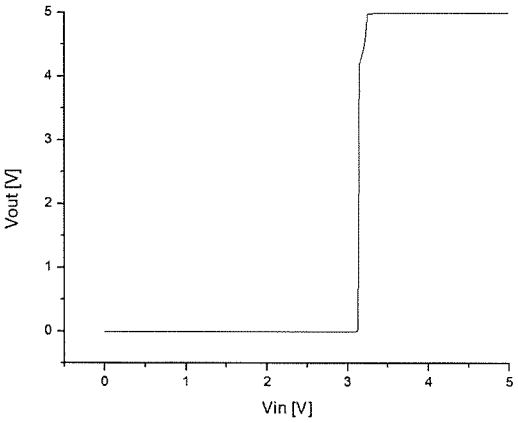

Figure 12: Reference Buffer

It was found that any device relying on the Metal 2 layer did not work. A faulty Via 1 etch was determined to be the culprit of this problem. Figure 13 show the I-V results of a 512 via chain. It can be seen that there is a resistive trend as the voltage is increased over the chain. Unfortunately though, the current drawn is in the pA range, suggesting that there is an unwanted insolating layer between each via. This was then verified through SEM images.

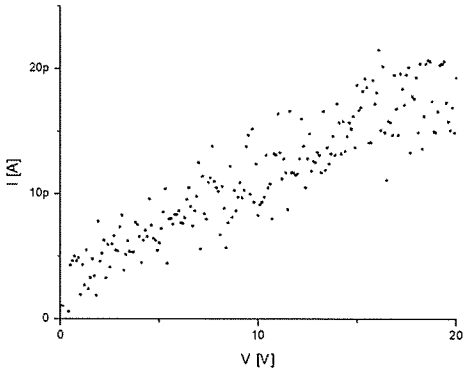

Figure 13: Via chain results

Figure 14 shows the resulting SEM cross section of a via. It is thought that the 34nm barrier layer is Alumina which is caused by an O_2 plasma step used to remove photoresist.

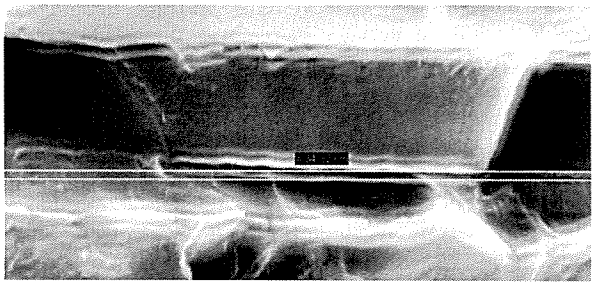

Figure 14: SEM cross section of Via A

III. IV. Conclusion

The goal of this lab was to design, simulated, layout, fabricate, and test an 8 bit successive approximation ADC. It was found that the device as well as a simplified three bit version were properly designed, being verified though simulation using BSIM3 models for the RIT process. Layout was then performed using Mentor Graphics software for the circuit as we all individual sub circuits. The chip was then fabricated using RIT's Sub-µ CMOS process. Working transistor were realized as well as simple devices. Unfortunately any device using Metal 2 was found to not work as a result of misprocessing post the via etch step.

References

1. Hoeschele, D. F. (1968). *Analog-to-digital, digital-to-analog conversion techniques.* New York: Wiley.