Process Design & Development of Contact Cut Double Patterning

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Abstract—**Optical double patterning allows for increased quality control over varying film stacks as well as allowing photolithography equipment to image smaller dense features. This is done by splitting dense patterns into two separate masks. A contact cut layer double patterning process was developed, and proved to be successful down to contact density of 4 µm CD by 4 µm density (4x4 µm CD x Density). Conventional dark field double patterning processes use two separate substrate etch steps (one etch step after each pass of lithography). This project developed a dark field double patterning process which incorporated light field double patterning techniques, which in effect eliminated one of the substrate etch steps by thermally curing the first pass of photoresist. Thermal cure temperatures of first pass resist were varied from 125°C to 200°C, finding that temperatures less than 175°C did not sufficiently cross-link the resist enough to stand up to the second pass of lithography, resulting in loss of first resist patterns. Temperatures greater than 175°C caused the first pass lithography to flow, resulting in the elimination/minimizing of contact cut feature densities less than 4x4 µm. A successful contact cut (dark field) double patterning process was developed; however feature densities were limited due to the incorporation of light field double patterning techniques.**

Index Terms—**Contact Cut, Dark Field, Double Patterning, Feature Density, Light Field.**

I. Introduction

Optical double patterning has recently come to the forefront in semiconductor manufacturing technology as a means to meet the ever-tightening demands on half pitch duty ratios. Decreasing node technology requirements place a strain on the Rayleigh Half-Pitch Criteria of (1). From an optical standpoint of view, enabling decreased node-technology fundamentally comes down to being able to continually scale the Rayleigh Criteria to allow for enhanced half-pitch resolution.

$$R = hp_{\min} = \frac{k_1 \lambda}{NA} \tag{1}$$

In order to drive down half pitch resolution it follows that either source wavelength (λ) can be decreased, or lens numerical aperture (*NA*) can be increased. Extreme Ultra-Violet (EUV) source technology, the long anticipated means to scale λ, may not be ready by the time the semiconductor manufacturing industry needs it to enable the 22nm node. Immersion lithography continues to scale objective lens *NA* by allowing for the collection of higher order diffraction pattern information within imaging media of higher indices of refraction, but is hindered from going forward by resist processing/chemical problems with various liquids used and is currently limited to H_2O-immersion for manufacturing applications.

Double patterning serves to scale the process dependent factor (k_1) of the Rayleigh Criteria by splitting the patterned layer into two separate, less dense exposure passes thus increasing the pitch (and duty ratio) for each exposure and allowing the tool to image with enhanced performance. This allows for greater half-pitch resolution imaging capability by the photolithographic equipment due to pitch doubling (splitting the dense half pitch features onto two separate masks requiring two separate passes of lithography). Properly aligning and overlaying both passes of lithography to each other theoretically enables the photolithographic equipment to accurately image half pitch features smaller than the constraints placed by the Rayleigh Criteria. This is enabled because of the two separate passes of lithography, each with increased pitch (also referred to as pitch doubling). For the optical double patterning technique to work, excellent alignment of the photolithographic equipment is required.

II. Theory

A. Double Patterning vs. Double Exposure

Double patterning utilizes two separate coatings of photoresist – each with their own separate image captures. Double patterning processes are therefore much more complex than conventional single pattern process, due to multiple photoresist processing steps. However, for double patterning processes with conventional (linear) photoresists, multiple coatings are absolutely required [1]. That is, one cannot expose the same coating of conventional linear photoresist twice when using mask features shifted by half pitch from each other on separate masks. This is because such photoresists exhibit a 'resist memory effect,' where areas around the fully exposed regions actually receive sub-threshold exposures [1].

The basic idea of double patterning is to split the dense half pitch features of one pattern into two different masks, thus doubling the pitch for each exposure. Therefore, each of these separate masks is shifted by half pitch relative to the other.

Photoresist captures the aerial intensity image reconstructed by the objective lens. A normal objective lens in the

photolithographic tool is usually designed with an *NA* sufficient enough to capture the 0^{th} and $\pm 1^{st}$ diffraction orders. Capturing these diffraction orders results in an aerial image intensity modeled by (2), which is a sinusoidal function.

$$I_{1stPass} = A\cos^2\left(\frac{\pi \cdot x}{pitch}\right) + B \tag{2}$$

Suppose that for the second pass exposure, the mask pattern is shifted by half pitch. Shifting this mask function by half pitch corresponds to a shift in the aerial image intensity by a phase factor of π/2, resulting in a sinusoidal function identical to that of (2), but shifted 90° and completely out of phase (3).

$$\begin{aligned} I_{2ndPass} &= A\cos^2\left(\frac{\pi \cdot x}{pitch} + \frac{\pi}{2}\right) + B \\ &= A\sin^2\left(\frac{\pi \cdot x}{pitch}\right) + B \end{aligned} \tag{3}$$

Therefore, if both aerial intensity functions (2) and (3) are captured in the same coating of photoresist, the final aerial intensity function (the addition of both aerial intensities) is simply a constant, as modeled by (4). With no variation in the final aerial image intensity captured by the photoresist, there is no final image transfer.

$$I = I_{1stPass} + I_{2ndPass} = A + 2B \tag{4}$$

With conventional photoresist, the shifted aerial image intensities of (2) and (3) *must* be captured in separate coatings. This is commonly referred to as the double patterning technique. Capturing the aerial image intensities of (2) and (3) in the same coating of photoresist is referred to as the double exposure technique, and is only possible with costly, non-linear photoresists that do not exhibit the memory effect. However, materials cost make the double exposure approach much less economically viable than the double patterning approach.

Fig. 1 depicts the shifted sinusoidal aerial image intensities of (2) and (3), and how – when captured in the same coating of conventional, linear photoresist – they cancel each other out resulting in no final pattern transfer.

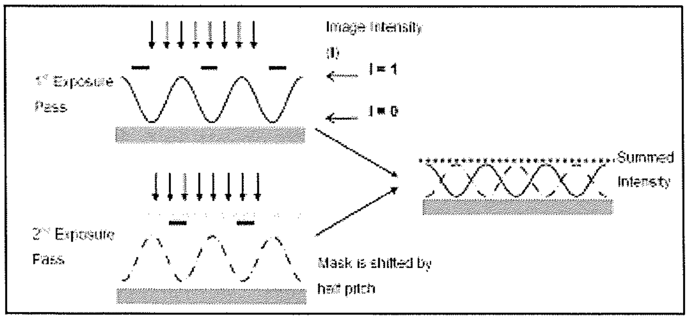
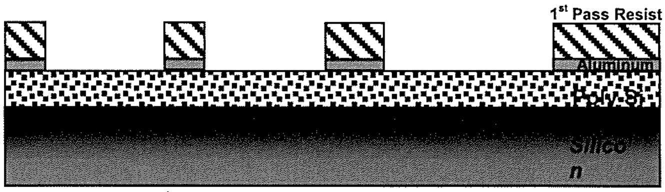


Fig. 1 Double exposure image intensity models shifted by π/2 phase factor, resulting in no final image transfer [1].

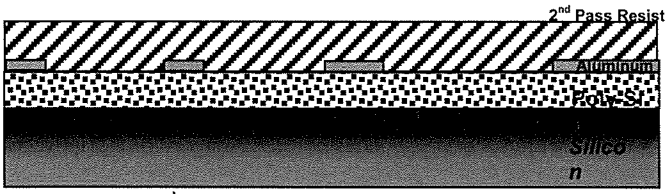
B. Clear Field Double Patterning Approaches

Perhaps the most conventional and widely used of the double patterning approaches is the clear field double patterning method. Patterning of mesas (lines) is done through the use of clear field masks, in which the critical features themselves receive no exposure dose. The pattern is then etched down into the substrate under the exposed areas, leaving the final mesa pattern.

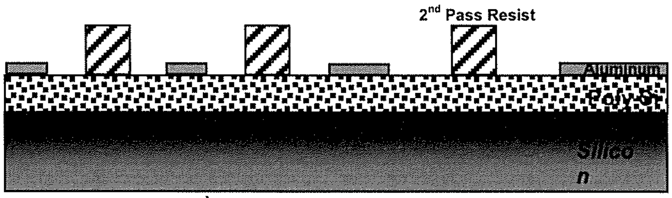
Fig. 2 illustrates the most widely used clear field double patterning approach, where the first pass lithography is imaged, developed, and etched into an underlying hardmask (e.g. Aluminum), which sits atop the actual substrate that needs the final pattern transfer (e.g. polycrystalline Silicon). Then, the second level lithography is imaged and the substrate itself is etched – the hardmask material for first level litho *and* the resist lines from second level litho *both* act as the hardmask for the etch step of the substrate. Such a process focusing on double patterning of polycrystalline Silicon lines has previously been developed at RIT [2].



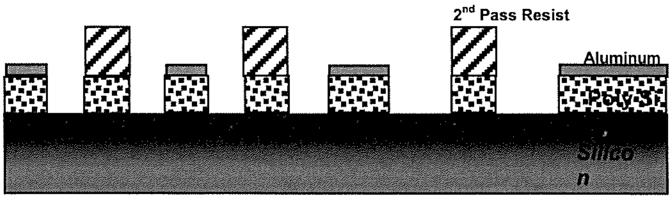
a. **Etch 1st pass pattern into Aluminum hardmask.**



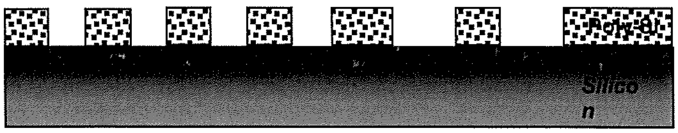
b. **Coat 2nd pass resist.**



c. **Perform 2nd pass lithography.**



d. **Etch polycrystalline Silicon substrate.**



e. **Ash resist, strip Aluminum hardmask – final pattern transfer.**

Fig. 2 Conventional light field double patterning technique of polycrystalline Silicon lines using an Aluminum hardmask.

Alternative process approaches have focused the elimination of the hardmask for clear field (mesa) double patterning through a 200°C thermal resist curing step for photoresist hardening [3]. The photoresist is coated over the substrate itself as with conventional lithography. Instead of etching the first level lithography pattern into an underlying hardmask layer, the photoresist pattern after development of the first pass lithography is hardened, and remains on the wafer during the second pass lithography processing. This is done by a flood exposure to completely crosslink the photoresist and eliminate all photo-active compound (PAC), following by a thermal cure step at a high temperature (200°C) to drive off all remaining solvent and harden up the photoresist lines to withstand the second pass lithography [3].

C. Dark Field Double Patterning Approaches

Widely used dark field double patterning approaches (of contacts, vias, or trenches) require no underlying hardmask protection, because two separate etch steps are required to transfer the pattern into the substrate (e.g. oxide) for each pass of lithography (Fig. 3).

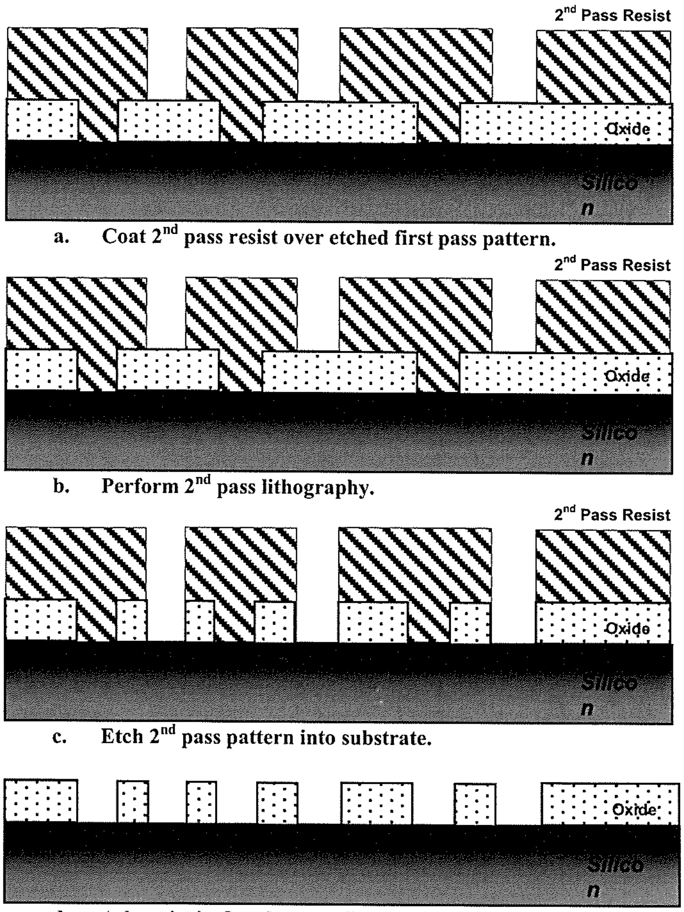


Fig. 3 Conventional dark field double patterning technique using the two etch LELE process on the substrate (LELE – Lithography Etch Lithography Etch).

The main difference between conventional clear and dark field double patterning approaches is that dark field approaches consist of two substrate etch steps (after each pass of lithography) while clear field approaches consist of only one.

III. Process Design

A. Contact Cut Double Pattern Process Flow

Initially, a process flow was designed by the author, incorporating both clear field and dark field double patterning approaches for the contact cut layer at RIT. The motivation behind development of this process flow was two fold – to allow for the resolvability of dense contact features, and allow for engineering critical dimension (CD) control over the different film stacks of the contact cut lithography layer. Additionally, the designed process flow sought to eliminate the intermediary substrate etch associated with dark field double patterning, through the addition of a thermal curing step of the first pass photoresist.

Fig. 4 depicts a cross-sectional schematic of the designed process flow for the contact cut layer.

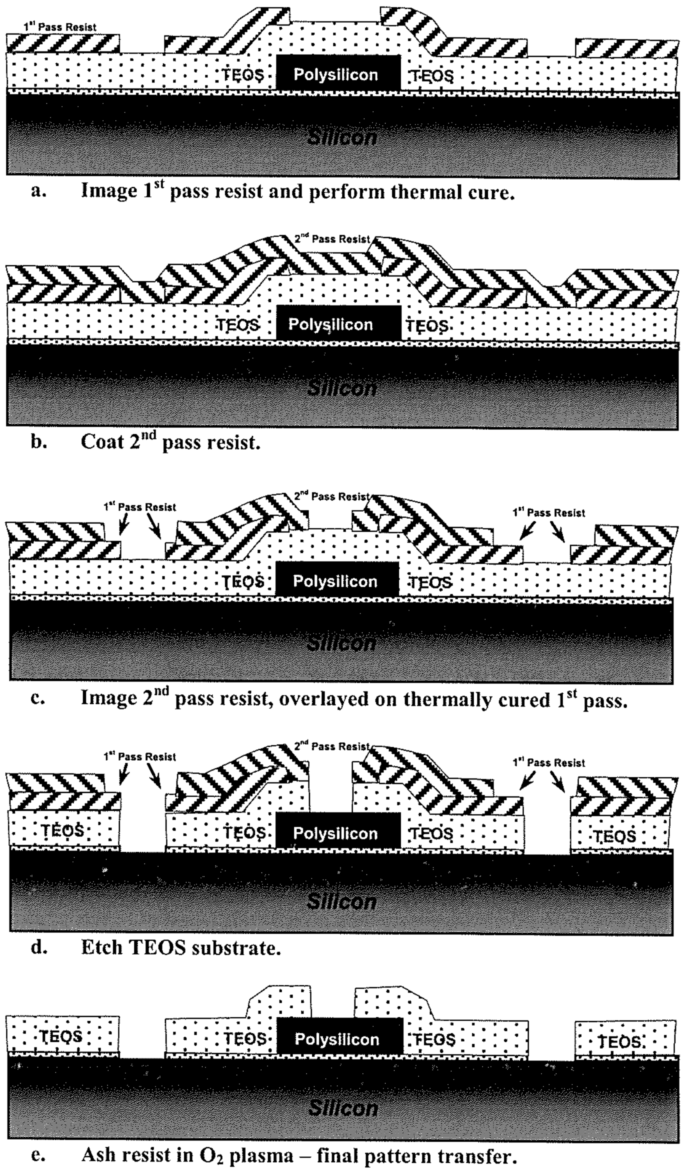


Fig. 4 Cross-sectional process design schematic for contact cut dark field double patterning with thermal photoresist hardening.

It should be noted that in Fig. 4, each pass of photoresist critically defines a certain set of contacts. The first pass lithography critically defines the Silicon (Si) contacts, while clearing an area for the polycrystalline Silicon (hereafter, poly-Si) contacts. The second pass does just the opposite – it critically defines the poly-Si contacts while clearing an area over the already defined Si contacts from the first pass lithography step. This is done so as not to block the final substrate etch.

For detailed processing step information, refer to the tabulated process flow of Appendix I.

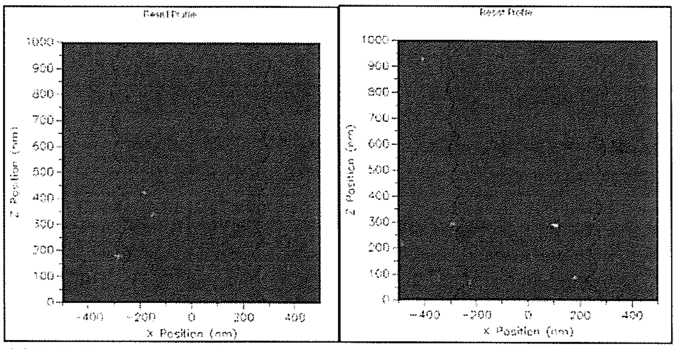
B. Lithography Simulations

Lithography simulations were then carried out using the *PROLITH* simulation software, in order to ensure viability of the resolution of contact cut feature sizes down to 1 μm with the equipment and materials available in the RIT Semiconductors and Microsystems Fabrication Laboratory (SMFL).

For this project, a Canon FPA-2000*i*1 *i*-line photolithographic stepper was used in conjunction with O*i*R620-10 *i*-line sensitive photoresist. The processing equipment corresponds to the following tool parameter inputs for the *PROLITH* simulations, where λ and *NA* correspond to the same parameters as in the Rayleigh Equation:

$$\lambda = 365nm$$
$$NA = 0.52$$

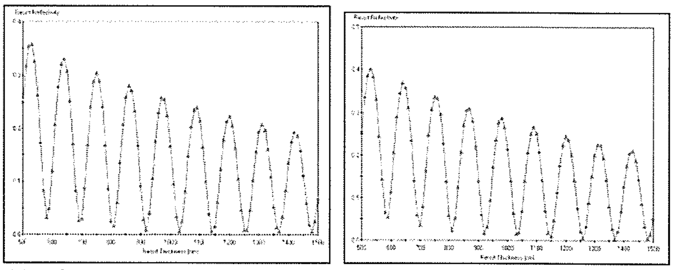
Contact CDs of 0.5 μm were simulated across both film stacks (Fig. 5), which corresponded to a dose of 305 mJ/cm^2 for the Si contacts, and 320 mJ/cm^2 for the poly-Si contacts.



(a) Poly-Si contact simulation *(b) Si contact simulation*
Fig. 5 *PROLITH* simulation CD results across the two film stacks.

Swing curves of reflectivity were also generated to simulate the CD variation across varying photoresist thicknesses (Fig. 6). Due to the high reflectivity of both types of film stacks, standing waves appeared in the photoresist. However, these waves were small compared to the overall CD of the features.

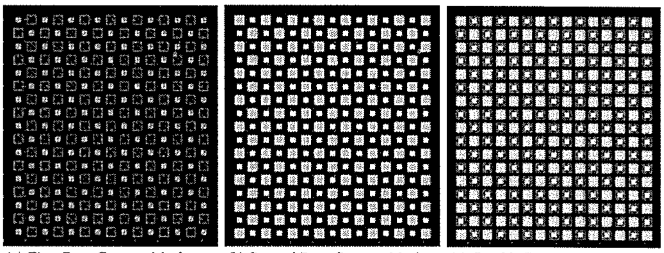
From the simulated results of Figs. 5 and 6, the project was determined to be theoretically viable down to CD features of 0.5 μm with the available equipment in the RIT SMFL.



(a) Poly-Si contact simulation *(b) Si contact simulation*
Fig. 6 *PROLITH* simulation swing curve results across the two film stacks

C. Mask Design

Pitch variation was incorporated into the mask design so that minimum successful pitches could be identified. Fig. 7 depicts one of the pitch variation grids on the mask design.



(a) First Pass Contact Mask *(b) Second Pass Contact Mask* *(c) Double Pattern Layout*
Fig. 7 Pitch variation grid mask design with two passes of contact cut lithography, using the designed dark field double pattern process with one substrate etch.

The mask layouts for the designed process flow for this project are non-conventional. This can be seen in Fig. 7. Normally, a grid of contacts would conventionally be designed on one mask. With the designed double patterning process, however, the first pass mask has defined contacts, but *also* has large areas that serve to clear out first pass photoresist where second pass contacts are to be defined. Similarly, this is true with the second pass mask. It defines contacts in the large areas in photoresist that were cleared out during the first pass of lithography, and it also clears out the second pass photoresist that covers up the already-defined contacts in the first pass lithography. These large areas are needed with a one-etch-step dark field double patterning technique, so as not to block the substrate etch. Fig. 7(c) depicts the non-conventional layout of the double pattern technique in this project.

Additionally, a large scale structure was created in order to demonstrate proof of concept for the process, and as a fallback to demonstrate the process in case the smaller features did not resolve. The thinking was that the success of this large scale layout should not be dependent on lithography processing parameters, such as exposure dose or focus.

Contact arrays were also laid out in the presence of poly-Si lines, and varied in pitch. This was done to simulate contacts over the different film stacks. The final die size of the layout was 10mm x 10mm consisting of 4 masks: poly-Si (first level), active contacts (Si contacts only – aligns to poly-Si pattern), poly-Si contacts (poly-Si contacts only, aligns to

poly-Si pattern), and a control contact mask which contained all contacts on the same mask.

IV. Processing Development

Included in this section are the areas in which processing development was required for the project, mainly with lithography and etch steps.

A. Polycrystalline Silicon Etch

Following the successful low pressure chemical vapor deposition (LPCVD) of 2000Å of poly-Si, a plasma etch development was required on the DryTek Quad Plasma Etching tool.

An existing recipe, entitled *EagleSi*, was used for this etch. Gas flows for this recipe were 40 sccms SF_6 and 40 sccms O_2. Since this recipe had never been used with the O*i*R620-10 photoresist, some etch development was needed. Photo-intensity readings were taken during the etch development on dummy wafers, so as to identify the endpoint (Fig. 8).

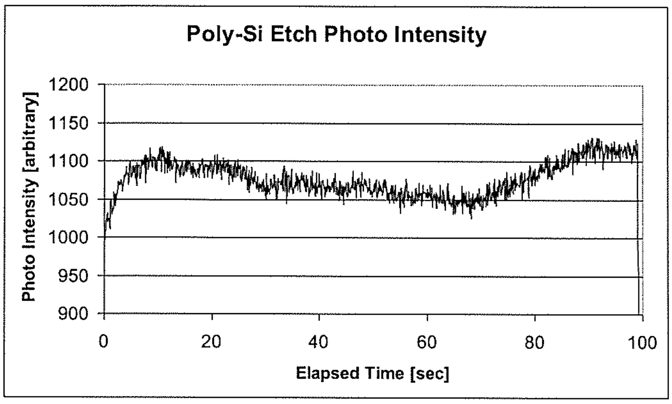


Fig. 8 Poly-Si etch endpoint development using the EagleSi recipe with 6" wafers and OiR620-10 photoresist.

The endpoint of the poly-Si etch can be seen on the graph, determined to be 92-94 seconds. All wafers for this experiment were etched at a time of 100 seconds (1:40 minutes), and poly-Si was verified to be fully removed across the wafer with etches of this time. Additionally, at the edges approximately 300Å of the initial 500Å gate oxide was removed as well.

B. First & Second Pass Contact Cut Lithography

The exposure dose and focus parameters were experimentally determined through the use of focus-exposure matrices (FEMs). An FEM for each film stack was shot on the Canon, and optimal focus and exposure parameters were determined visually from the matrix.

It was determined that the poly-Si contact layer resolved optimally (with a line resolution of 0.5 μm) with an exposure condition of 260 mJ/cm^2, and a focus offset condition of 0.00 μm. It was determined that the Si contact layer resolved optimally (with a line resolution of 0.5 μm) with an exposure condition of 280 mJ/cm^2, and a focus offset condition of 0.00 μm. These values were then used when shooting each respective contact cut mask.

C. TEOS Magnetically-Enhanced Reactive Ion Etch

Etch development was performed on dummy wafers in the AME P5000 tool using the Oxide MERIE chamber. The Oxide MERIE etch rate on bare TEOS (no patterned photoresist on top) was calculated to be 21 Å/sec. The etch rate on TEOS with patterned photoresist on top was found to be slightly lower – 15 Å/sec. This was the etch rate used in determining the time to etch each experimental wafer. Each experimental wafer to be etched was etched for a time of 240 seconds.

Each wafer had a starting TEOS thickness of approximately 4000 Å. The Oxide MERIE etch time was intentionally set to be low so as not to remove all the oxide (240 seconds removes approx. 3600 Å of the TEOS). To finish up the etch, an HF dip in 10:1 buffered oxide etch (BOE) with surfactant was performed. The etch rate of the 10:1 BOE with surfactant was calculated to be approximately 8 Å/sec. A 35 second dip in the 10:1 BOE removed most of the remaining oxide (approx. 100-300 Å was left, varying across the wafer).

The purpose of finishing off the etch with the BOE dip is so that the underlying substrate (poly-Si and Si) is not over-etched once all the TEOS is etched away. BOE has selectivity against poly-Si and Si.

V. Experimental Results

A. Proof of Concept

Initially, a proof of concept of the process was obtained in photoresist. Fig. 9 illustrates the top down view of successful double patterning at the photoresist level (prior to oxide etch), where the cutline corresponds to the cross sectional illustration Fig. 4(c). Fig. 10 further illustrates the large scale proof of concept of a double pattern in photoresist, where first pass lithography defines the Si contact (while clearing an area for the poly-Si contact), and second pass lithography defines the poly-Si contact (while clearing an area for the Si contact). This produces a double pattern final result equal to that of the control wafer, where both contact types are defined on the same mask.

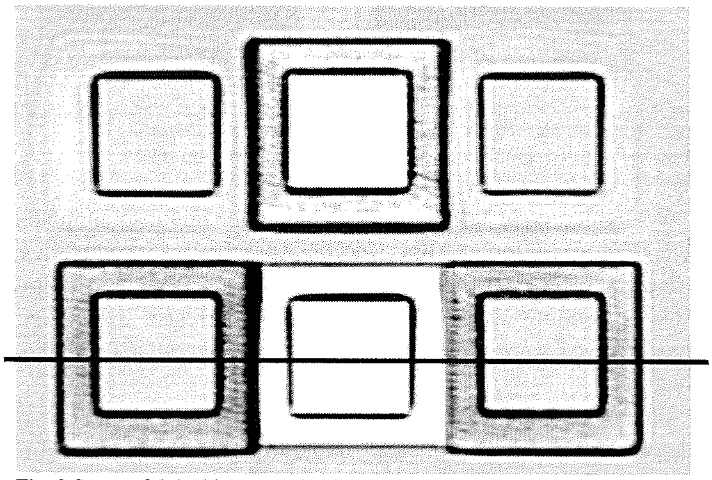
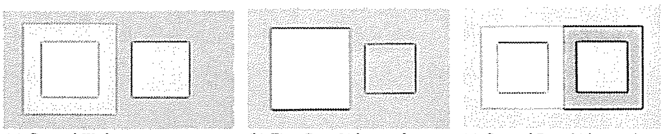


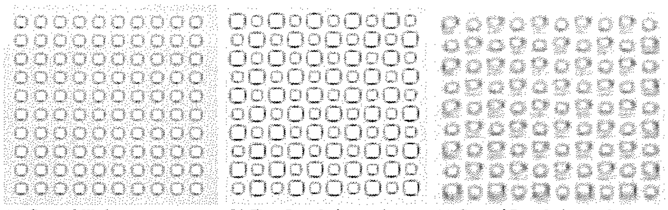
Fig. 9 Successful double pattern in photoresist. Cutline is the cross-section of Fig. 4(c).



(a) Control Wafer *(b) First Pass Lithography* *(c) Second Pass Lithography*
Fig. 10 Large-scale DP proof of concept in photoresist.

It should be noted that the CD features of Figs. 9 and 10 are very large (~25 μm). These were intentionally designed to be large on the mask, so as to be independent of any focus/exposure variability effects on the photolithographic tool. The large features of Figs. 9 and 10 were designed solely to illustrate a proof of concept of the process.

Additionally, a proof of concept of smaller features can be seen in Fig. 11 as compared to the control wafer with all contacts on a single mask.



(a) Control Wafer *(b) First Pass Lithography* *(c) Second Pass Lithography*
Fig. 11 Successful 5x5 μm dense contact arrays in photoresist.

The features of Fig. 11 are 5 μm CD with a 5 μm density. Second pass contacts appear to be slightly oblong due to slight y-misalignment of the second pass lithography, as seen with the alignment verniers of Fig. 12. This y-misalignment on the wafer was 0.5 μm, and contributed to second pass contacts (for this particular wafer) that were not fully landed in the areas of photoresist cleared for them in the first pass lithography step.

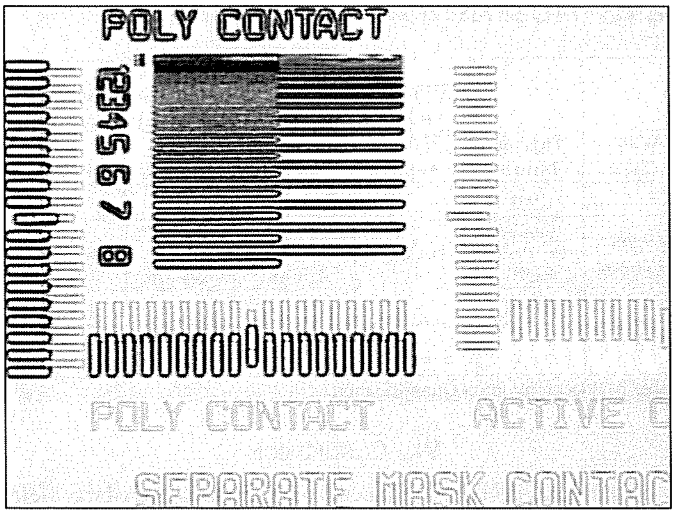


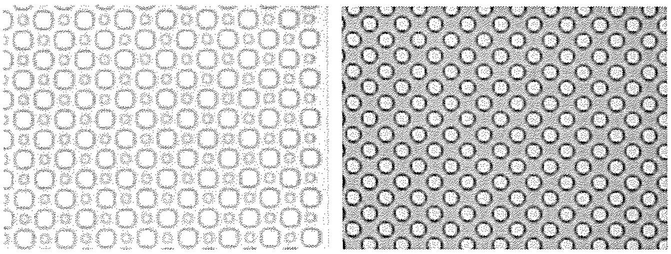
Fig. 12 Separate mask alignment, y-alignment is +0.5 μm. Second pass photoresist is coated over the active contact alignment marks.

In all, a successful proof of concept was obtained from the process in photoresist for larger features down to 4x4 μm.

B. Photoresist Reflow

It was observed that reflow from higher thermal cures (of the first pass photoresist features) caused smaller features to close up entirely. The first pass photoresist thermal cure was added into the process as a way to preserve first pass lithography and eliminate the intermediary substrate etch step in the dark field double patterning approach. This thermal cure was varied from 125°C to 200°C across four different wafers in steps of 25°C. All thermal cures were at a constant temperature for a duration of 90 seconds. It was determined that temperatures less than 175°C were not sufficient enough to cross-link and harden the photoresist to withstand the second pass lithography process – resulting in unclear/partially developed areas. Because of this, it was concluded that the high temperature thermal cure step (of greater than 175°C) was crucial to the process, but did cause the first pass photoresist to flow – resulting in a decrease in CD of the first pass features and in some cases, the elimination of smaller features altogether.

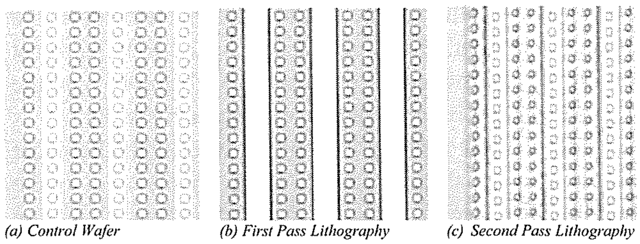
Fig. 13 illustrates the effect of the thermal cure on the first pass photoresist of a 2 μm CD feature grid.



(a) Before Thermal Cure *(b) After Thermal Cure*
Fig. 13 2x2 μm dense contact array after first pass lithography, illustrating the photoresist reflow induced by the 200°C thermal cure.

The small features of Fig. 13(a) are the 2 μm CD contact features, whereas the large features of Fig. 13(a) are simply the large open areas that allows an area for the critical definition of second pass contact features. From Fig. 13(b), it can clearly be observed that photoresist reflow induced by the high temperature thermal cure (in this case, 200°C), causes the elimination of the first pass contact features.

The designed double patterning technique was also applied to Si and poly-Si contacts in the presence of poly-Si lines, in which the Si contacts were imaged in the first pass lithography, and poly-Si contacts were imaged in the second (Fig. 14). First pass contacts of Fig. 14 are slightly minimized – likely due to the added thermal cure step of 200°C being well above the glass transition temperature of the photoresist itself.



(a) Control Wafer *(b) First Pass Lithography* *(c) Second Pass Lithography*
Fig. 14 4x4 μm contacts in presence of poly-Si lines.

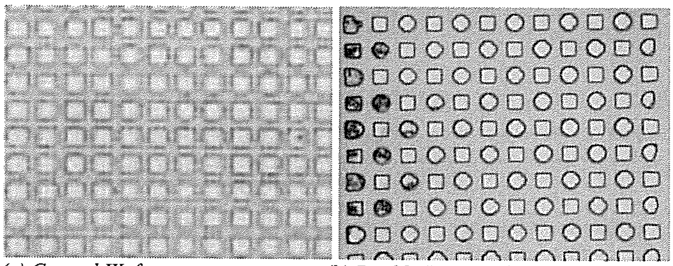
In the case illustrated in Fig. 14, the contact features (4 μm) are large enough to not be completely eliminated by the photoresist reflow induced by the thermal cure step, but were clearly affected.

It was concluded that removing one of the substrate etches through the addition of a thermal cure prevented final resolvability of contacts smaller than 4x4 μm due to the induced photoresist reflow.

C. Successful Pitch Quantification

Successful pitches were observed down to feature CDs and densities of 4 μm contacts, limited by the resist reflow induced by the addition of high temperature thermal cure step. On the control wafer, minimal feature CDs and densities were observed to be 1 μm.

Fig. 15 illustrates the double pattern in TEOS after the magnetically-enhanced RIE and photoresist ash in an O_2 plasma.



(a) Control Wafer *(b) Double Patterned Wafer*

Fig. 15 Control and DP contacts (5x5 μm) after oxide MERIE TEOS etch and photoresist removal

An every-other contact circular effect is evident in the double pattern of Fig. 15. This was due to the photoresist reflow as discussed previously, causing the contact features to become circular in photoresist (and thus etching circularly).

Scanning electron micrograph (SEM) images were also taken of the double pattern, both in photoresist (Fig. 16) and in TEOS after oxide etch and photoresist strip (Fig. 17). In Fig. 16, the positive y-misalignment is evident with the second pass photoresist pattern, further emphasizing the importance of alignment in a double pattern process.

Final tabulation of successful pitch quantification is expressed in Table I, as compared to the control wafer.

Insufficient thermal cure temperatures (i.e. under 150°C) did not cross-link the photoresist enough to stand up to second pass lithography, resulting in loss of patterns. High thermal cures were sufficient enough to cross link the photoresist, but induced reflow of the first pass pattern which prevented resolvability of smaller features (below 4 μm). However, the dark field double patterning approach designed in this project is useful if the ultimate aim is engineering CD control over the different film stacks of the contact cut lithography layer.

The control wafer itself was unable to resolve final contact CD features lower than 2 μm in TEOS, likely due to the substrate MERIE etch. Etching of dark field small feature sizes is challenging, due to aspect ratio dependent etch rates.

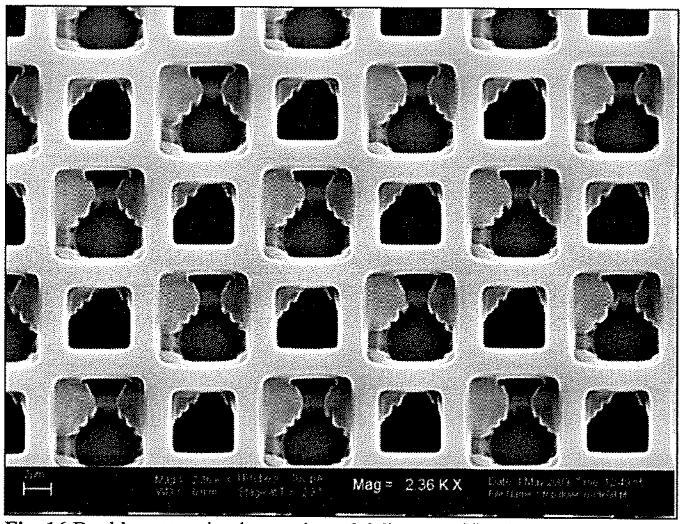


Fig. 16 Double pattern in photoresist at 2.36kx magnification.

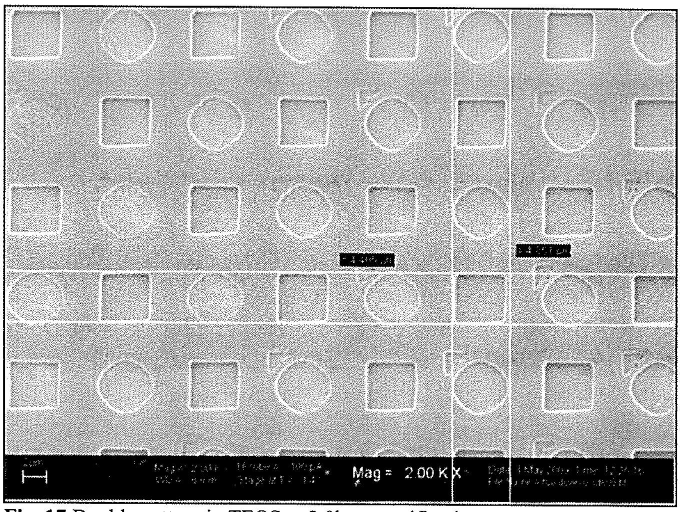


Fig. 17 Double pattern in TEOS at 2.0kx magnification.

Wafer Type	Thermal Cure	Minimum Resolvable 1st Pass Dimensions		Minimum Resolvable Final Dimensions	
		Before Cure	*After Cure*	*In Resist*	*In TEOS*
Double Pattern	125°C	1x1 μm	1x1 μm	n/a	n/a
	150°C		2x2 μm	n/a	n/a
	175°C		4x4 μm	4x4 μm	4x4 μm
	200°C		4x4 μm	4x4 μm	4x4 μm
Control	N/A	N/A	N/A	1x1 μm	2x2 μm

Table I: Successful Pitch Quantification

VI. Conclusion

Initially, a proof of concept of the designed dark field double patterning approach was achieved. The process successfully combined clear field and dark field double patterning approaches for application to a contact cut etch process in oxide.

After achievement of the proof of concept, smaller contact cut features were fabricated using the designed process. It was determined that (by virtue of eliminating the intermediary etch

in the dark field process) resolvability of smaller features was prevented. This was because of first pass photoresist reflow induced by the thermal curing (hardening) of the first pass photoresist pattern. It was also likely due to the fact that large features had to also be incorporated into the mask designs for both passes of lithography – these were needed in order to clear photoresist for the critical definition of features on the opposite mask. This prevented true 'pitch doubling' for the Rayleigh Equation. In clear field double pattern approaches, this problem does not exist since clearing out areas for features on the opposite mask is not needed.

Because of these process complications, if one is trying to achieve densities of dark field features past the physical limits of the photolithographic tool dictated by the Rayleigh Criteria, the two separate substrate etch (LELE – lithography-etch-lithography-etch) processes of dark field double patterning approaches are unavoidable. This is because in order to take full advantage of double patterning, true pitch doubling of the features needs to be done.

However, if the aim of the dark field double patterning process application is to allow for more engineering CD control over varying film stacks (as with the contact cut lithography layer), the designed process of this project can be utilized. Some additional engineering development would need to be applied, such as designing the first pass features to be slightly larger in order to account for the photoresist reflow through the thermal cure. Also, more focus on the thermal cure itself could be explored and engineered, such as a ramped bake to reduce the amount of first pass photoresist reflow.

Overall, the project was successful in combining clear field and dark field double patterning approaches, developing a unique dark field double patterning approach which eliminated the intermediary substrate etch step. The designed process can be used for CD control over different film stacks, and down to a feature density of 4 μm with a contact cut CD of 4 μm.

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APPENDIX I – PROCESS FLOW

Process Step	*Action*	*Required Equipment*	*Processing Details*
1	RCA Clean, Spin-Rinse-Dry	RCA Bench #2, SRD	-
2	Gate Oxide Growth	Bruce Furnace Tube #4	*Recipe:* #250, dry-ox *Target Thickness:* 500Å
3	RCA Clean, Spin-Rinse-Dry	RCA Bench #2, SRD	*omit HF dip on RCA clean*
4	Poly-Si Deposition	AME LPCVD	*Recipe:* Poly 630 *Time:* 30 min
5	RCA Clean, Spin-Rinse-Dry	RCA Bench #2, SRD	-
6	Coat O*i*R620-10 Photoresist	SSI Track	*Recipe*: coat *Target Thickness*: 1µm
7	Expose Poly-Si Pattern	Canon Stepper	*Jobfile:* F083WNAMEST_POLY *Exposure Dose:* 180 mJ/cm^2 *Focus:* 0.24µm *Mask:* X690.04 Poly
8	Develop	SSI Track	*Recipe:* develop
9	Etch Poly-Si Pattern	DryTek Quad	*Recipe:* EagleSi *Target Thickness:* 2000Å *Gas Flows:* 40 sccms SF_6, 40 sccms O_2 *Pressure:* 150 mTorr *Power:* 200W *Time:* 100 sec
10	Ash Photoresist	Branson Asher	*Recipe:* hardash
11	RCA Clean, Spin-Rinse-Dry	RCA Bench #2, SRD	*omit HF dip on RCA clean*
12	TEOS Deposition	AME P5000 - Chamber A	*Recipe*: TEOS 4000 *Target Thickness:* 4000Å
13	Coat O*i*R620-10 Photoresist	SSI Track	*Recipe:* coat *Target Thickness:* 1µm
14	Expose 1st Pass Contact Cut Pattern (Si Contacts)	Canon Stepper	*Jobfile:* F083WNAMEST_CC1 *Exposure Dose:* 280 mJ/cm2 *Focus:* 0.00µm *Mask:* X690.04 Active Con
15	Develop	SSI Track	*Recipe:* devcc
16	Thermal Cure	Hotplate	*Temperature:* between 175°C and 200°C *Time:* 90 sec
17	Coat O*i*R620-10 Photoresist	SSI Track	*Recipe:* coat *Target Thickness:* 1µm
18	Expose 2nd Pass Contact Cut Pattern (Poly-Si Contacts)	Canon Stepper	*Jobfile:* LF083WNAMEST_CC1 *Exposure Dose:* 260 mJ/cm2 *Focus:* 0.00µm *Mask:* X690.04 Poly Con
19	Develop	SSI Track	*Recipe:* devcc
20	Etch TEOS Pattern	-	-
	Oxide MERIE	AME P5000 - Chamber C	*Recipe:* C6 Oxide Etch *Time:* 240 sec
	10:1 BOE Dip (with sufactant)	Chemical Bench	*Time:* 35 sec
21	Ash Photoresist	Branson Asher	*Recipe:* hardash
22	RCA Clean, Spin-Rinse-Dry	RCA Bench #2, SRD	*omit HF dip on RCA clean*