Low Temperature Junction Formation in Silicon

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Abstract— The goal of this project was to examine the low temperature formation of silicon P-N junctions on SOI substrates. P+N and N+P diodes were fabricated with several different dopants at various implant doses. The effects of the silicon thickness were also examined. Existing theories of low temperature phosphorous solid-phase epitaxy (SPE) were verified through this study.

XXXII. INTRODUCTION

Currently in the display industry, the trend is towards higher integration of electronics required to run the display onto the TFT backplane. Currently the processes that are used in industry are low-temperature poly-silicon (LTPS) processes. Transistors fabricated using LTPS do not have the characteristics, mainly field-effect mobility, necessary to integrate the electronics that are necessary onto the backplane. By using a crystalline semiconductor bonded to a glass substrate electronic integration is possible.

Previous experiments have been performed at RIT regarding both low-temperature and high-temperature dopant activation, and junction integrity. This project is focused mainly on low-temperature processes because high-temperature dopant activation is already well characterized. Previous work on low temperature dopant activation has been performed at RIT [2,3].

The goal of this project is to provide some new data on dopant activation, and junction integrity that will in-turn yield better results for the low-temperature CMOS process run at RIT. This project continues on the previous work done at RIT while exploring new doping schemes and providing further insight of the electrical characteristics of the solid-state devices effected by these annealing methods at low temperature.

In this experiment thin-film lateral diodes were fabricated on SOI substrates using different doping and pre-amorphization schemes. Each substrate consisted of a silicon thickness that varied from 650 to 1500 angstroms. The various regions of silicon film thicknesses on the SOI substrates were created by using sacrificial thermal oxidation and a nitride diffusion barrier, a process similar to the local oxidation of silicon (LOCOS) isolation found in early CMOS technologies. The different treatment combinations were characterized by examining the sheet resistance via the Van der Pauw method and examining diodes ideality factors.

XXXIII. THEORY

In the thin-film transistor (TFT) industry there are low-temperature constraints during processing that are not an obstacle in normal high-temperature CMOS processing. The TFT process at RIT does not exceed temperatures of 600 °C because of constraints imposed by the glass substrate. Due to this constraint, achieving acceptable levels of dopant activation becomes difficult. There are many methods for increasing dopant activation efficiency. The technique that is commonly used is called solid phase epitaxy (SPE). SPE is when the substrate can re-grow by layer-by-layer epitaxial realignment beginning from an amorphous/crystalline interface [1]. For SPE to occur, an amorphous layer needs to be created. Phosphorous and arsenic implants can self-amorphize the silicon because of the size and mass of the ions. Boron, being a smaller ion, does not amorphize the silicon at the required dose. To circumvent this issue, a pre-amorphizing implant is used (co-implants). Once amorphized and implanted the wafers need to be subjected elevated temperatures for SPE to occur. SPE occurs between 500-600 °C. The rate at which the silicon re-crystallizes is proportional to the anneal temperature [1]. During the process of re-crystallization, most of the dopant atoms that are in the amorphous regions are incorporated into the silicon lattice as substitutional donor or acceptor sites. It is currently believed that the re-crystallization of an amorphous phosphorous layer occurs from a bottom seed crystal while boron may occur from either the top or bottom or both. If there is no seed crystal for epitaxial regrowth the film with stay amorphous. The assumption is that the thicker silicon thicknesses will show re-crystallization while the thinnest will not because of the lack of a seed crystal below the amorphous region caused by the implant. The process for making lateral diodes is similar to making diodes on bulk silicon. The major difference is that the lateral diodes are isolated on a silicon mesa. During SPE all of the damage is annealed out except the end of range implantation damage that is below the amorphous/crystalline interface [1]. For high-temperature processes these end-of-range defects at the junction are not an issue because they will form <311> clusters and dissolve at ~800 900 degrees Celsius, but for low temperature processes they need to be minimized.

XXXIV. PROCEDURE

The first step of this project is to fabricate silicon steps of varying thickness on four SOI wafers so that thin film annealing mechanisms involved in the re-crystallization of phosphorous, arsenic, and boron can be understood. Using a process similar to LOCOS isolation, a staircase of different

silicon thicknesses was fabricated. The thicknesses ranged from 60 nm to 150 nm. The process is shown in Table I on the following page.

Table I - Silicon Step Formation Process

Step	Process
1	Deposit 500A LTO Pad oxide (to preserve original silicon thickness)
2	"Densify" in dry O2 for 1 hr at 1000C
3	Deposit 1500A LPCVD Nitride
4	Oxidize nitride surface at 1000C
5	Level 1 Litho
6	Etch oxy-nitride in BOE
7	Strip Photoresist
8	Etch Nitride in Hot Phos.
9	Etch oxide in BOE
10	Furnace run 1 (67 minute soak)
11	Level 2 Litho
12	Etch Oxide and oxy-nitride in BOE
13	Strip photoresist
14	Etch Nitride in Hot Phos.
15	Etch thermal oxide in BOE
16	Furnace run 2 (191 Minute Soak)
17	Level 3 lithography
18	Etch oxide and oxy-nitride in BOE
19	Strip photoresist
20	Etch Nitride in Hot Phos.
21	Etch Thermal oxide in BOE
22	Furnace run 3 (65 min soak)
23	Etch oxide
24	Etch all nitride
25	Etch all oxide

Once fabricated, the SOI step wafers will be used to make lateral diodes. Three of the SOI wafers had have N+P diodes; one wafer with two different doses of phosphorous, and two wafers with two different doses of arsenic. The arsenic and phosphorous-based N+P diodes will be made at two different doses to compare both activation and junction integrity. Doses of 1×10^{15} cm^{-2} and 2×10^{15} cm^{-2} will be used. Arsenic doses greater than 2×10^{15} cm^{-2} were not be used because previous work [2] shows that arsenic activation begins to decrease as the dose gets higher due to clustering. For the fourth wafer, P+N lateral diodes will be fabricated. Since N-type SOI wafers are not readily available a counter-doped P-type SOI wafer will be used. The implant to counter-dope the wafer will be 2×10^{11} cm^{-2} phosphorous implant at 100 KeV. The fourth wafer will also explore different pre-amorphization schemes with Boron. The wafer was masked in two halves, one which received a fluorine pre-amorphization and one having silicon pre-amorphization. All of the wafers were be annealed at 600 °C for 1 hour. All treatment combinations are summarized in Table II.

Table II - Treatment Combinations

TC	Dopant	Wafer #	Dose
1	Phosphorous	1	1×10^{15} cm^{-2}
2	Phosphorous	1	2×10^{15} cm^{-2}
3	Arsenic	2	1×10^{15} cm^{-2}
4	Arsenic	3	2×10^{15} cm^{-2}
5	Boron w/Si	4	2×10^{15} cm^{-2}
6	Boron w/F^{+}	4	2×10^{15} cm^{-2}

Simulations for the counter-doping and step formation are shown in Figs. 1-3 on the following pages. These simulations also compare a 120 minute high temperature anneal after counter-doping implant versus no anneal. These simulations show that a separate high-temperature anneal is not needed to activate the phosphorous because the step-making process contains thermal energy to provide full activation and a evenly diffused dopant concentration profile throughout the entire film thickness. The simulation also shows that when the silicon is thicker the net dopant concentration is lower. This result is expected because diffusivity of phosphorous into oxide is low; the phosphorous just piles up at the Si/SiO_2 interface. The difference in body doping between the thickest and thinnest silicon thicknesses is ~8×10^{15} cm^{-3} which will cause a difference in the series resistance of the diodes. Since it is known that the series resistance will change due to the dopant segregation, it can be accounted for in the final analysis.

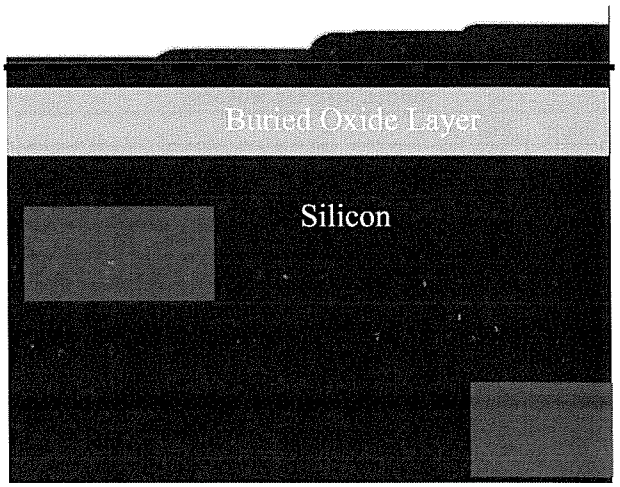

Figure 1: Silicon Step Process Simulation (Dashed Line Shows Cutline for Figures 2 and 3)

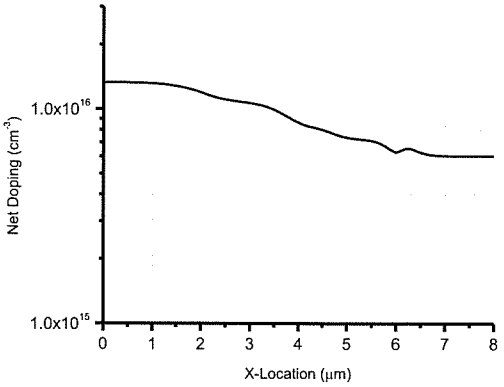

Figure 2: Final simulated dopant profile for counter-doped silicon steps

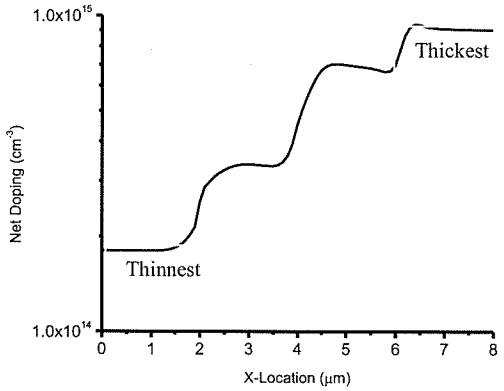

Figure 3: Final simulated dopant profile for non counter-doped silicon steps

From the characterization of the diodes it is possible to determine if the N+ implanted regions have fully re-crystallized or not. The process for making the lateral diodes is shown in Table III. A process cross-section is shown in Fig. 4.

Table III – Process Flow for making lateral diodes on SOI wafers

Step	Process
1	RCA Clean
2	Deposit Screen Oxide (For counter doped wafer only) 1000Å
3	Counter Doping implant (For counter doped wafer only) P^{31} 2×10^{11} cm^{-2} 100 KeV
4	Strip Screen Oxide (For counter doped wafer only) in BOE
5	Fabricate Silicon Steps (See Table II)
6	Litho 1 Mesa Definition
7	Etch Mesa
8	Strip Resist
9	Deposit Screen Oxide (500Å)
10	Litho 2
11	P+ or N+ contact implant - B^{11} 4×10^{15} cm^{-2} @ 17 KeV - P^{31} 4×10^{15} cm^{-2} @ 55 KeV
12	Strip Resist
13	High Temp Anneal
14	Litho 3
15	P+ or N+ Junction Implant - B^{11} @ 17 KeV - P^{31} @ 55 KeV - As @ 120 KeV
16	Strip Resist
17	Low Temp Anneal (600C 2 hr)
18	Deposit 4000 Angstroms of Oxide (LTO)
19	Litho 4
20	Etch Oxide
21	Strip Resist
22	Al Deposition
23	Litho 5
24	Metal Etch
25	Strip Resist
26	Sinter (425°C 15 Min)

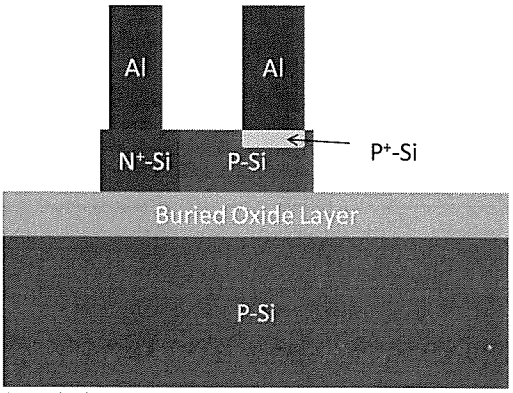

Figure 4: Lateral Diode Cross Section

XXXV. RESULTS AND ANALYSIS

SOI Step Fabrication

The steps were fabricated on each of the SOI wafers using the process shown in Table III. Once fabricated the silicon thickness was measured on the Prometrix Spectramap. The resulting average thicknesses for the four silicon steps were 65nm, 85nm, 110nm, and 1450nm. A recipe was written on the Spectramap for a 1264-point measurement. A recipe with so many points provides a good visual representation of the sample. Fig. 5 shows the graphical representation of the data collected by the Spectramap.

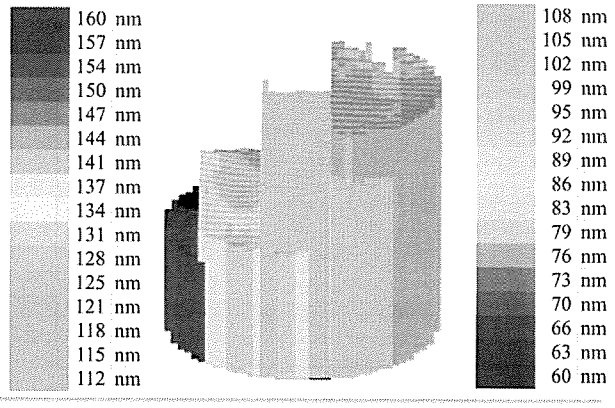

Figure 5: 1264 point silicon thickness map

Processing Notes

All four wafers made it through the process with minimal issues. All lithography was done on the GCA 6700 stepper. After every level of lithography, the alignment was verified to be with in 2 microns of nominal. For separating half wafers for certain treatment combinations the dropout die feature on the GCA stepper was utilized. During processing there were only two notable issues that could influence yield. These issues were:

- The second phosphorous implant was done at 110KeV instead of 55KeV
- The 2×10^{15} arsenic implant (done by CORE systems) caused the resist to burn.

The phosphorous wafer misprocessing was simulated in SRIM and determined not to be a major issue. These simulations are shown in Figs. 6 and 7. The only issues that it may cause are fully amorphous junctions in the thinnest part of the wafer. Through characterization of the VDP structures, it can be determined whether or not the thinnest silicon has been fully amorphized.

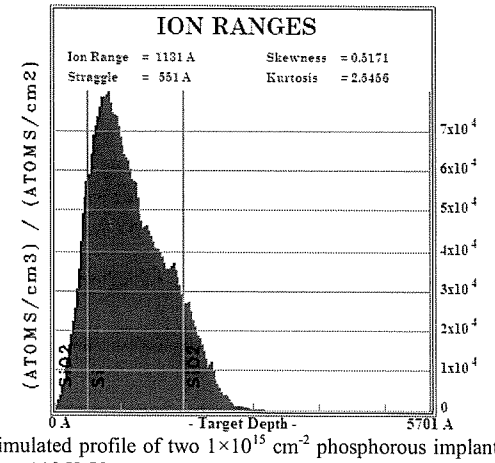

Figure 6: Simulated profile of two 1×10^{15} cm^{-2} phosphorous implants; one at 55 KeV one at 110 KeV

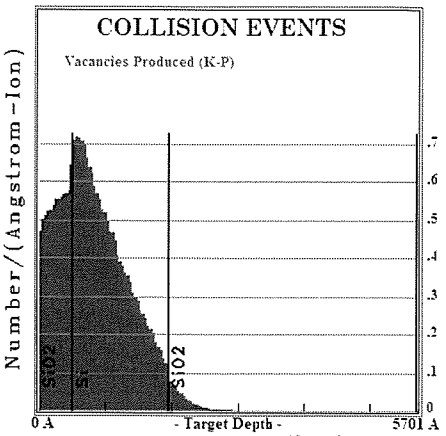

Figure 7: Simulated damage profile of two 1×10^{15} cm^{-2} phosphorous implants; one at 55 KeV one at 110 KeV

There is nothing that can be done to change what happened to wafer 3 (2×10^{15} As). Test results will show whether the implant was aligned or not.

VDP Testing

Figs. 8 and 9 show the results from testing the N^+ VDP structures on wafers 1-3.

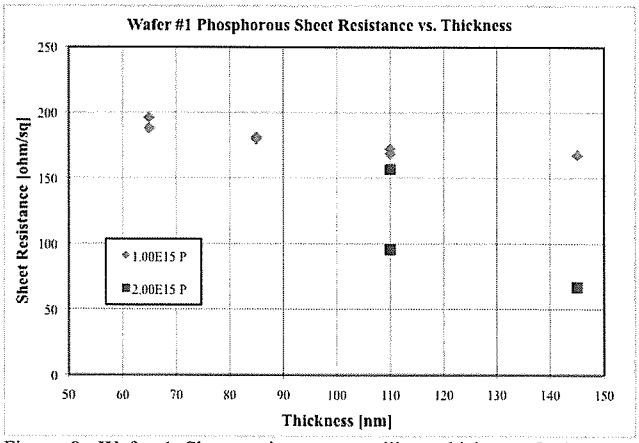

Figure 8: Wafer 1 Sheet resistance vs. silicon thickness 55 KeV 1×10^{15} phosphorous followed by 110 KeV 1×10^{15} phosphorous

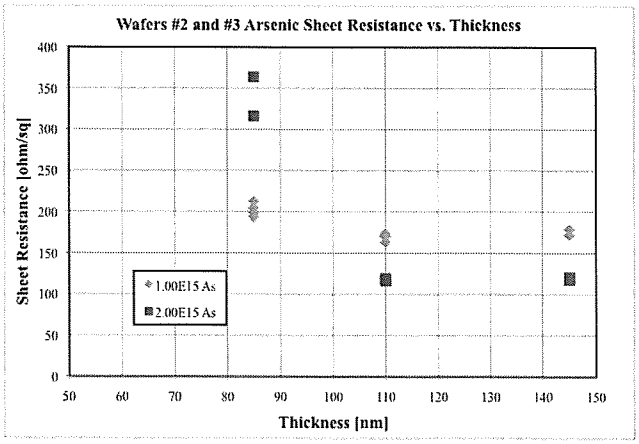

Figure 9: Wafers 2 and 3 Sheet resistance vs. silicon thickness 120 KeV Arsenic

Fig. 8 shows the sheet resistance vs. silicon thickness for both doses of phosphorous on wafer 1. There are no data points below 110nm for the 2×10^{15} cm^{-2} dose of phosphorous because they gave open circuit measurements. The reason for the open circuits below 110nm is that the implant was done at two different energies so the damage profile is a lot deeper throughout the silicon. The assumption is that the damage caused a fully amorphous layer of silicon so that no solid phase epitaxial re-growth was able to occur. For both doses of phosphorous once there was a sufficient seed crystal for SPE to occur, there was little change in sheet resistance with respect to the seed crystal thickness. This shows that for phosphorous the epitaxial re-growth is a "bottom-up" process that is not dependant on seed crystal thickness; once there is a seed crystal there will be epitaxial re-growth.

Fig. 9 shows the VDP data for arsenic wafers 2 and 3. The arsenic behaves similarly to the phosphorous. The damage from the implant in the 65nm thick step was enough to fully amorphize the region for both doses. At the 85nm thickness some re-crystallization does occur, but the sheet resistance for both cases is still high. At thicknesses 110nm and greater, the damage in the lattice has annealed out and the arsenic is active. The 2×10^{15} cm^{-2} dose of arsenic does show a lower sheet resistance than the 1×10^{15} cm^{-2}.

In the case of P^+ VDP testing all of the VDP's on all of the wafers show open circuit behavior. This suggests that either boron did not activate (even at high temperatures) or there is an issue with the contacts.

Lateral Diode Testing

Figs. 10-12 show the results from diode testing. All of the plots show the ideality factor in the diffusion current dominated region of the lateral diode vs. the thickness of the silicon.

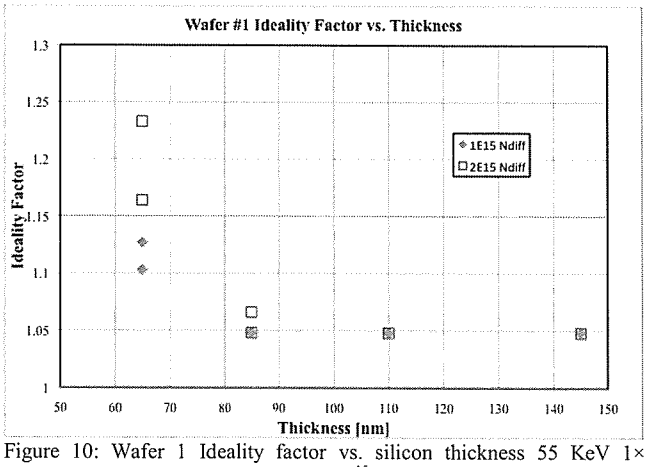

Figure 10: Wafer 1 Ideality factor vs. silicon thickness 55 KeV 1×10^{15} phosphorous followed by 110 KeV 1×10^{15} phosphorous

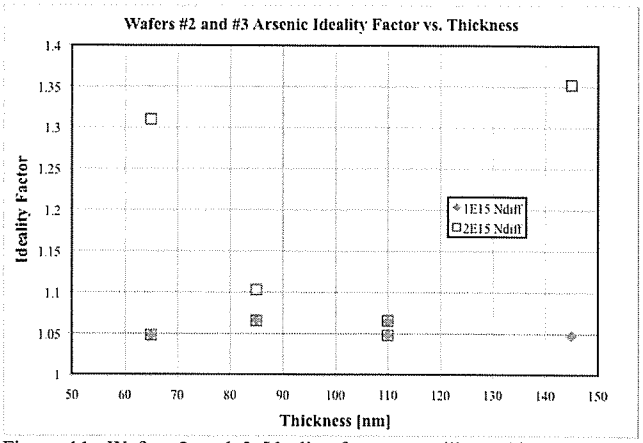

Figure 11: Wafers 2 and 3 Ideality factor vs. silicon thickness 120 KeV Arsenic

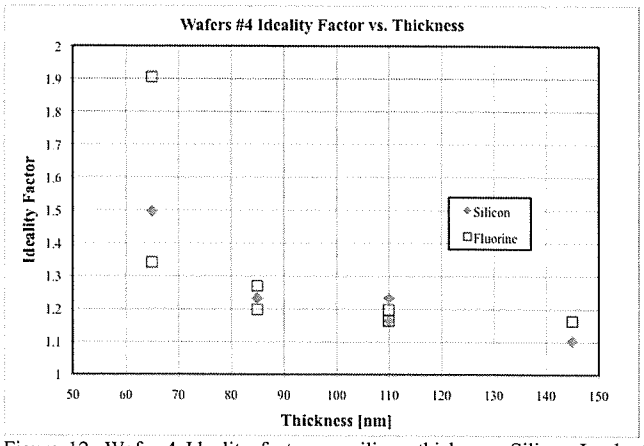

Figure 12: Wafer 4 Ideality factor vs. silicon thickness. Silicon Implant 55 KeV 1×10^{15} cm^{-2}, Fluorine Implant 33 KeV 3×10^{15} cm^{-2}, Boron Implant 17 KeV 2×10^{15} cm^{-2}

Fig. 10 on the previous page shows the ideality factor for the phosphorous-doped diodes on wafer 1. At a thickness of 65nm, the ideality factor for both doses of phosphorous is greater than 1.1. The reason for this could be the fact that the dopant is not active in the silicon thus there are more sites for carrier recombination and generation. Another theory is that the recombination generation sites are at the silicon oxide interfaces and the thinner the silicon the higher the recombination-generation current. As the silicon thickness increases, the junction becomes more ideal. With this wafer, once the silicon has been epitaxially re-grown the ideality factor of the diodes become approximately 1.05. This is consistent with previous values for thin-film lateral diodes [3]. Again the junction ideality factor is not dependant on the seed crystal thickness; once the damage is annealed the junction behaves the same.

Fig. 11 shows the junction ideality factor for the two treatment combinations with arsenic used as doping. Although steady state activation was not achieved for the thinnest silicon, the 1×10^{15} cm^{-2} dose of arsenic showed an ideality factor consistent with the other silicon thicknesses with the same dose. The 2×10^{15} cm^{-2} dose, on the other hand, showed more variability in the ideality factor. The ideality factor at both 65 nm and 145 nm showed a high value greater

than 1.3. The issues with the resist burning on this implant could explain the variability.

Fig. 12 shows the data for the boron junction ideality factor. In this case the dose of boron is constant (2×10^{15} cm^{-2}), but the pre-amorphization implant is different. With the boron implants the ideality factor steadily decreases with silicon thickness. Even though the ideality factor steadily decreases with silicon thickness, it does not reach the near ideal levels that the N+ doped diodes reach. These results suggest an issue with the low-temperature boron activation. This boron activation issue is supported in previous data [2]. The boron activation at low temperature is not nearly as good as phosphorous activation at low temperature. The silicon pre-amorphization performs more consistently than the fluorine pre-amorphization. This effect is expected because fluorine tends to cluster with boron and cause defects while silicon implants just cause excess damage and interstitials.

All wafers were all tested to try and establish a correlation of junction integrity to breakdown voltage. There was no correlation that was found for any wafers. The reverse bias behavior of these diodes is not ideal. All diodes on every wafer show high leakage and a two-step breakdown behavior.

The P+ VDP Issue

The current theory for the reason that the P+ VDP structures do not work is that the P+ contact cut did not fully etch. The reason that the diodes work is that there are 12 contacts for each end of the diode and the probability that one will work is high since there was a 200% over etch. The VDP structures do not work because each of the 4 ends of the structure has two contacts so four of the eight total contacts must work for the VDP to measure the sheet resistance. Given more time, a contact cut and metal rework could be done to further examine the activation.

XXXVI. CONCLUSION

This project examined how a P-N junction forms in silicon at low temperatures. Silicon steps were fabricated on four SOI wafers. On the different thicknesses of silicon, lateral thin-film diodes were fabricated utilizing different dopants and implant doses. Results validated the existing theory that phosphorous SPE occurs from the bottom of the amorphous layer. The phosphorous junction ideality had no dependence on seed crystal thickness. Results also showed that silicon preamorphization created a higher quality junction than fluorine preamorphization. Arsenic was proved to form relatively ideal junctions for a dose of 1×10^{15} cm^{-2}, but for a dose of 2×10^{15} cm^{-2} the junction did not behave as well. Two factors that could influence the behavior of the junction are arsenic clustering and the fact that the implant burned the resist. This project provided more information on SPE and junction formation at low temperature.

XXXVII. REFERENCES

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[2] E. M. Woodard, "Low Temperature Dopant Activation for Applications in Thin Film Silicon Devices," M.S. thesis, MS&E., RIT, Rochester, NY, 2006.

[3] R. G. Manley and K. D. Hirschman, private communication, October, 2008.