

A New 6" Metal Gate PMOS Process

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Abstract—This paper presents the development, fabrication, and testing of a new 6" Metal Gate PMOS process. The new 6-inch Metal Gate PMOS process is an upgrade from the 4-inch Metal Gate PMOS process, which is the process currently used at RIT for the IC Technology course as well as the Short Course. The upgrades include the use of 6-inch wafers from 4-inch wafers, four levels per mask lithography instead of one level per mask lithography, ion implant instead of spin on dopant, and the number of control wafers was reduced from five wafers to three wafers. Development and fabrication of the 6-inch Metal Gate PMOS process are discussed, as well as the testing of the devices on the chip. The overall process was determined to be successful, yielding working devices, and is suitable to be used in the future with the IC Technology course and the Short Course.

Index Terms—Metal Gate PMOS, RIT

I. INTRODUCTION

As technology moves forward, devices are becoming smaller and the wafers upon which they are being created are becoming larger. This suggests that there is a need for the option of processing on 6-inch wafers in addition to 4-inch wafers. The RIT Metal Gate PMOS process has an overlay design rule of 10 μm and is easily within the capabilities of the SMFL toolset. The process almost always produces working components. Using prior course knowledge, alternative processing methods were able to be determined for the substitution of steps such as the spin-on p-type dopant to ion implant as well as creating jobs and utilizing masks with four lithography layers per mask on the Canon stepper.

II. PROCESS DESIGN

A. Process Details

The starting material is an n-type wafer, resistivity of 5-20 Ohm-cm, with a $\langle 100 \rangle$ orientation. The specific process details include four design layers with four corresponding lithography levels: the masking oxide, diffusion, contact cut, and metal. With regards to the lithography levels, there is a 10 μm overlay tolerance. The p+ source and drain regions are ion implanted. There are a variety of components within the Metal Gate PMOS mask, including digital logic (NAND gates, multiplexors, NOR gates), transistors, Van der Pauw structures, CBKR's, and integrated circuits. Results include plots that confirm the correct operation of each test structure; IV curves for resistors, the family of curves for transistors, and digital output waveforms for logic. A cross-section is shown in Figure 1.

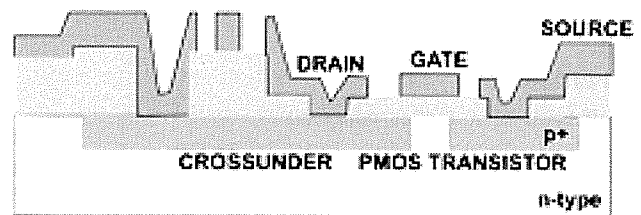


Fig. 1. Cross-sectional view of a PMOS transistor. [1]

B. 4-Level Per Mask Lithography

A key component in designing the process was to utilize four-level per mask lithography. This method puts four lithography levels on one mask, shown in Figure 2. This specific type of mask is able to be used with the Canon Stepper, which is an i-line, 5X reduction stepper capable of processing 6-inch wafers. Using the set-up of four layers per mask saves money, time, and inventory. However, the downfall may be that the chip size is 10 mm by 10 mm from 20 mm by 20 mm. [2]

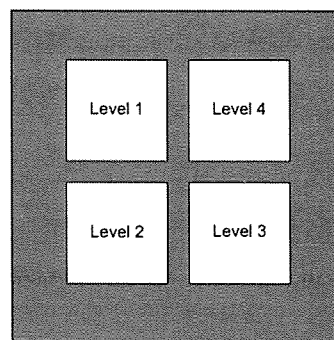


Fig. 2. Mask with four lithography levels

C. Ion Implant

Another key component in designing the process was to switch from using the spin on dopant process to ion implant in the source and drain region. Ion implanting reduces processing time since the spin on dopant process requires additional processing steps, such as the application of the spin on dopant and a pre-deposition step, which is an additional furnace step.

A special consideration to take into account with ion implant is that it produces a shallower junction depth. A too shallower junction depth would pose problems with the subsequent field oxide growth since silicon dioxide growth not only consumes silicon (approximately 44% of the oxide thickness), but also depletes boron from the silicon at the Si/SiO₂ interface. [3]

Simulations were used to model the ion implant and subsequent field oxide growth steps for various dose and power combinations. The resulting parameters used were to use a boron dose of 2×10^{15} ions/cm², at an energy of 60 KeV, shown in Figure 3. This results in a 6.5 minute per wafer implant on the Varian 350D implanter.

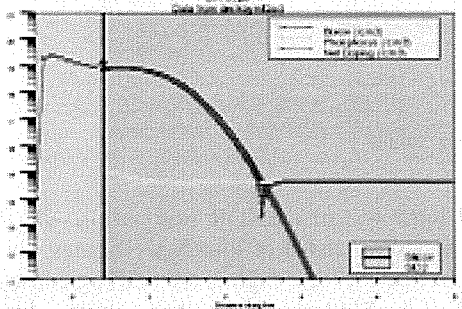


Fig. 3. Ion implant simulation

With regards to an implant mask thickness, the existing masking oxide (5000 Å) would be sufficient. Additionally, the photoresist used to pattern the source and drain areas could be etched off before the implant, which could allow for a higher power to be used if necessary.

D. Control Wafers

Reducing the number of control wafers is beneficial due to the fact that control steps are processed on device wafers and are disposed of after they have been used. This is another step that saves money. The previous 4-inch Metal Gate PMOS process utilized five control wafers and this number is reduced to three with the 6-inch Metal Gate PMOS process. Table 1 shows what each wafer was used for.

TABLE 1
CONTROL WAFER USES

	4-inch Process	6-inch Process
C1	-Masking oxide etch rate -Minimum masking oxide thickness	Top half -Masking oxide etch rate -Minimum masking oxide thickness Bottom half -Junction depth after implant -Sheet resistance after implant
C2	-Junction depth after pre-deposit -Sheet resistance after pre-deposit	-Junction depth after field oxide -Sheet resistance after field oxide
C3	-Junction depth after field oxide -Sheet resistance after field oxide	-Junction depth after gate oxide -Sheet resistance after gate oxide
C4	-Junction depth after gate oxide -Sheet resistance after gate oxide	
C5	-Determine fast and slow etch rates	

To begin with, C5 was not needed as it was used to determine the etch rate of spin on dopant on oxide. Also determined was that C1 could be split into a top and bottom half. The top half was used to perform the step etch to determine the masking oxide etch rate and the subsequent minimum masking oxide needed. The bottom half could be

used to determine the junction depth and sheet resistance after the implant, which is what C2 was used for previously.

III. FAILURE ANALYSIS

A. Incomplete Contact Cut Etch

After the first run was complete, testing was performed to determine whether or not the devices worked, deeming the process successful. This initial testing, shown in Figure 4, proved there was an incomplete contact cut etch. This resulted in no contact between the metal and the p+ regions due to the remaining field oxide.

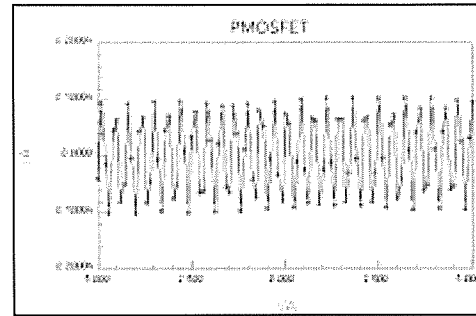


Fig. 4. Incomplete contact cut etch results

In order to fix this, the wafers were reworked by removing the metal and redoing the contact cut lithography, etch and metal steps.

B. Oxide Degradation

Although the rework was successful in creating operating devices, not all regions of the wafer worked successfully, nor did transistors smaller than a certain length and width in all of the working regions. Through electrical results and microscope inspection, it was determined that there was an issue with the gate oxide, more specifically the degradation of the gate oxide resulting from the rework process. This factor affected the operation of the resistors post-rework and the operation of the various devices. Due to this, rework should be avoided and a rework process compatible with the Metal Gate PMOS process should be developed.



Fig. 5. Image of oxide degradation

IV. VERIFICATION TESTING

A. PMOSFET

This test consisted of creating a family of curves for various PMOSFET transistor sizes. The goal of this testing was the main determinant as to whether or not the process was successful. Figure 6 shows the actual transistor used for testing. Figure 7 shows the family of curves using the previous 4-inch process while Figure 8 shows the family of curves using the new 6-inch process for comparison.

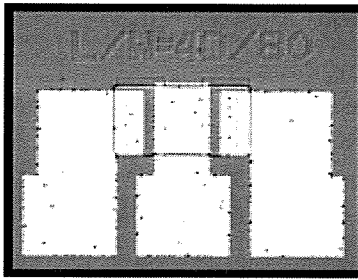


Fig. 6. PMOSFET L=40μm W=80μm

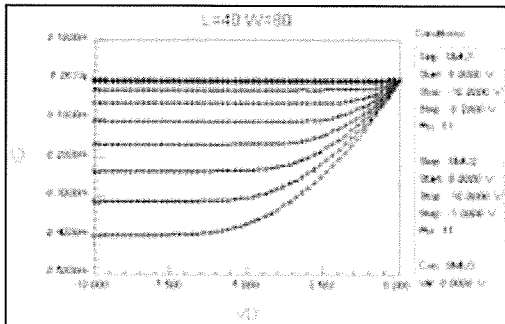


Fig. 7. Family of curves for 4'' Metal Gate PMOS process with spin on dopant

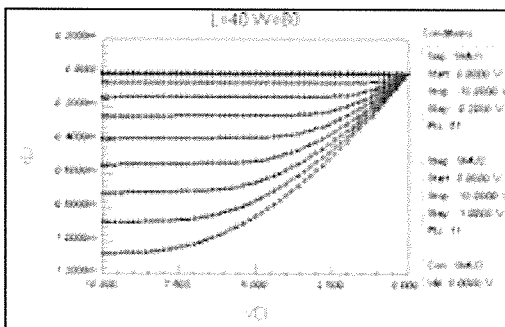


Fig. 8. Family of curves for 6'' Metal Gate PMOS process with ion implant

B. Inverter

The next test involved an inverter, shown in Figure 9. This inverter was designed using two PMOSFETs. The designed gain for this specific inverter was 2 V/V, but the testing showed it was approximately 3.56 V/V, shown in Figure 10. The difference may have been due to the oxide degradation issue or the design.

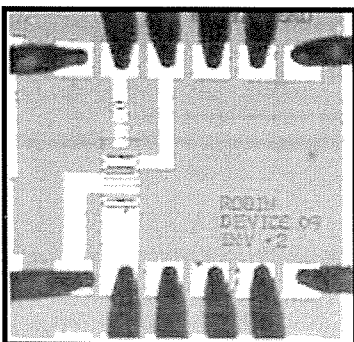


Fig. 9. Inverter

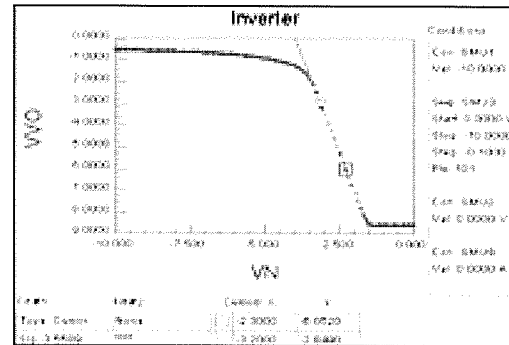


Fig. 10. Inverter test results

B. XOR

The digital logic test of an XOR was performed. The specific XOR tested consisted of four NAND gates, shown in Figure 11. In PMOS, logic high is a 0 and logic low is a 1. The output of an XOR should be “low – high – high – low”, but the test resulted in an output of “low – high – high – zero”, where the zero may be taken to be high or low, this is shown in Figure 12. The possible errors may include the XOR design, a design using NOR gates may be more successful, or once again the oxide degradation issue.

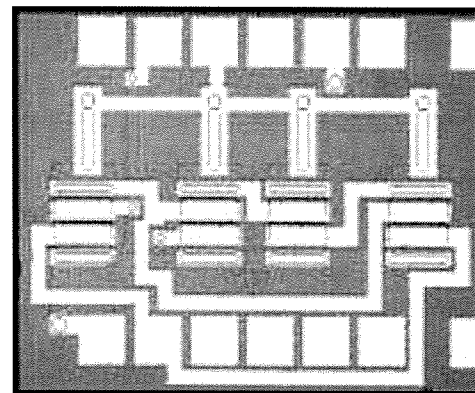


Fig. 11. XOR

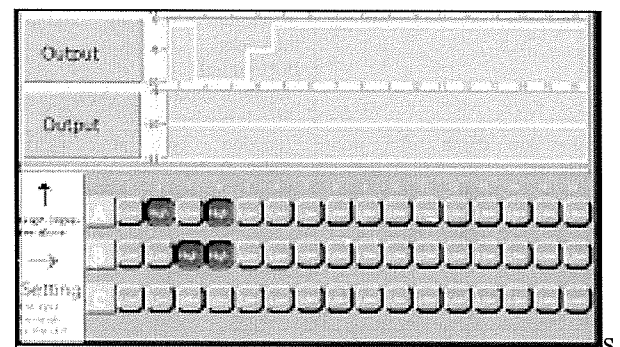


Fig. 12. XOR Test Results

B. Resistor

A resistor, shown in Figure 13, was also tested yielding interesting results. When no substrate bias was applied, as should be the normal testing, the resistor behaves characteristically as a diode, shown in Figure 14. If a -10 Volt bias is applied, the resistor behaves as it should; very linear with an intercept through the origin, shown in Figure 15.

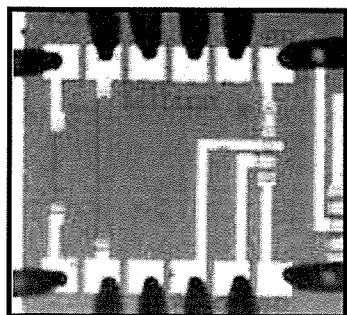


Fig. 13. Resistor

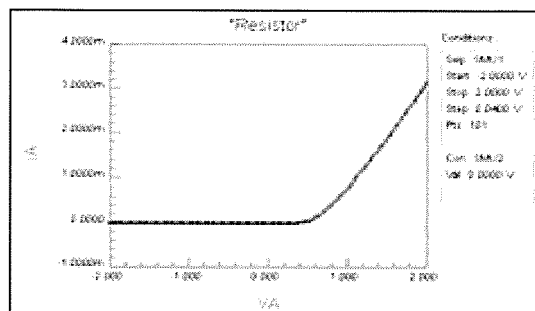


Fig. 14. Resistor behaving characteristically as a diode.

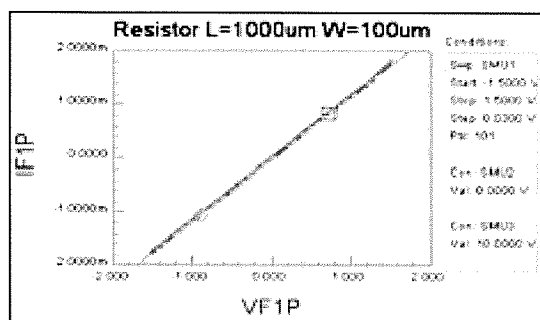


Fig. 15. Resistor results when using a -10 V bias

V. CONCLUSION

A new 6" Metal Gate PMOS process has been developed that features ion implanted p-type regions, plasma etch, 4-level per mask lithography using the Canon stepper and a new sequence for control wafers. The process was shown to yield working devices and students taking the IC Technology or the Short Course will use this process in the future.

VI. REFERENCES

- [1] Fuller, Lynn. PMOS Process Details. 2003.
- [2] Fuller, Lynn. Canon Four Levels Per Mask Plate Stepper Jobs. 2009.
- [3] Colinge, Jean-Pierre & Cynthia A. Colinge. Physics Of Semiconductor Devices. Kluwer Academic Publishers. 2007

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