# Fabrication and Characterization of Solar Cells on p-type Si and p/p+ Epitaxial Si

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***Abstract*—Solar cells were fabricated at the Semiconductor and Microsystems Fabrication Laboratory at Rochester Institute of Technology on two different substrates. Standard polished p-type Si and a substrate consisting of a 15 μm p-type epitaxial Si built on a p+ substrate Si wafer. In addition, on the epitaxial Si both diffusion and ion implantation were used for doping. Using both epitaxial Si and ion implantation created solar cells that outperformed the diffusion and p-type Si solar cells.**

***Index Terms*—solar cells, epitaxial silicon**

## XXVIII. Introduction

THE Microelectronic Engineering Department at RIT offers an elective course in photovoltaics, as well as outreach programs for K-12 teachers and students to gain exposure to semiconductor processing through the fabrication of a solar cell. In an attempt to improve cell performance, devices were built on p-type Si substrates and p/p+ epitaxial Si which were generously donated by Eastman Kodak Company. The p-type Si substrates had a resistivity of 25 Ω-cm while the p/p+ epitaxial wafers consisted of a 15 μm epitaxial layer with a resistivity of 5-6 Ω-cm on top of a p+ substrate with a resistivity of 0.01-0.02 Ω-cm. The solar cells fabricated on the epitaxial wafers should perform better due to a back surface field (BSF) and reduced diffusion distances. For the p-type Si, spin-on dopant was used. For the epitaxial wafers, solar cells were built with either spin-on dopant or ion implantation.

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## XXIX. Experimental Procedure

### A. Standard Process Flow

The process flow for the solar cells is fairly simple as the primary goal is to introduce semiconductor processing to either teachers or students. In addition, a large solar cell is fabricated so that it can be seen without magnification. First, a field oxide of approximately 5000 Å is grown on the wafers. Using contact lithography, a large circular area is etched to provide an active region. Following a clean step the active area is then doped using spin-on dopant and it is diffused at 950°C for 30 minutes in wet $O_2$. This oxide is etched and an anti-reflective oxide is grown at 950°C for 132 minutes in dry $O_2$ to obtain an oxide thickness of 950 Å. A coating of lift-off photoresist is spun on the wafer followed by a coat of photoactive photoresist. Contact lithography is performed in order to pattern the aluminum. Aluminum is sputtered for 2500 seconds at 1000 W. The lift-off step is then performed to remove the aluminum. The wafers then are sputtered on the backside to the same conditions to form the backside contact. Lastly, the wafers undergo a sinter process at 450°C for 18 minutes in an $N_2/H_2$ forming gas.

### B. Ion Implantation

On some of the epitaxial wafers, an ion implantation step was done instead of spin-on doping. This step occurred after the wet oxide growth. An implant was performed at a dose of $1x10^{16}$ atoms/cm$^2$ at an energy of 60keV. The goal of this step was to provide better uniformity of dopant across the wafer as well as create a shallower junction that would occur as the drive

in occurred while the anti-reflective oxide was grown.

## XXX. Results

### A. Overall Results

Figs. 1 and 2 show a completed p-type Si and p/p+ epitaxial Si wafer respectively. In Fig. 2, leftover aluminum from the lift-off process can be seen. This was due to an error in the lithography process where not enough lift-off resist was able to be coated on the larger 6-inch wafers.

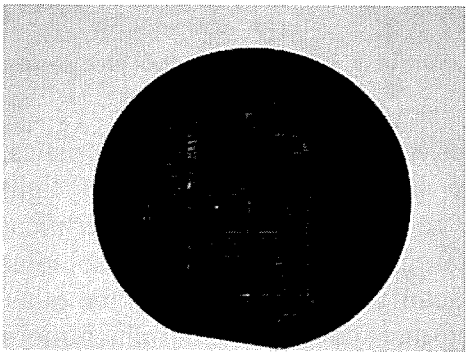

Fig. 1 Completed 4-inch p-type wafer. This wafer underwent the standard process flow.

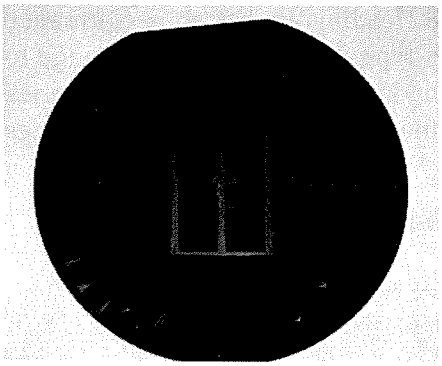

Fig. 2 Completed 6-inch p/p+ epitaxial wafer. Large amounts of aluminum are visible on the outside protective oxide. This was caused by not enough lift-off resist being deposited on the wafer. The samples did not experience any adverse effects due to this. This wafer underwent ion implantation.

### B. P-type Si Solar Cells

The solar cells fabricated on the p-type Si performed similarly to devices previously fabricated using the same process [1]. Fig. 3 shows the I-V characteristic of the solar cells. The top curve represents operation in no light conditions, the middle curve represents operation in room fluorescent broadband light conditions and the bottom curve represents operation in room light as well as an additional Xe light source. The tests were performed in this was as they mimic the testing done for the outreach program.

TABLE I
P-TYPE SI SOLAR CELL PERFORMANCE

| Quantity | Value |
|---|---|
| $V_{OC}$ | 0.60 V |
| $I_{SC}$ | 3.0 mA |
| $P_{Max}$ | 0.60 mW |
| $FF$ | 0.33 |
| $P_{Max}/Area$ | 26.1 mW/m$^2$ |

Area of the device is 0.023 m$^2$.

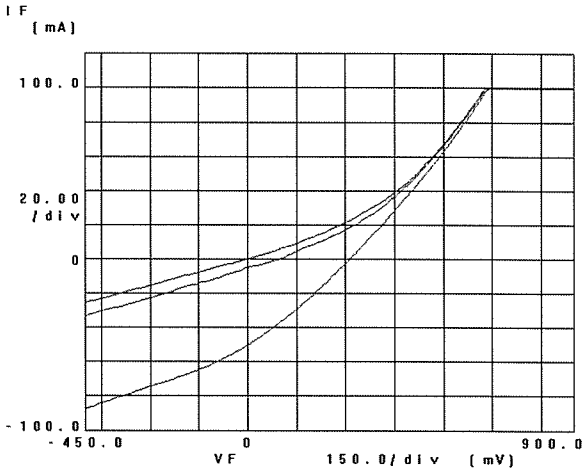


Fig. 3 I-V characteristic of p-type Si solar cells.

These devices exhibited a high amount of series resistance. In addition, there is only a 4% difference in the current flowing in the device from complete dark conditions to maximum light conditions. Table 1 shows the relevant data obtained from testing including fill factor (*FF*).

### C. P/P+ Epitaxial Si, Standard Process Solar Cells

These devices performed better than those processed on p-type Si. However, there still was a large amount of series resistance as seen in Fig. 4. This cause is unknown.

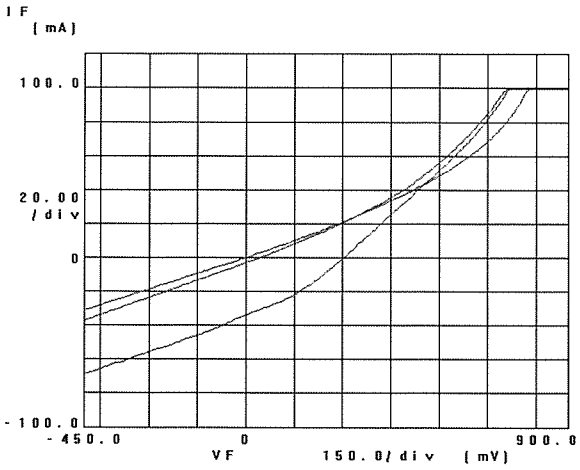


Fig. 4 I-V characteristic for p/p+ epitaxial Si solar cells using spin-on dopant.

There is a 7% difference between the dark and bright light current in these devices, a large improvement over the standard p-type Si. Table 2 shows data extracted from these devices.

TABLE 3
P/P+ EPITAXIAL SI SOLAR CELL PERFORMANCE

| Quantity | Value |
|---|---|
| $V_{OC}$ | 0.50 V |
| $I_{SC}$ | 4.6 mA |
| $P_{Max}$ | 1.16 mW |
| $FF$ | 0.50 |
| $P_{Max}/Area$ | 50.4 mW/m$^2$ |

Area of the device is 0.023 m$^2$.

### *D. P/P+ Epitaxial Si, Implant Process Solar Cells*

The solar cells fabricated on the p/p+ Epitaxial Si using ion implantation performed the best of the three splits of wafers. There was very little series resistance and the solar cells more closely resemble diodes. Fig. 5 shows the I-V characteristic of these devices.

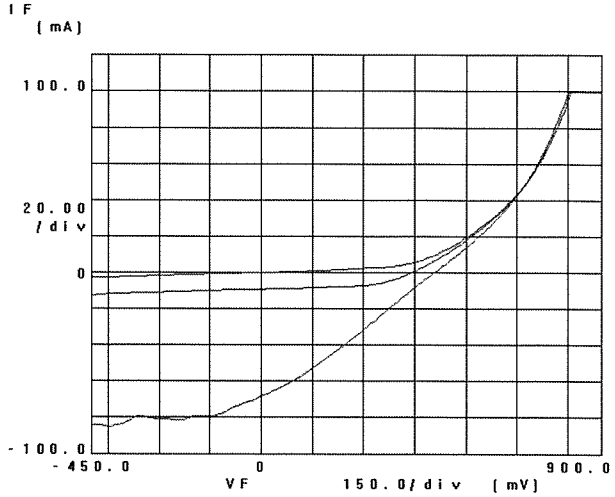


Fig. 5 I-V characteristic of p/p+ eptaxial Si implant process solar cells.

These devices exhibit very good characteristics. The difference between dark and bright light current is 8%. Table 3 shows all of the pertinent data obtained from the devices. For these solar cells, the fill factor is much higher than the other devices proving that it is functioning much more efficiently.

## XXXI. CONCLUSIONS AND FUTURE WORK

The completed solar cells exhibited response to light. It appears that a BSF was created in the epitaxial samples leading to better performance versus standard p-type Si. In addition, a change to ion implantation shows a decrease in series resistance in the solar cells. The devices fabricated on the p/p+ epitaxial Si are the first such solar cells fabricated on that kind of substrate at RIT.

TABLE 2
P/P+ EPITAXIAL SI SOLAR CELL PERFORMANCE

| Quantity | Value |
|---|---|
| $V_{OC}$ | 0.57V |
| $I_{SC}$ | 3.4 mA |
| $P_{Max}$ | 0.76 mW |
| $FF$ | 0.39 |
| $P_{Max}/Area$ | 33.0 mW/m$^2$ |

Area of the device is 0.023 m$^2$.

More work should be done to optimize the junction depth as well as metal thickness. These were not optimized in this process. Other work should consider using a smaller cell size to minimize series resistance effects and to use a

subtractive aluminum etch as opposed to lift-off processing to ensure no extraneous aluminum is left on the wafer.

## ACKNOWLEDGMENT

The author would like to thank Eastman Kodak Co., especially M. Miller, B. Sopko and D. J. Seidler for the donation of the epitaxial wafers. In addition, the author would like to thank Dr. M. A. Jackson, his principle adviser as well as Dr. L. F. Fuller, E. Lewis and S. O'Brien for their help.

## REFERENCES

[5] E. Lewis, M. A. Jackson, Prior Work

**Nathaniel Kane** (Student M'06) resides in Webster, N.Y. and will complete the engineering portion of his B.S. degree in Microelectronic Engineering and Economics from Rochester Institute of Technology in May 2009.

He worked at Irondequoit High School from 12/07-5/08 as part of a service learning cooperative education experience. While there, he helped develop several labs for physics students that utilize semiconductor devices as well as critical thinking skills. He also worked for 9 months at the Image Sensor Solutions department of Eastman Kodak Co. as a Silicon Characterization Engineer Co-op. While there, he prepared wafers for processing and characterized completed image sensors for metal contamination. He manually analyzed dark current spectroscopy results for over 4000 sensors and created a database to store the results.