Mask-less Crystalline Silicon Solar Cell (May 2009)

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Abstract—**A mask-less crystalline silicon solar cell was made by using a surface texturing technique coupled with an oblique aluminum evaporation. To achieve this, trenches with a steep sidewall are mechanically grooved into the bulk silicon using the KS 775 Wafer Saw. More importantly, metal evaporation with the CVC evaporator at angles near parallel to the wafer surface allows deposition to occur along the side of the trenches creating the self-aligning front metal contacts. Of the four solar cells that made it through the processing, only one solar cell showed diode like I-V characteristics. The dark conditions shows a diode I-V where current doesn't flow with a negative applied voltage and in the forward applied voltage, there is a turn on voltage around 0.6V, typical of a silicon diode. This is followed by an exponential gain in current. The n value of the diode is under dark conditions is 1.7. Under illuminated conditions, the I-V curve shows a dramatic negative current for voltages below 0.25V. This isn't the I-V curve of a solar cell but it does show that this device is light sensitive. The other three solar cells made are resistors with resistances of 4 Ω, 2 Ω and 19.2 Ω for wafers 3, 4 and 5 respectively. The shorts on the solar cells are due to a non-uniformly coated N-250 spin on glass (SOG) for the n+ layer on the p type wafer. Air pockets remained in the trenches and kept certain spots on the wafer surface to remain p. When the Al front contacts and bus paste are applied to the solar cells, it creates the p-n junction shorts. This was confirmed by breaking wafer 3 into smaller pieces where one of the pieces had a uniform n+ layer that showed I-V curves of a diode.**

Index Terms— **Diode, Lithography, Self-alignment, Silicon Solar Cell**

XI. Introduction

Electric power demand is continuing to increase and is currently satisfied by Earth's limited resources, primarily oil. The Sun could supply most, if not all the power demands of this world. This is not currently done because of the payback cost of solar cell fabrication relative to their efficiencies. Crystalline silicon solar cells are one method to convert solar energy into electrical energy.

Crystalline silicon solar cells typically require patterning of the front metal contact through lithography. A method to pattern and avoid lithography for the front contacts is the self-alignment of the front metal contacts. Fig. 1 shows a schematic of both a simple solar cell and the mask-less solar cell created in this project.

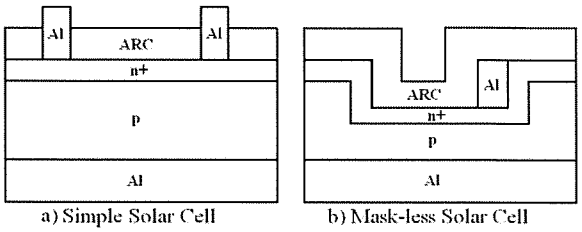

Fig. 1. Schematic of a) simple solar cell and b) mask-less solar cell

A crystalline silicon solar cell has an n doped region, and a p-doped region, to create a diode. When a photon strikes the depletion layer within a crystalline silicon solar cell, it generates an electron hole pair which is separated due to the diode's electric field causing the electrons to go to the p region and the holes to go to the n region. The electrons and holes are then captured by metal contact on either side. Antireflective coatings are also typically applied to reduce the high reflectivity of silicon. Fig. 1b shows the schematic of a mask-less solar cell. In this diagram you can see the recessed trench and along the side of the trench there is Aluminum, Al. In both schematics the only pattern layer is the Al front contacts.

XII. Theory

For this project, the trenches are physically grooved using the KS 775 Wafer Saw. Fig. 2 shows a diagram of the variables that needs to be

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characterized such as width of each trench, depth of each trench, and the spacing of each trench. The trench width is set by the thickness of the diamond grit saw blade which was found to be approximately 200 μm, while the spacing is set by the indexing capability of the saw with deviations around 20 μm and trench depth is variable based on the recipe with deviations of 20 μm.

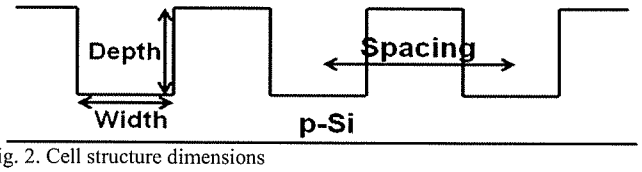

Fig. 2. Cell structure dimensions

Other important characteristics of the trenches that were investigated are the sidewall profile and edge roughness of the cut. Fig. 3 is an cross-sectional image of trenches without a steep sidewall.

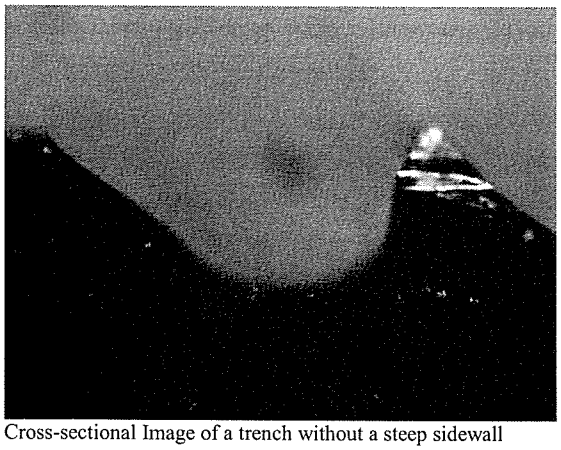

Fig. 3. Cross-sectional Image of a trench without a steep sidewall

Fig. 4 is an SEM image of the wafer surface with a groove showing a really rough wafer surface around with the saw cut.

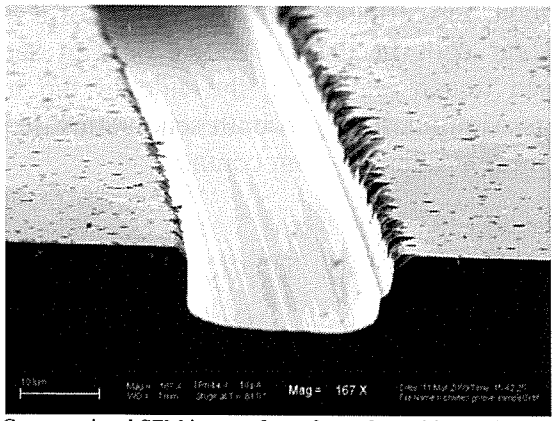

Fig. 4. Cross-sectional SEM image of a wafer surface with saw damage

Both poor sidewall and rough surface was solved by using a new wafer blade. Fig. 5 shows a image of a wafer with hundreds of grooves cut into it.

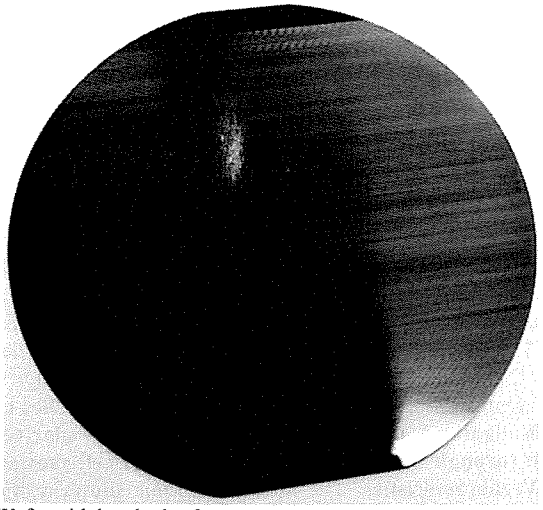

Fig. 5. Wafer with hundreds of grooves

An oblique angle evaporation was the second process step that undergone extensive characterization. The trench creation was necessary to make this step work. Evaporated metal travels linearly away from the metal source and if the wafer is placed at an oblique angle, the evaporated metal can adhere to the side of the trenches. This results in self aligning metal. Fig. 6 is an illustration of how the oblique angle evaporation works.

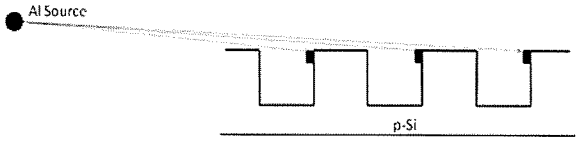

Fig. 6. Oblique angle evaporation

The CVC evaporator was used to perform the oblique angle evaporation. A wafer holder was created to hold a wafer at an oblique angle. Fig. 7 is an image of the oblique angle evaporation setup. Fig. 8 shows the controllable angle function of the wafer holder.

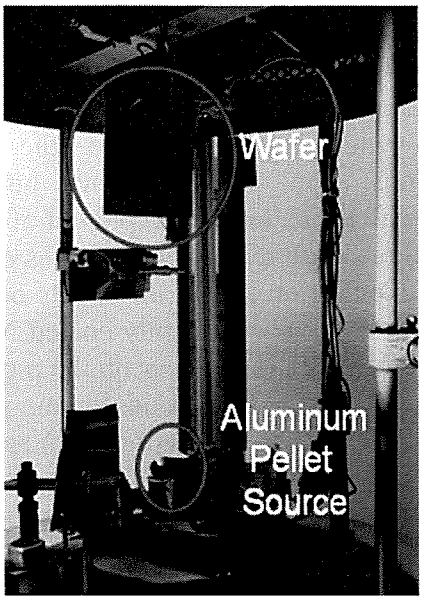

Fig. 7. Oblique angle evaporation in the CVC evaporator

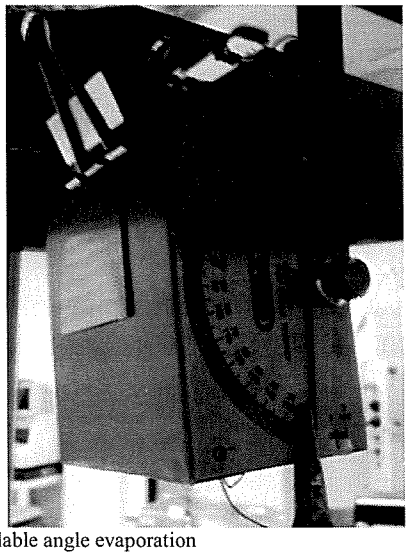

Fig. 8. Controllable angle evaporation

Two methods of characterization was done to optimize the angle of the evaporation, SEM imaging and electrical probing. Electrical probing was done after growing oxide on the wafer with trenches grooved followed by an aluminum evaporation allowing for only electrical readings from the aluminum. The optimized aluminum angle was determined to be about 4 degrees.

XIII. Major Processing Steps and Treatment Combinations

The major process steps for the solar cell are as follow:

1. Trench Creation using the KS 775 Wafer Saw
2. RCA and SRD
3. Oxide Growth for a rear diffusion mask using the Bruce Furnace
4. Top Oxide Etch using the Drytek
5. n+ Diffusion using SOG N-250 with the Bruce Furnace
6. Oxide Etch
7. Front Contact Aluminum Evaporation at Oblique Evaporation
8. Rear Contact Aluminum Evaporation
9. Nickel Paste bus Interconnect

TABLE I
Different Treatment Combinations

Wafers	Trench Depth	Sinter
1	50 μm	No
2	50 μm	No
3	110 μm	Yes
4	110 μm	Yes
5	110 μm	No

XIV. Results

The following figures are I-V curves for wafers 2, 3, 4 and 5. Wafer 1 was scrapped.

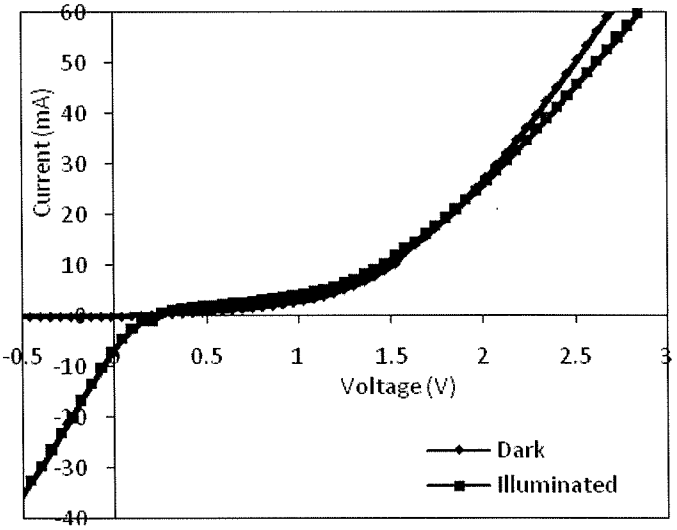

Fig. 9. I-V curves of a wafer 2 in dark and illuminated conditions

Fig. 9 shows the I-V curve for wafer 2 under dark and illuminated conditions. Under dark illumination conditions, the diode shows a I-V where current doesn't flow with a negative applied voltage and in the forward applied voltage, there is a turn on voltage around 0.6V, typical of a silicon diode. This is followed by an exponential gain in current. The diode ideality factor, n, is approximately 1.7. Under illuminated conditions, the I-V curve shows a

dramatic negative current for voltages below 0.25V. This isn't the I-V curve of a solar cell but it does show that this device is light sensitive. There is definitely something occurring during the illuminated conditions, giving the abnormal I-V curve.

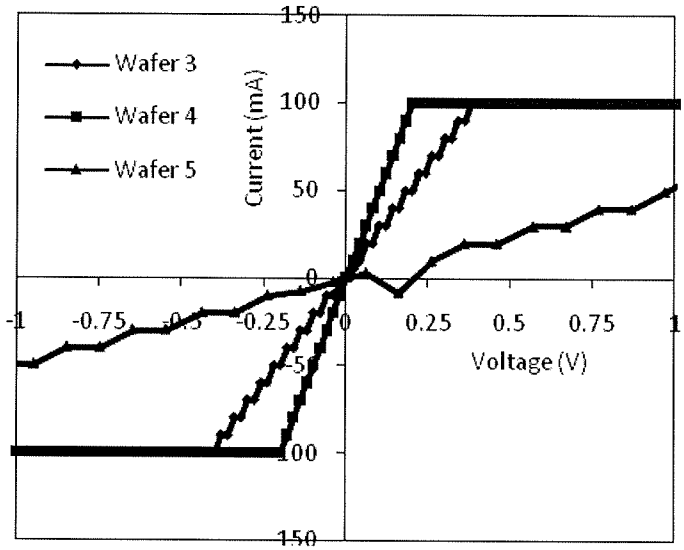

Fig. 10. I-V curves of wafers 3, 4 and 5 showing resistor I-V characteristics

Fig. 10 shows I-V characteristics of the other three solar cells as resistors with resistances of 4 Ω, 2 Ω and 19.2 Ω for wafers 3, 4 and 5 respectively. Shorts are occurring in this wafer resulting in a resistor.

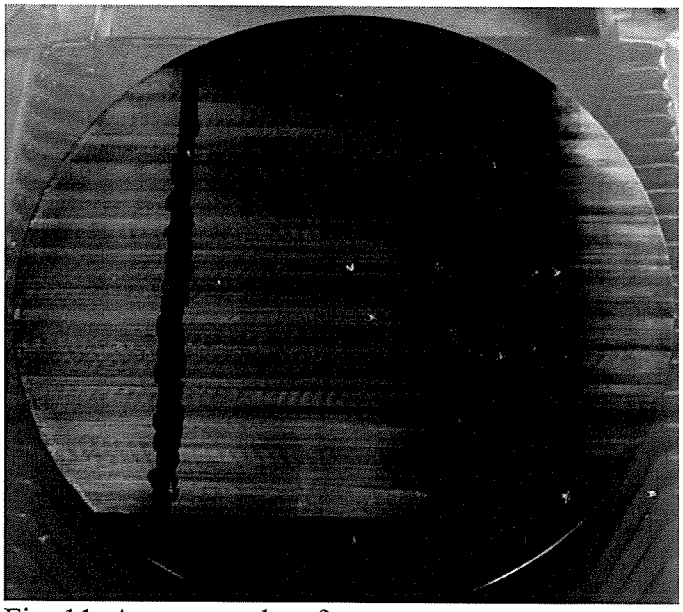

Fig. 11. A processed wafer

XV. Analysis

An investigation into what went wrong for the other 3 wafers leads back to the treatment combinations. The only difference between the wafers is wafer 2 had trench depths of 50 μm while the other three wafers had trench depths of 110 μm. The only explanation is that the shorts on the solar cells are due to a non-uniformly coated N-250 spin on glass (SOG) for the n+ layer on the p type wafer. There is an increase likelihood for air pockets to remain in the trenches and kept certain spots on the wafer surface to remain p. When the Al front contacts and bus paste are applied to the solar cells, it creates the p-n junction shorts. Fig. 11 is an illustration of how an air bubble could create the p-n junction short.

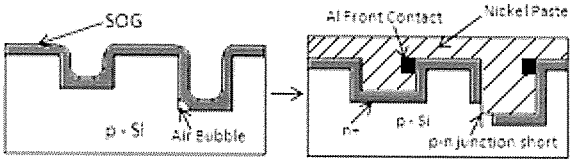

Fig. 11. Schematic Diagram showing the creation of the p-n junction short

This was not considered a problem in the beginning because SOG was assumed that it would coat the trenches uniformly but for this topography it wasn't the case. Normally, SOG is used on a flat or near flat topography. This could explain the abnormal I-V curve under illuminated conditions for wafer 2.

XVI. Conclusion

A mask-less solar cell was made using the processes developed such as the trench creation and oblique angle evaporation. Problems occurred with the p-n junction shorts due to a non-uniform SOG coat. In the future, a different technique to create the p-n should be utilized to avoid the p-n junction shorts.

XVII. Acknowledgments

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