Development of a Planarization Process for the Fabrication of III-V on Silicon Esaki Diodes

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Abstract—**Esaki diodes are tunnel diodes with a very abrupt and degenerately doped PN junction. This abrupt junction causes the conduction bands to overlap, thus allowing for tunneling when a small bias is applied. III-V on silicon Esaki tunnel diodes offer higher performance at lower power supplies compared to silicon. A vertical mesa etch is used to isolate the Esaki devices from each other. The etch results in a significant undercut below the gold contact which can cause issues with electrical testing. When probed the gold contact can short to the substrate. The solution to this is the addition of a dielectric layer around the tunnel diode. The dielectric layer will reduce the topography variation caused by the mesa etch and prevent the metal contact from shorting to the surface. Bisbenzocyclobutene (BCB) is a spin on polyimide with a low dielectric constant (k = 2.5) and a high degree of planarization.**

The development of BCB planarization process allows for better electrical testing of the Esaki diodes. Further, this BCB planarization process can be incorporated into e-beam lithography process and utilized in the fabrication of Tunneling Field Effect Transistors (TFET) and Heterojunction Bipolar Transistors.

Index Terms— **Esaki Diodes, Bisbenzocyclobutene (BCB)**

I. Introduction

For many years semiconductor industry has been mainly focused on silicon. As technology has progressed the industry is nearing the limits of silicon scaling. With ever smaller feature sizes and more transistors per device, traditional silicon scaling is approaching a wall. That wall is power. With increase in the number of gates per chip, power consumption has become a critical design factor. To overcome these power challenges recent research has been focused on alternative semiconductor materials such as III-V compound semiconductors. III-V compound semiconductors offer the advantage of good low and high field electron transport properties. While the III-V semiconductors offer improved device performance there are many more production challenges associated with them when compared with silicon. III-V compound semiconductors are more expensive and difficult to process than silicon substrates. Recent research has focused on incorporating the benefits associated with III-V semiconductor with silicon substrates.

The incorporation of III-V semiconductors on silicon substrates presents several fabrication challenges. The fabrication III-V based Esaki tunnel diodes on silicon substrates utilizes an etch process to isolate individual devices. This isolation etch or mesa etch results in a significant undercut bellow the contact metal layer. The result of this undercut is an uneven topography that can cause the metal contact layer to short the diode to the substrate. Figure 1 shows two III-V Esaki diodes fabricated RIT. The diode to the left shows a gold contact on top of a mesa, with severe undercut. The diode to the right shows another diode where the undercut topography variation has caused the gold contact to break off of the diode mesa and short to the substrate surface.

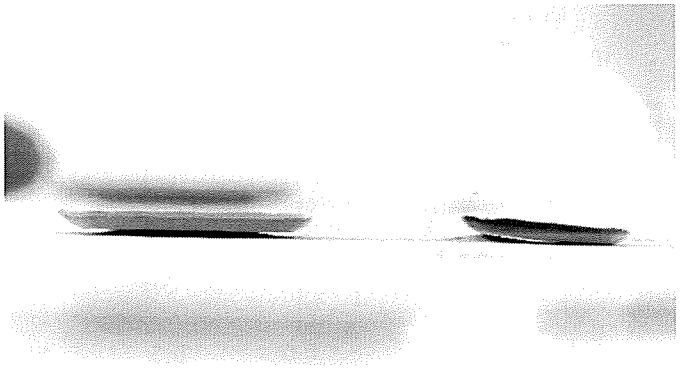

Fig 1. SEM Image of Esaki Diode *Left- Esaki Diode with Undercut Mesa; Right- Esaki Diode Where Gold Contact has shorted to the Substrate* (1)

A dielectric layer is needed to reduce to topography variation caused by the mesa etch and prevent the metal contact from shorting the diode to the surface.

II. Theory

Esaki diodes are tunnel diodes with a very abrupt and degenerately doped PN junction. The abrupt junction causes the conduction bands of the two doped regions to overlap. This overlap allows for tunneling between the two regions when a small biased is applied. An applied reverse bias on the Esaki diode results in Zener tunneling. When a forward bias is applied there is a tunneling component where the current increases with forward bias. At a certain point the current drops as forward bias is increased. The max current value before the current begins to decrease, is referred to as the peak tunneling current. The current continues to degrade as the voltage is increased until the forward applied bias reaches a certain value where the current will begin to increase again. The minimum current before the current begins to increase again is referred to as the valley current. The region where forward biased is increased yet the current decreases is referred to as negative differential resistance. Negative

differential resistance is a key characteristic of an Esaki diode. In this region of negative differential resistance, tunneling is the main current transport mechanism. The current decreases as forward bias is applied due to the conduction bands passing each other as the forward bias is increased. As the conduction bands separate from each other the degree of tunneling decreases. Following the valley point diffusion current is the current transport mechanism. Figure 2 shows these different regions of operation for an Esaki diode as current is plotted against voltage.

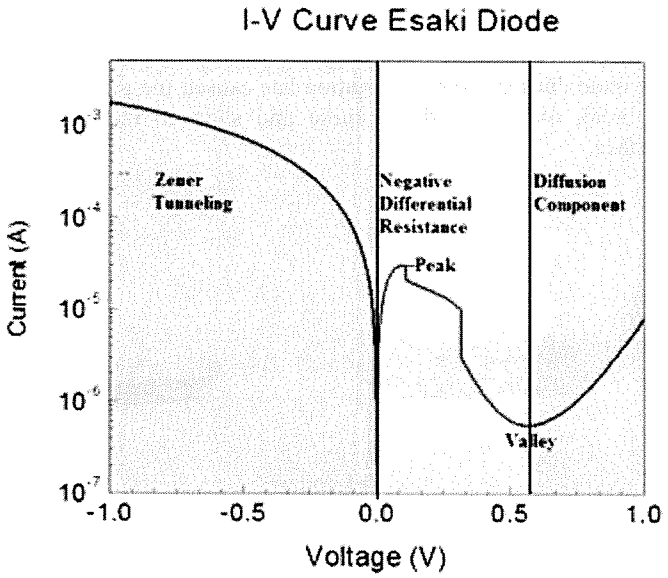

Fig 2. SEM Image Esaki Diode Regions of Operation.

Esaki diode performance is evaluated utilizing the Peak to Valley Current Ratio (PVCR). A high PVCR is desirable for logic applications and noise margin performance. The higher the PVCR the more robust a device is against noise in the input signal. For logic applications a PVCR of 2.0 is needed. The PVCR is the ratio of the peak tunneling current to the lowest tunneling current when forward bias is applied to an Esaki diode. Equation 1 shows the equation used to calculate PVCR.

$$PVCR = \frac{I_p}{I_v} \tag{1}$$

As seen in Figure 2, the peak tunneling current is the max current at the onset of negative differential resistance; the valley current is the current level when diffusion currents begin to be responsible for carrier transport. Current density is another parameter used to analyze and compare different Esaki diode. Equation 2 shows the calculation of current density.

$$J = \frac{I}{A} \tag{2}$$

The current density is equal to the current through the diode over the area of the diode. The current density can be used to normalize electrical performance and compare different sized Esaki diodes.

Esaki diodes have been fabricated in germanium and in silicon semiconductor material systems. III-V semiconductors combine a group III element with a group V element to form a compound semiconductor. III-V compound semiconductors offer improved device performance over other material systems due to their excellent high and low field electron transport properties. The electron velocity for III-V semiconductors is higher than that of silicon. The result of which is ultra fast switching speeds at lower supply voltages. Lower supply voltages equate to less power. While III-V semiconductors offer improved device performance there are limitations to their development. The crystal structure of III-V semiconductors is very weak when compare to silicon. This weak structure limits III-V semiconductors to substrate sizes up to 100mm in diameter. Furthermore III-V semiconductors are more expensive and rare than other semiconductor materials like silicon. Silicon is the second most abundant element on the Earth; the rarity of III-V semiconductors makes them cost up 16 times more than silicon. Integrating III-V semiconductors with silicon substrates via epitaxial growth allows for the combination of improved device performance with strength, larger size substrates and processing capability of silicon.

InGaAs is an III-V semiconductor that has been used to fabricate Esaki Diodes on silicon substrates. A mesa etch is utilized to isolate individual Esaki diodes from each other. The isolation etch process uses sulfuric acid and hydrochloric acid to etch away the InGaAs layer not masked by a gold contact. However this isolation etch has a relativity low degree of anisotropy. The InGaAs layers under the gold contact, which compose the Esaki diode, are partially etched. This undercutting of the material results in the possibility of the gold contact shorting the diode to the substrate. Furthermore the device sidewalls are exposed by the etch process. These exposed sidewalls can create chemically active dangling bonds and introduce surface states. These defects can lead to leakage and long-term device stability issues (2). Benzocyclobutene (BCB) layers have been used in III-V semiconductor fabrication to provide a planarization layer and provide passiviation of the sidewalls (2).

BCB has a dielectric constant of 2.5, which is lower than dielectric constant for silicon dioxide of 3.9. However the silicon dioxide on III-V semiconductors requires a Chemical Vapor Deposition (CVD) step. The CVD process used to deposit silicon dioxide can lead to stress on the Esaki diode. BCB is spin coat process with a low temp thermal cure process. The spin coat and thermal cure process can be adjusted to optimize stress on the III-V Esaki diode. Stress can induce strain on the diode thus effecting channel performance in the device.

BCB layers are generally applied through a spin coating process followed by a curing step. The spin coating process is one of the key factors to BCB planarization properties. Varying the spin speed affects the thickness of the polyimide coating. The higher the spin speed the lower the thickness of the polyimide. BCB is a polyimide composed of

oligmers. When the BCB is heated during a post application-baking step these oligmers crosslink causing the BCB to cure (3).

The ability of the polyimide layer to reduce the surface topography and planarize a surface is given by the Degree of Planarization (DOP) as seen in Equation 3 (4)

$$DOP\% = \left(1 - \frac{H_2}{H_1}\right) \times 100 \qquad (3)$$

Where H_2 is the final step height of the topography features following planarization while H_1 is the initial step height of the feature. The degree of planarization is affected by spin speed (5)and the variable factors including molecular weight, backbone rigidity, cure mechanisms, solvent volatility, solution viscosity, solids content, feature dimensions, processing and cure conditions(3). A single coat of BCB offers an average degree of planarization of 84% (3). A two-coat application increases the degree of planarization to an average of 96% (3).

The BCB planarization process results in a significant amount of BCB overburden. This overburden is a thick layer that is on top of the isolated device mesa. To make contact to the Esaki diode this overburden needs to removed up-to the top of the mesa. A Reactive Ion Etch RIE process is utilized to etch back the BCB and expose the top of the isolated device. The chemistry used for this RIE process is typically fluorine based. A common etch process utilizes 5:1 O2/SF6 (5). Another etch chemistry that can be used is an 80% O2 20% CF4 mixture (3). Fluorine helps to attack the silicon based BCB and increase the etch rate. Using oxygen plasma without a fluorine component for the RIE can result in undesirable amorphous silicon oxide forming on the surface of the BCB. As a result of this the etching process becomes self-passivating, and the etch rate slows down and eventually stops. The resulting SiO2 layer is brittle and can lead to cracking of the BCB film(6).

III. Fabrication Process

The initial stage of the process development focused on device isolation. The device isolation etch using $H_2SO_4/H_2O_2/H_2O$ (1:8:80) was characterized on three III-V on Silicon substrates as well as an InP substrate. Figure 3 shows the substrates that were studies as part of this experiment. The initial devices were defined using the Karl Suss MA55 for contact lithography with HPR504 serving as an etch mask. A screening experiment was preformed analyzing etch depth versus etch time. Profilometer measurements and SEM cross sections were taken to extract etch rate and undercut profile data.

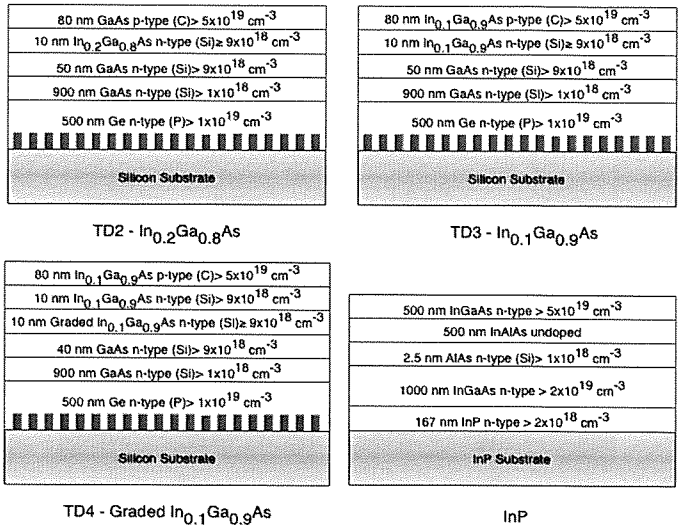

Fig. 3. III-V on silicon tunnel diode substrates structure.

Following the isolation etch characterization the BCB deposition process was optimized. The CSC hand spinner was used for the coating of the III-V on Si substrates with the BCB polyimide. The BCB was applied at 1000 rpm for one minute yielding a BCB thickness of 2.5 microns. The curing bakes were performed using hotplate at 180°C for one minute followed by a 250°C bake in the Blue M oven for one hour. Profilometer measurements and SEM cross-sections were used to analyze the BCB deposition process for film thickness and degree of planarization.

The next stage of the project involved the development of the plasma etch of the BCB layer. The gas mixture, pressure and power parameters of the plasma etch were optimized to create a uniform and controlled etch. The LAM 490 Plasma Etcher was used to etch the BCB in a SF_6/O_2 plasma. A full factorial DOE consisting of 27 runs was preformed to optimize O_2 flow, SF_6 flow and RF power.

A lift of resist process was used for the metallization step. Two layers of LOR5A lift off resist were coated followed by an HPR 504 top coat. A Karl Suss MA55 contact aligner was utilized to align the metal mask to the previously etched mesa. Following alignment, exposure, and develop, gold was deposited via thermal evaporation. The excess gold was then lifted off using Nanoremover PG.

The final stage of the project combined all of the optimized process parameters for device isolation etch, BCB deposition, BCB etching, and metallization to build functional Esaki Diodes. Following this the Esaki diodes were electrically tested and compared to previous Esaki Diodes on III-V substrates without BCB planarization layer fabricated at Rochester Institute of Technology. Figure 4 summarizing the Esaki diode fabrication process including the planarization process.

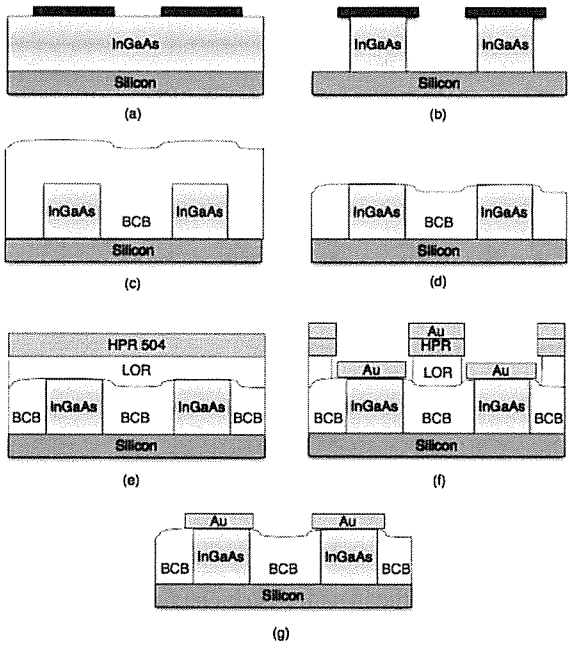

Fig. 4: Esaki diode fabrication with BCB planarization: (a) Define the Esaki diodes via lithography, (b) isolate the individual devices via chemical etching $H_2SO_4/H_2O_2/H_2O$ (1:8:80), (c) seal the devices using a spin on BCB and cure bake (d) etch back the polymer past the top of the Esaki diode in SF_6/O_2 plasma (e) coat with LOR resist and then a top coat of HPR 504, (f) second lithography layer defining contacts then deposit gold, (g) lift off the remaining gold leaving completed diodes.

IV. Process Results

A. *Device Isolation Etch*

The device isolation etch using $H_2SO_4/H_2O_2/H_2O$ (1:8:80) was characterized on three III-V on Silicon substrates as well as an InP substrate. Figure 5 shows the extracted etch depth versus etch time. The etch rate was found to vary with the layer of the device. The substrates have multiple different layers of III-V material. These layers differ in doping and concentration of In and Ga. The result of this that one layer of the device may etch at a greater rate than another.

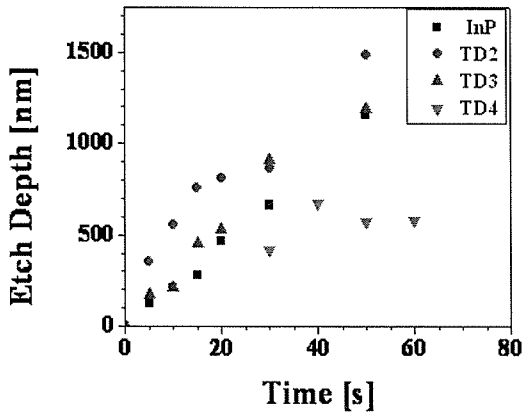

Fig. 5. Etch time versus etch depth for tunnel diode structures studied

This difference in etch rates is apparent in SEM cross-sections. Figure 6 shows an SEM cross-section of TD4.

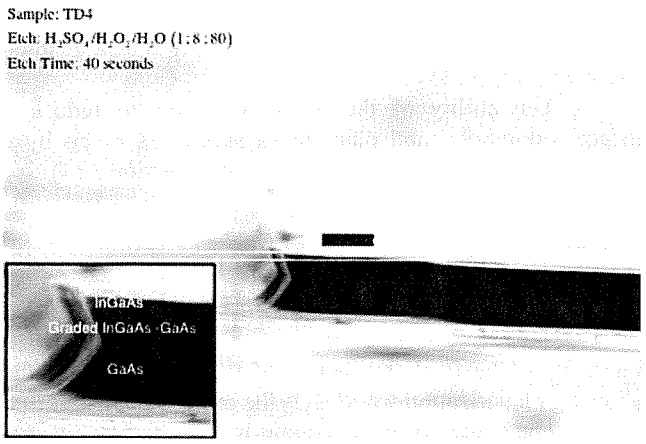

Fig. 6. SEM- cross section of mesa etched in to TD 4. Etch time was 40 seconds. Sample etched in $H_2SO_4/H_2O_2/H_2O$ (1:8:80).

The etch attacking the different layers of the device at different rates leads to this unique hour glass etch profile. Further seen in the SEM cross-section is the pn junction of the Esaki diode. The pn junction is at the top 80 nm of the device. In the SEM cross section this pn junction is the white region on top of the mesa. This over etch past the pn junction indicates that the etch can be limited to 10 seconds. This reduced etch time will isolate the pn junction while minimizing the undercut and initial topography variation caused by the etch

B. *BCB Etch*

The BCB was etch in an oxygen fluorine plasma in the LAM 490. A full factorial DOE was performed to optimize SF_6 gas flow, O_2 gas flow and RF power, for a slow and controlled etch rate. This yielded an optimized uniform BCB etch with an etch rate of 280 nm/min. This optimized recipe has the following parameters; pressure of 325 mTorr, RF power of 100 W, a gap spacing of 1.5 cm, O2 Flow of 100 sccms, SF_6 Flow of 100 sccm

C. *Fully Fabricated Esaki Diodes with BCB planarization.*

Using the optimized etch conditions an Esaki diode was fully fabricated utilizing BCB. Figure 7 shows an SEM cross-section of an Esaki diode with BCB layer

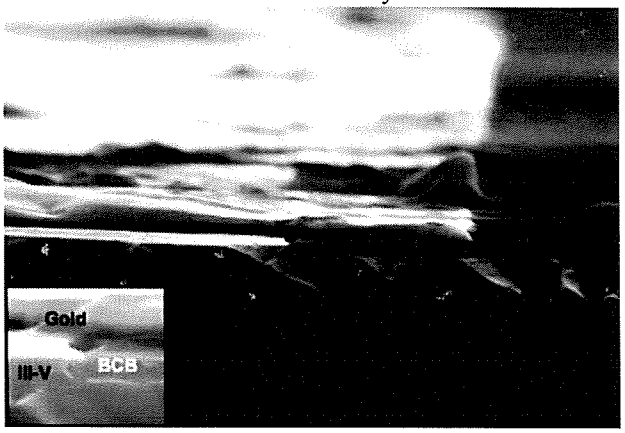

Fig. 7. TD3 cross-section. The BCB fills in around the mesa and is planar to the top of the mesa. The BCB supports the gold contact that extends out form the mesa.

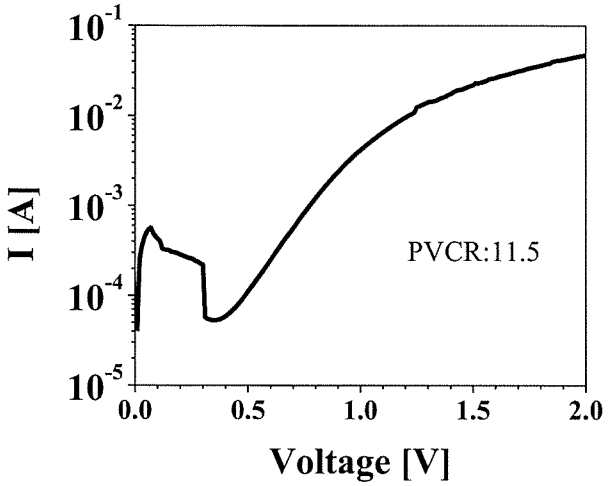

Fig. 8. TD3 – IV curve. Extracted PVCR of 11.5.

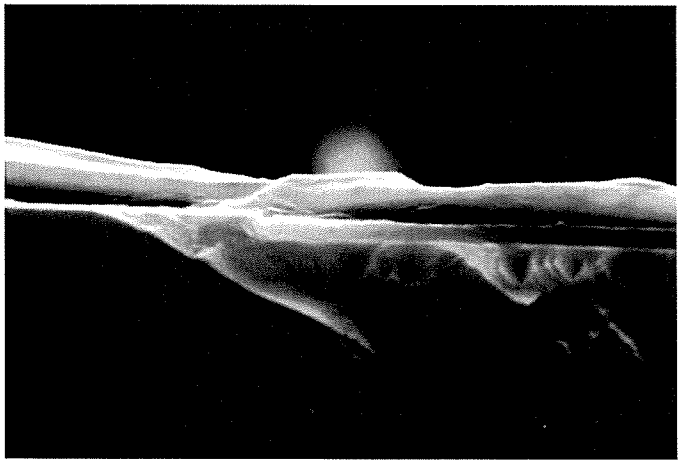

Fig. 9. TD3 – 90° cross section of Esaki diode with gold contact on mesa and BCB. The BCB is not perfectly planar to the mesa. The small step height between the mesa and the BCB has allowed gold to overlap the sidewall of the device especially over the pn junction.

Figure 7. shows that the BCB is somewhat planar to the mesa and that the BCB is able to support the gold contact that extends out form the mesa. The BCB has been able to prevent the gold from shorting out to the substrate of the device. Figure 8 shows the IV curve of the Esaki diode fabricated on TD-3. As seen in Figure 8 the PVCR of the device was found to be 11.5. This PVCR value is quite low. This substrate has been found to yield a PVCR of 56 (7). This low PVCR indicates that either plasma damage or an electrical short is lowering the PVCR.

Upon further inspection with SEM cross-sectioning it was found that there is a slight short along the pn junction. As seen in Figure 9 the BCB is not exactly planar to the top of the mesa. There is a small step height of about 50nm. This step height has allowed the gold to overlap the sidewall of the pn junction. This problem of gold overlapping the pn junction could be solved through shifting the location of the pn junction in a subsequent substrate growth.

V. Conclusion

The BCB planarization process has been shown to isolate and support the gold contact. Since III-V materials are dopants in silicon, there is a risk of tool contamination in a silicon based fabrication. BCB allows for a planarization and dielectric process without the use of contamination sensitive tools. The BCB planarization process can be used with optical and e-beam lithography processes and adapted for use in the fabrication of Tunneling Field Effect Transistors (TFET) and Heterojunction Bipolar Transistors.

VI. Acknowledgments

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