Characterization of P-N Junctions for Variation in Dose and Annealing Temperatures (May 2008)

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Abstract—**The following experiment was completely in order to analyze and quantify the influence implantation dose and post implant anneal conditions have on the source and drain regions of a typical transistor. A DOE experiment was designed to investigate three different variations in each the implantation dose and post implant anneal temperatures of the source and drain regions of the advanced CMOS process transistor at RIT. Electrical characterization was used to obtain quantifiable results for each experimental variation. The experiment was successful in manufacturing a complete analysis for variations in the source and drain doping profile.**

I. Introduction/Theory

Device characterizations of basic building block structures of the CMOS transistor are necessary in designing improvements in overall functioning of the transistor. The source and drain regions of a typical transistor can be profiled and experimentally improved by researching variables related to basic PN junction diodes. In this experiment, P^+N junction diodes were made to simulate the source and drain regions of a typical PMOS transistor. The experiment was designed to examine the influence that P^+ implantation dose and post implant anneal temperatures have on the source and drain electrical characteristics and physical profile. Electrical analysis was accomplished by measuring data for I-V curves for each processing split. Characteristics of the diode, such as series resistance, breakdown voltage and ideality factor, can be extrapolated from the measured curve. Series resistance is related to the slope of the log(I)-V curve at the point in which it deviates from linearity[1]. The breakdown voltage is the point on the I-V curve in which current begins to flow at reverse bias conditions.

Fig. 1 consists of a table that outlines the different DOE splits for each wafer in the experiment. The P^+ implant was varied from $1x10^{13}$ to $1x10^{15}$ cm^{-2}. Also, the anneal temperatures were varied from 900 to 1100°C. It is important to note that the 900°C anneal was done by a rapid thermal process. The 1000°C anneal was performed by a 20 min soak in a furnace with oxide growth present. The 1100°C anneal was processed by a 20 min soak in N_2. Fig. 2 shows the theoretical cross-section of the desired device in the experiment. The desired device includes an N^+ implant to make improved contact to the well.

	P^+ Implant Dose (cm^{-2})	Anneal Temp. (°C)
W1	1×10^{13}	900 RTP
W2	1×10^{13}	1000 Furnace
W3	1×10^{13}	1100 Furnace
W4	1×10^{14}	900 RTP
W5	1×10^{14}	1000 Furnace
W6	1×10^{14}	1100 Furnace
W7	1×10^{15}	900 RTP
W8	1×10^{15}	1000 Furnace
W9	1×10^{15}	1100 Furnace

Fig. 1. DOE breakdown for Implant Dose and Anneal Temperature variations.

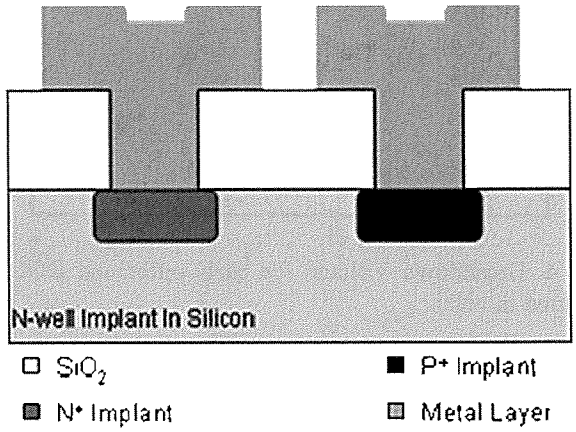

Fig. 2. Theoretical cross section of diode. N^+ Implant used to contact N-well.

II. Results/Analysis

Devices were successfully created for each process variation step. The devices manufactured were simple P^+N junction diodes, which are representative of the source and drain structures of a typical transistor. A top-down picture of the manufactured devices can be seen in Fig. 3. The P^+ implant was done in the small 8x8 μm^2 structure viewable in Fig.3. The U-shaped structure in the figure is where the N^+ implant was implanted and the white area is the metal layer overlaying both implants.

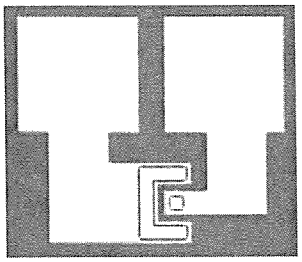

Fig. 3. Top-down photo of manufactured p^+n diode.

In Fig. 4 breakdown voltage was extracted from the I-V curves for each process split in the experiment. The table shows a sizeable increase in breakdown voltage for the 1100˚C anneal. Higher breakdown voltage for PN junctions within the transistor is desirable to limit current leakage. Based on the results, an increase in anneal temperature is ideal to improve breakdown voltage, although temperature increases in transistor manufacturing is not always possible dependent upon material properties throughout the transistor. Also, there is an apparent increase in breakdown voltage dependent upon P^+ implant dose. This increase is significant between $1x10^{13}$ cm^{-2} dose and the two higher implants.

	Breakdown Voltage (V)
W1	-6.35
W2	-6.42
W3	-7.61
W4	-8.96
W5	-6.96
W6	-13.09
W7	-8.37
W8	-8.61
W9	-11.32

Fig. 4. Breakdown Voltage for each wafer and DOE split measured in volts.

	Leakage Current at -5V(μA)
W1	511.91
W2	449.55
W3	356.75
W4	0.0061
W5	122.1
W6	45.59
W7	98.3E-6
W8	60.21
W9	241.4

Fig. 5. Leakage current at -5V reverse bias for p^+n diode for each wafer and DOE split.

Fig. 5 shows a table consisting of the leakage current at -5V reverse bias condition for each of the process splits. It is important to note that the 900˚C rapid thermal anneal process for post implant annealing resulted in extremely low current leakage for both the $1x10^{14}$ and $1x10^{15}$ cm^{-2} dose splits. Fig. 6 and Fig. 7 display I-V characteristic plots for the various splits that were performed. The plot in Fig. 6 highlights process splits under reverse bias conditions. Under reverse bias conditions, there were only slight shifts in current due to anneal conditions at low doses. Current measurements run at higher doses appear to be more dependent upon anneal conditions. Fig. 7 displays a close up of the I-V curve under forward bias conditions. Similar to the reverse bias conditions, post implant anneal conditions appear to have a greater influence on the current measured as the dose is increased. In addition, increases in implant dose resulted in shifts of the overall measured current. Further analysis of the data for this experiment will be presented.

The ideality factor of the P^+N junction diodes can be extracted from the forward bias I-V curves in Fig. 7. The slope of the quasi neutral recombination region of the curve is related to the ideality factor by the following expression:

$$n = \frac{1}{2.3\left(Slope\right)\left(kT/q\right)}$$

The ideality factor is a measure of how 'ideal' a diode is behaving from theoretical expectations. Fig. 8. shows a table of the extracted ideality factors of the devices manufactured. The devices that received the lowest implant dose functioned more ideally than those at higher implant doses.

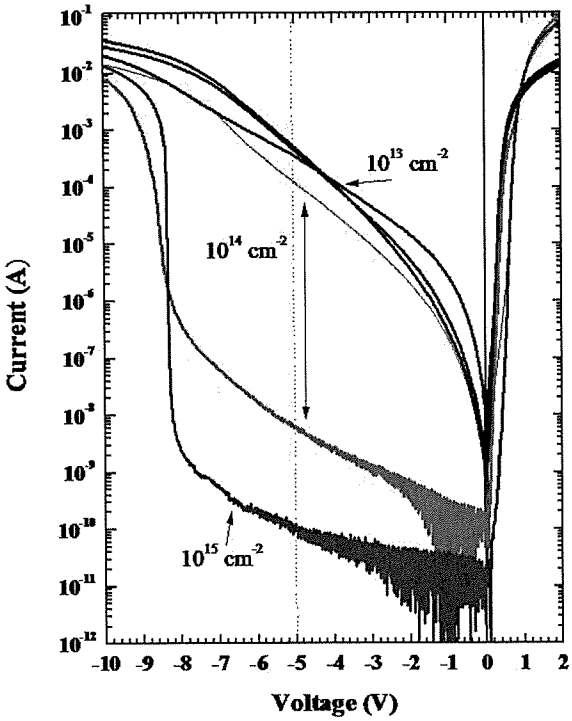

Fig. 6. Log(I)-V Curve. Reverse bias conditions are highlighted for each set of doping variations.

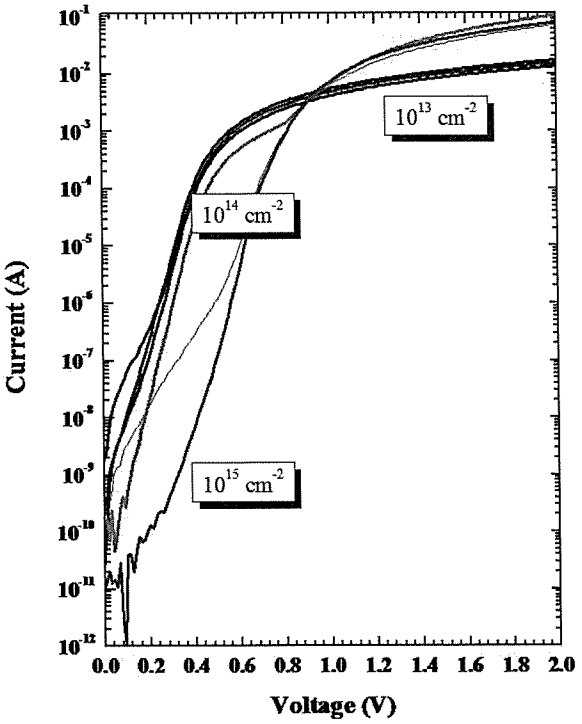

Fig. 7. Log(I)-V Curve. Forward bias conditions are highlighted for each set of doping variations.

	Ideality Factor
W1	1.175
W2	1.141
W3	1.172
W4	1.544
W5	1.503
W6	1.302
W7	1.406
W8	----
W9	----

Fig. 8. Extracted Ideality Factors from slope of quasi neutral recombination region of the forward bias I-V curves.

III. Conclusion

Overall, there were significant effects on device characteristics due to variations in implant dose and post implant anneal conditions. These effects were able to be quantified using electrical testing to produce I-V plots. The plots were then used to extract desired data to further characterize the devices. These results demonstrate the ability to improve transistor performance by experimenting with process conditions on basic components of the transistor.

Acknowledgment

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References

[1] Dieter K. Semiconductor Material and Device Characterization. New York: Wiley-Interscience Publication, 1998.