Process Characterization for Integration of Esaki Diodes into Aspect Ratio Trapping Material

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Abstract—**A process for forming Esaki Diodes in Germanium bulk material was characterized. In doing so its processing characteristics were studied to determine whether it could be transferred into Aspect Ratio Trapping, ART, material. It was determined that transfer was feasible with the optimization of the spin on dopant process and strict control of the wet etching of the spin on dopant and Aluminum. Following process characterization electrical data was collected for a range of devices with varying process parameters. The maximum peak to valley current ratio was 1.5 and maximum peak current density was 5kA/cm^2. The PVCR value was very close to data collected by a group at Notre Dame who's process was the basis for the one used in this project[4]. However, the maximum peak current density was much lower, most likely due the decreased dopant concentration of the spin on dopant. Upon completion of the project a process, which could be transferred to ART, was obtained and baseline data was collected for comparison to future devices.**

Index Terms—**Aspect Ratio Trapping, Esaki Diode, spin on dopant, peak to valley ratio, current density**

I. Introduction

With semiconductor technology continuing to advance into smaller and smaller dimensions it has become increasingly important for new/rekindled areas of device development to progress and lead to new innovation which can lessen the constraints. One such area of interest is in the development of devices in non-silicon material which can lead to different if not better electrical characteristics for new devices. This paper discusses the integration of a process for Esaki Diodes into bulk Germanium and then the difficulties in implementation into Aspect Ratio Trapping (ART) material. By doing so it will allow the confirmation of device operation in non standard material as compared to an already developed process with a more common material base. The process undertaken was adapted from the work done by a group out of Notre Dame.[4]

II. Theory

A. Electrical Properties

The Esaki Diode is a device which has its basis as a standard diode, however, during processing the cathode and anode regions of the device are heavily doped leading to degeneracy. The impact of this is to create a junction which allows for electron penetration through the barrier, known as electron tunneling, since the states on both the n side of the junction and p side of the junction will line up over some finite region of applied voltage.

During Esaki operation there are a few regions of interest which are distinctive to a tunneling device and thus the Esaki diode. These states will be shown in two ways, the first through the band diagram and how it is manipulated during biasing, Figure 2, and the voltage-current curve shown in Figure 3.

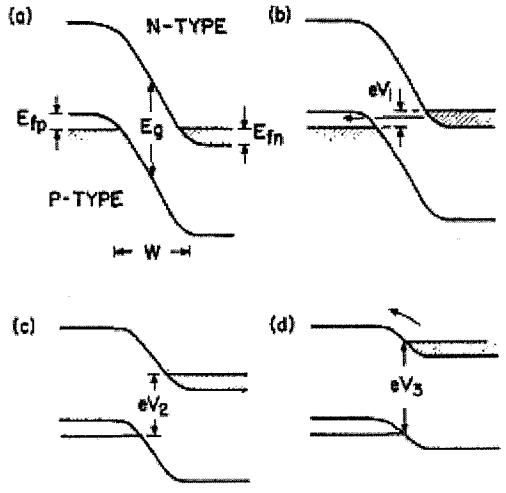

Figure 1: Band Diagrams at Various Bias Conditions[2]

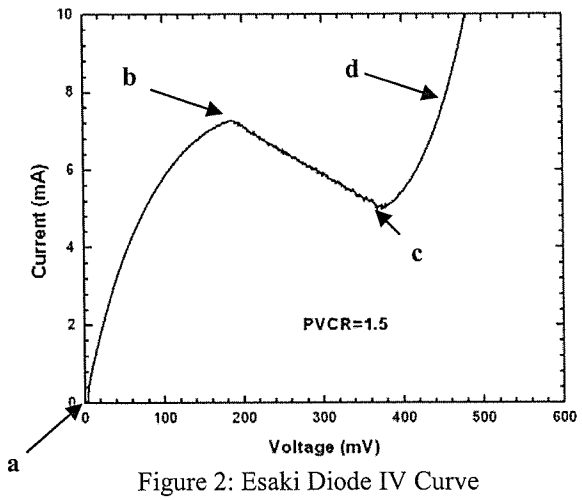

Figure 2: Esaki Diode IV Curve

Initially during non-biased conditions, as seen in (a) of both Figures 1 and 2, there is no current flow since there is no external electric field to drive the tunneling, there can be seen in Figure 1 that there are, however, allowed/occupiable states on both sides of the junction. By beginning the biasing of the junction the condition of (b) is met, where maximum tunneling current is achieved due to the high bias and available states. The current at this point is known as the peak current and is a crucial characteristic of any tunneling device. Biasing the device after the peak current leads to a subsequent valley which is caused by the fact that the states on the cathode and anode side of the device are offset with no overlapping of the states, as seen in (c) of both Figures 1 and 2. With no overlapping of the states there should be, in theory, no current, however, it can be seen at this point that there is some current flow. This is caused by trap states which allow for some electron flow through the barrier.[1] This valley current is necessary for device characterization since it will yield how optimally the device works to inhibit current. The peak current and valley current are often presented as a ratio known as the peak to valley current ratio, PVCR, which allows the determination of the quality of the device. Past the valley the device is highly biased and thus begins to operate as a standard diode, (d) in both Figures 1 and 2.

B. Aspect Ratio Trapping

Aspect Ratio Trapping material, ART, was developed by Amberwave Systems in Salem, NH. In this method a base material, such as Germanium or III-V materials, can be placed onto a host material, such as Silicon with a surface that is free or lattice errors and thus suitable for device fabrication. In standard methods for placement of one material onto another, without any surface modification, the lattice constants of the material must be taken into consideration. This is due to the fact that since they do not have the same distance between bonding atoms at some point a thickness, for the deposited material, will be reached which will cause stress induced lattice errors to propagate through the material. This thickness is known as the critical thickness and is of concern since it can be very small for certain material systems which are of interest for unique device fabrication. To alleviate this problem Amberwave Systems uses high aspect ratio trenches, made in Silicon Dioxide on Silicon, to trap lattice errors above which a clean surface is created, as seen in Figure 3, which can then be used for device fabrication.

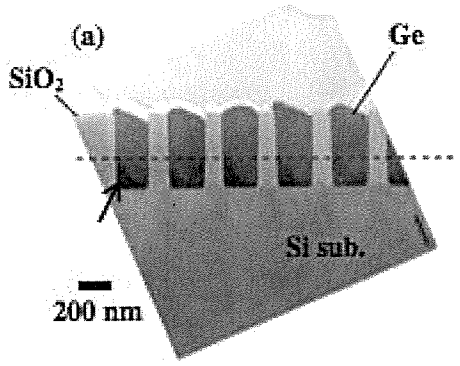

Figure 3: Aspect Ratio Trapping side profile[3]

There are many different applications for such material, however, in this case the most notable benefit is for use as a basis for devices which do not use silicon as a bulk material. This is important since it will provide the alternative material for less cost, since it is on Silicon and not in bulk form, and also allow the continued use of semiconductor toolsets which were designed for use with standard Silicon substrates.

C. Process and Material Considerations

The operation of the Esaki Diode is based upon tunneling current through a PN junction. Since this is the case it is necessary that the doped regions are degenerate such that there are available states for electrons to occupy, thus providing for a high tunneling probability. On the same note the doped regions must also form a sharp junction since any grade between them will only act to reduce tunneling probability and thus the peak current to valley current ratio, yielding a non-optimized device. Although the quantum operation of this device is complicated the needs for device fabrication are not.

For development of such a device the needs as laid out above are obtainable through a number of methods. For high doping it is initially expected that an ion implantation method would be instituted for both p and n regions, however, with the need for a sharp junction, ion implantation would not yield a optimum interface due to ion diffusion. The alternative method to this is to use a rapid melt growth technique.

Initially a spin on dopant with a high concentration is used to n-type dope the substrate for creation of the cathode. Following this Aluminum can be deposited onto the surface. When this Aluminum is then heated above the eutectic temperature of 420°C the Germanium and Aluminum will incorporate into one another and upon cooling create a degenerately doped p-type Germanium area. In addition to this is the fact that it is expected that very little of the dopant, Aluminum in this case, will diffuse past the highly doped area

and thus allow for a very sharp junction. Another benefit to this process is that the doping concentration and depth vs. anneal temperature is well known for Aluminum in Germanium as seen in Figure 4 below, which allows for the optimization of the devices. Also since not all of the Aluminum is incorporated in Germanium as a dopant the remaining layer can be used as a top contact to the device.[4]

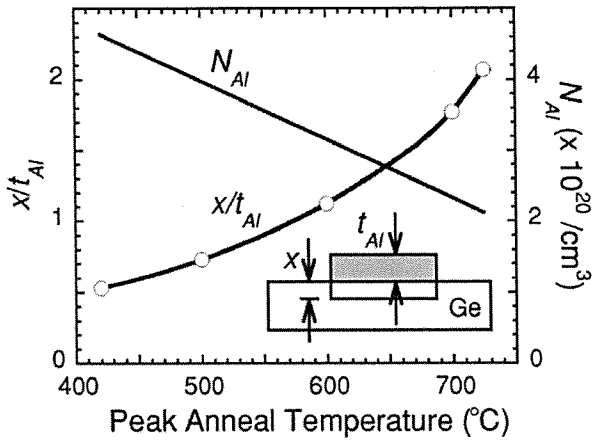

Figure 4: Doping depth and concentration vs. anneal temperature[4]

To undertake testing of the devices it is necessary to make back contact to them as well. This can be done in a multitude of novel methods but the easiest is to recognize the fact that the devices are already serially "wired" across the surface of the bulk germanium. This makes it very easy for testing since top side contacts between adjacent devices is all that is necessary for testing. With this accomplished there are two main parameters which are of particular interest in device operation and characterization. Those two being peak to valley current ratio, PVCR, and current density. PVCR, as stated above, is the ratio between the peak current which propagates through the device during tunneling and then the subsequent minimum current when the tunneling is diminished and normal diode operation begins. This parameter is crucial for tunneling devices such as Esaki Diodes, Resonant Tunnel Diodes, etc since it represents how effectively the devices promote electron propagation through the barrier and then how effectively they prohibit it, thus the quality of the devices. It must be recognized that this device property is dominated by material properties and peak to valley current ratios in the fifties have been obtained which dwarf the 1.5 value seen in many Esaki Diodes. However, the Esaki Diode has a very simple fabrication process as compared to the better performing, but more complicated devices, and was thus the better selection for proof of tunneling device feasibility in Aspect Ratio Trapping material. The second device criterion that is collected for these devices is current density. This parameter is crucial for understanding the ability of the material to promote current flow, thus determining how well it can drive larger circuits, and is especially intriguing to study in Aspect Ratio Trapping material since there is an interest in seeing the effect of confinement based upon the ART's surface.

III. Process

Initially when undertaking fabrication there were a few departures from the process laid out by the group at Notre Dame. First was that the bulk germanium sample used was not an optimized sample for the process since it was not specifically obtained for this project. It was of unknown doping and the orientation was not specified, meaning the diffusion of the n-type dopant may or may not have been optimized to create the highest doping or sharpest junction. This was not a roadblock as much as a nuisance since the Esaki fabrication was highly robust as will be seen later. With that said the first step was to introduce the n-type dopant. This was performed using an Emulsitone Phosphorosilica film with a dopant concentration of $5x10^{20}$ atoms/cm^3, which deviated from the model process that implemented a much higher concentration spin on dopant[4]. Before applying the film the surface of the germanium was prepared using a DI rinse followed by a rinse in isopropyl alcohol. The spin on dopant was then applied using a coater for 60 seconds at 3000 rpm followed by a high temperature bake at 200°C for 15 minutes to drive out solvent and densify the film. The film underwent the drive in step using an AG 410 Rapid Thermal Processor at 800°C for 5 minutes, it was at this step that the first experiments were conducted to determine the impact of temperature on diffusion and thus electrical characteristics. The film was then stripped in 10:1 BOE. Following the strip it was clear that the film was not being fully removed from the surface and led to what looked to be cracking on the germanium surface. This problem was alleviated using a decreased spin time, 8 seconds, to increase the thickness of the film and a two step bake, 100°C for 15 minutes, followed by the 200°C bake for 15 minutes. Implementing this process led to the clearing of the surface properly after the BOE strip.

With the n-type doping region created in the germanium the next step was to create the aluminum contact and p-type region. The aluminum was deposited as Aluminum with 12% Silicon using a CVC601 DC Sputtering system at a thickness of roughly 1000Å. The Aluminum was then patterned using a contact lithography system and wet etched using a solution containing acetic acid, phosphoric acid and nitric acid. The patterned Aluminum then underwent a spike anneal at around 550°C for 1 second. This temperature was varied to determine effect on electrical characteristics. This completed device fabrication and thus led to device testing.

IV. Results

Since the main purpose of undertaking this process was to prove the feasibility of instituting the process developed by Notre Dame[4] and to understand its nuances in regards to processing in ART based material, much of the information gained was not for electrical purposes but material characterization. In terms of material characterization the largest challenge was in implementation of spin on dopant.

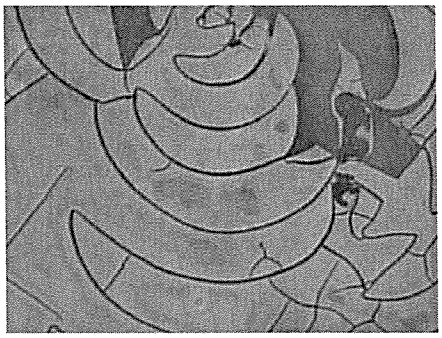

Figure 5: 60 Second Spin, 200°C Densification Bake and 800°C Drive-in

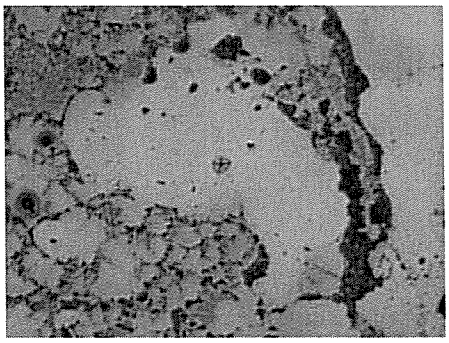

Figure 6: 60 Second Spin, 100°C and 200°C Densification Bake and 800°C Drive-in

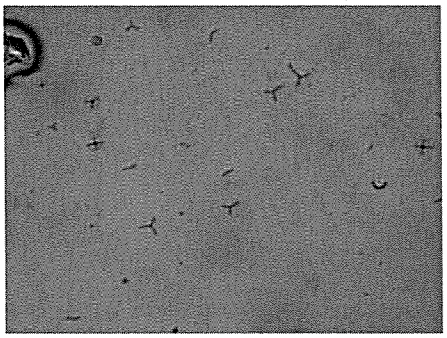

Figure 7: 8 Second Spin, 200°C Densification Bake and 800°C Drive-in

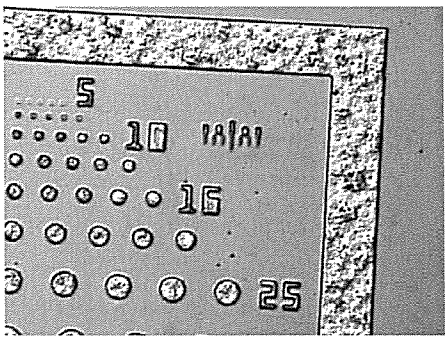

Figure 8: 8 Second Spin, 100°C and 200°C Densification Bake and 800°C Drive-in

During implementation it was found that under the initial process conditions for application, 60 second spin at 3000rpm and then subsequent 200C bake and 800C drive-in, the surface would appear cracked as in Figure 5. To alleviate the issue both a two step densification, 100C and 200C, and a decreased spin time, 8 seconds, were implemented. A small experiment was undertaken to show the effect of each as seen in Figure 6 and 7, it can be seen that until both were implemented the surface was not optimized, Figure 8. It has been postulated that this cracking effect occurred due to dopant suspension solvent interaction with the surface.

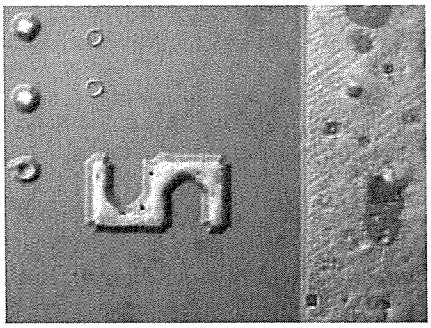

Figure 9: Aluminum post etch and anneal

Another issue which needed to be understood was that dealing with the etching chemistries. Since ART material is based upon a grating of alternating Silicon Dioxide and structure material, in this case Germanium, the BOE will undoubtedly attack the Silicon Dioxide during dopant strip. This means that extra care must be taken during this step such that the Silicon Dioxide isn't overly exposed thus weakening the structure and possibly causing shorts. On the same note it was determined that the Germanium was etched by the Aluminum etching chemistries thus yielding the same concerns as with the dopant etch. The Germanium etching can be seen in Figure 9 with the large slope beneath the aluminum areas. In the future these two issues may be resolved by implementation of dry etch and lift off resist processes.

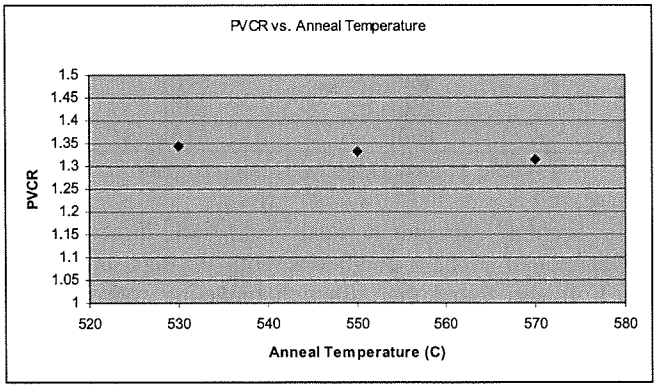

Figure 10: PVCR vs. Anneal Temperature

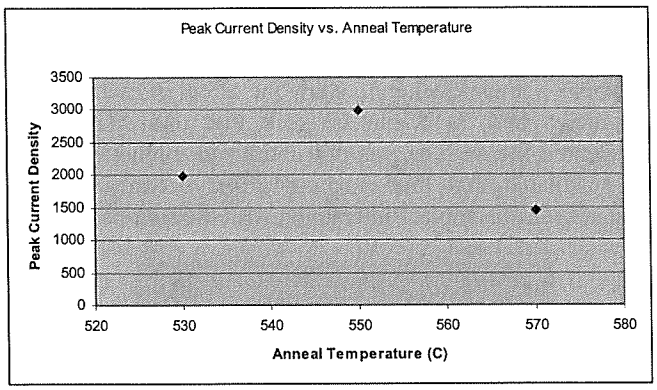

Figure 11: Peak Current Density vs. Anneal Temperature

In undertaking electrical testing two separate designs of experiment were conducted to determine the effect of anneal temperature, aluminum-silicon thickness and drive-in temperature on the electrical characteristics of the devices. The first experiments specifically targeted how the diodes responded with varying anneal temperatures of 530°C, 550°C and 570°C with no other variations in processing conditions. Under these circumstances there appeared to be a change in the maximum peak current density and the max peak to valley current ratio as seen in Figures 10 and 11, however, the data is skewed since so many data points showed a very low PVCR for all temperatures and such a wide variation in peak current density.

Set	Drive in Temperature	Anneal Temperature	Al-Si Thickness
1	800	525	1400
2	800	540	1400
3	800	525	1000
4	800	540	1000
5	825	525	1400
6	825	540	1400
7	825	525	1000
8	825	540	1000
9	850	525	1400
10	850	540	1400
11	850	525	1000
12	850	540	1000

Table 1: Experimental Design Matrix

The second experiment dealt with all three of the aforementioned process conditions with settings as seen in table 1. It was found that although tunneling was found in each case there was not enough data gathered to provide any distinct difference between any process condition set since the range of values was so high and thus the standard deviation, as seen in Figures 12, 13 and 14. This did not result in a failure of the experiment since it showed that the process was very robust and thus suitable for implementation in ART material. The data did show that maximum values for PVCR of roughly 1.5 were obtainable which was what was reported at Notre Dame for peak to valley current ratios.[4] Figure 15 below shows much of the data collected during this project vs. anneal temperature and Figure 16 shows the IV characteristic of the device with the highest PVCR. All of this information is crucial for comparison to ART devices to determine the impact of the alternative material.

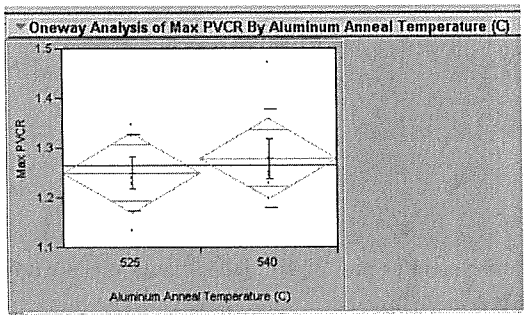

Figure 12: JMP data for anneal temperature

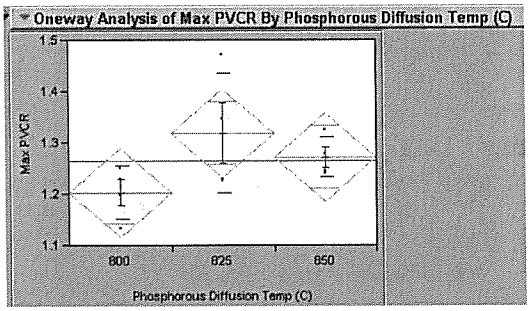

Figure 13: JMP data for diffusion temperature

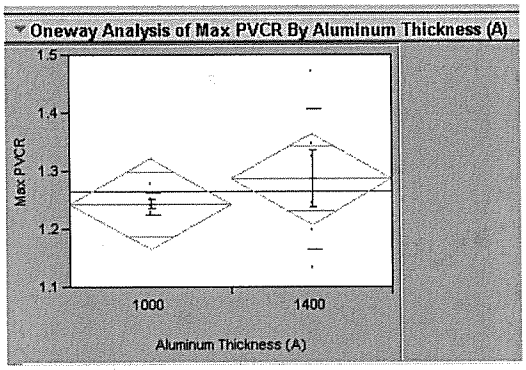

Figure 14: JMP data for Aluminum thickness

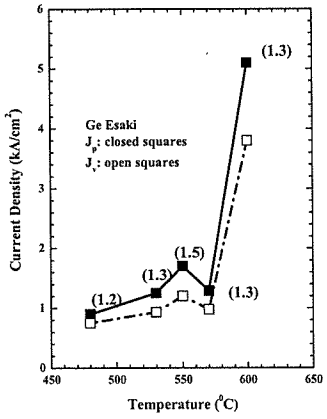

Figure 15: PVCR and Peak Current Density vs. Anneal Temperature

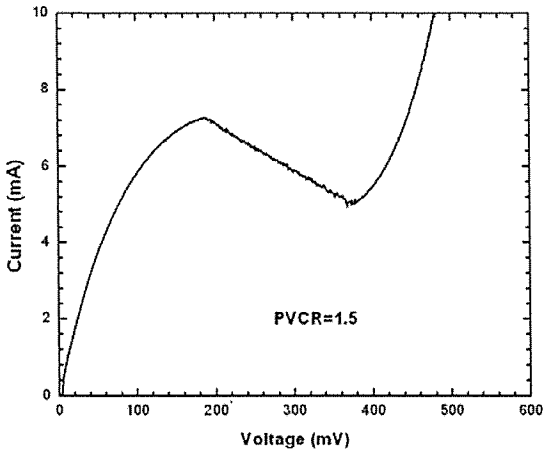

Figure 16: IV Curve for maximum PVCR device

V. Conclusion

By undertaking the implementation of a process to fabricate Esaki diodes in bulk germanium a process for implemention in non standard material has been obtained. Initially concerns of etching in BOE were examined and it was determined the best option was to ensure correct timing in the etch. At the same time it was found that the Germanium was being etched at a very high rate by the chemistries of the Aluminum etch. This was unexpected and therefore yielded important knowledge for implementation into ART based material, where it is imperative to have the least amount of unnecessary surface manipulation as possible. To alleviate this issue timed etches were instituted, however, another method for counteracting this effect would be the institution of a lift off resist process for removal of the patterned Aluminum. Material characterization also yielded knowledge into the processing conditions of the spin on dopant where a more satisfactory process was necessary to correct for inferior surface quality seen with basic processing conditions. For electrical testing two designed experiments were performed on a variety of process conditions to determine effect on peak to valley current ratio and current density. In both experiments a few trends were seen on the surface, but due to the range of variation, in both PVCR and peak current density, there were no trends that could be considered statistically significant. What could be said was that the process was very robust since most devices across a sample exhibited tunneling characteristics and that the maximum PVCRs were the same as those seen in other studies. Future research into this process should yield a more optimized method, however, at the moment this process could be implemented into ART material and provide operational devices for characterization.

Acknowledgment

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