# Fabrication of Thermally Actuated Micromirror using CMOS Compatible Surface MEMs Process with $XeF_2$ Release etch

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*Abstract*—**Thermally actuated micromirrors were fabricated to demonstrate a CMOS compatible surface micromachined MEMs process that was developed. A key step in the process was the used of a XeF2 etch to release the structures. A design was created that varied key factors including mirror pad size and number of anchors. For the smallest pads attached by a single anchor, the length and width was varied. The release etch was found to require a sacrificial layer of greater than one micron for fest lateral undercutting. Mirrors with the longest and narrowest necks were found to display the greatest deflection.**

*Index Terms*— **Thermal Actuation, Micromirror, Surface MEMs, $XeF_2$**

## I. Introduction

Micromachined mirrors on silicon substrates have been fabricated for quite some time. Their most notable use is the digital micromirror device (DMD) commercialized by Texas Instruments for television and projectors. The demand for optics-lab-on-chip devices has increased as integrated microsystems become more prevalent. While the DMD works well for its specialized application, its binary nature limits the scope of its use. A thermally actuated micromirror offers analog positioning allowing a much broader range of applications. With this technology optical switching matrices or optical multiplexers are conceivable.

## II. Theory

### A. Review Stage

A surface micromachined MEMs fabrication sequence compatible with fully processed CMOS wafers was developed. The design was based upon previous work done at the RIT using bulk fabrication methods [1]. The updated process is constrained to low temperatures ($T < 400°C$) and makes use of only deposited layers. The devices were formed using a 2 μm layer of tetraethyl orthosilicate (TEOS) deposited above a sacrificial silicon layer with the mirrors defined using reactive ion etch (RIE) to create a trench in the structural oxide. Using a DC magnetron sputtering system, tantalum and aluminum layers were deposited for the formation of heater elements and contact regions, respectively. Polyimide was applied as the actuating mechanism, with a $XeF_2$ silicon etch used to release the structures. An image of a typical mirror as created by Clever 3D process simulation is shown in Fig. 1.

A mask layout was created to incorporate as many variations of the micromirror design as possible. Varied design parameters included the length, width and number of anchors, as well as the width of the trench etch. Serpentine and ladder resistor designs were used that scaled to the size of the anchors. The polyimide pad placed over the anchors induced a tensile stress when cured, pulling the mirror out of the wafer plane. When heated by the underlying resistor, the large thermal expansion of the polyimide allows the position of the mirror to be controlled. This technique provides analog positioning of the mirror as opposed to the digital versions that are in commercial production today.

## III. Design

The design was created in Mentor Graphics Expert layout software. All of the mirrors were created within the 12 pin test probe pad for ease of testing. Three different mirror sizes were created, the largest (1000 x 500 μm) fills the entire pad and had either 1, 2, or 4 anchors. The middle sized mirrors were 500 x 250 μm and had either 1 or 2 anchors. For the smallest mirrors with a square pad 250 μm on a side, the length and width of the single anchors was varied. Six of the single mirrors fit within the test pad with anchor lengths of 0, 50, 100 (x2), 150, and 200 μm. This pad was replicated with anchors widths of 250, 150, 100, and 50 μm. All of the designs were created with the width of the trench defining the mirror as 2 μm, 5 μm and everywhere the mirror structure is not. Mirrors were fabricated with both ladder and serpentine type heater elements. Test structures were included to determine the intrinsic stress of the heater and metal layers as well as their resistivities. Microhotplates were also included in the design as they were compatible with the process sequence. The final cell layout can be seen in Fig. 2. This cell was scaled across multiple form factors (¼X, ½X, 1X, 2X, 4X) to create the final die.

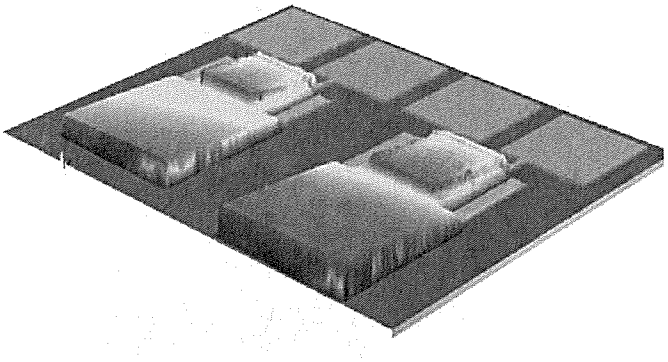

**Fig. 5** Topographical profile of released micromirrors from Veeko Wyko NT1100 Optical Profiler. Mirrors shown have anchor lengths of 150 μm and 200 μm, and a width of 200 μm.

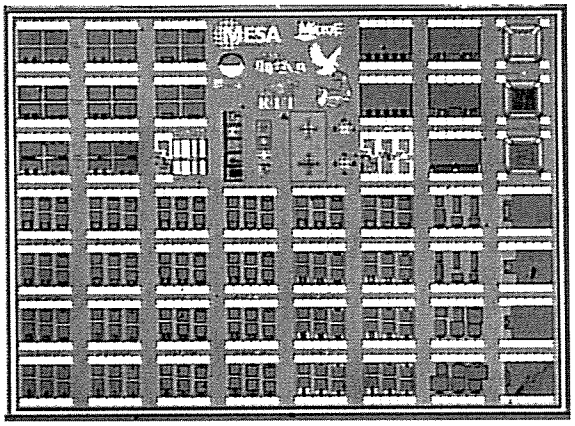

**Fig. 2** Optical image of 0.25X form factor devices at 2X. Device fabrication is finished and awaiting only the release etch.

## IV. Fabrication

The starting substrates for the process serve only as mechanical supports for the devices. Heavily arsenic doped 6" 100 silicon wafers were used due to their abundance. Onto this 1 μm of oxide was deposited from TEOS in an Applied Materials P5000 at 390° with 500 W. The sacrificial silicon layer was deposited using e-beam evaporation in the CHA. The source for the silicon was a ground up 2" wafer placed into a carbon crucible. The silicon layer was patterned and plasma etched to leave only select release areas. An additional 2 μm of oxide was deposited to form the structure of the mirror. This layer was patterned with the trench layer outlining the mirrors, and the oxide was etched anisotropicaly in the P5000 RIE chamber.

First attempts to etch the trench caused arcing events in the chamber around the edge of the wafer. It was initially thought that the secondary flats on the wafers were exposing part of the seal. New substrates were acquired that did not have a secondary flat, but were SOI wafers. These wafers were carried through the same fabrication as previously described. Upon attempts to perform the oxide trench etch, the same arcing events were observed. These created large variations in

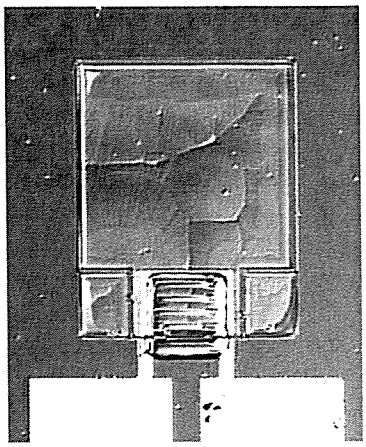

**Fig. 3** Nomarski enhanced optical image of typical mirror showing underlying silicon ridges

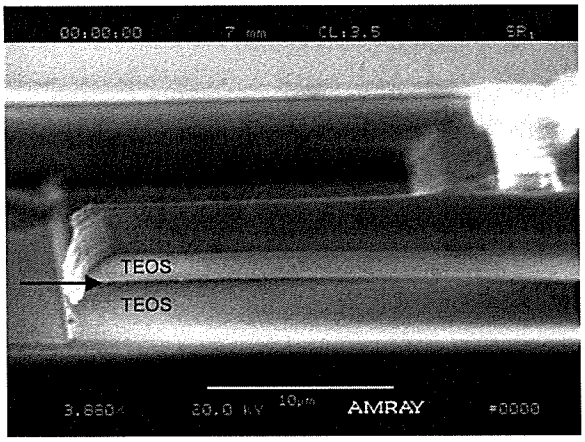


**Fig. 4**. SEM Cross-section of partially released mirror with TEOS layers labeled

the DC bias of the chamber which caused unpredictable etch rates. The cause was eventually determined to be poor electrical contact with the electrostatic chuck due to the presence of a backside oxide. This was removed by applying a blanket coat of photoresist to the wafers and submerging them in BOE (10:1 DI:HF) for 20 min. Pinholes in the resist coat did allow some HF to attack the oxide, although this did not have a significant effect on yield.

A thin layer of tantalum was deposited using DC magnetron sputtering in the CVC 601. A 4" target was used at a pressure of 5 mTorr with 250 W. The deposition rate was found to be ~100 Å/min. Tantalum was chosen for it high etch resistance and melting point. The etch resistance was required as the heater elements would be exposed during the etching of the contacts. Once patterned the tantalum was etched in a LAM4600 Chlorine etcher. A low power (125 W) recipe was used, and 1500 Å was found to etch completely in 45 sec. Aluminum was deposited in the same DC sputter system using the standard RIT metal process for electrical contacts to the heaters. A power of 2000 W was used for the 8" target at 5 mTorr. The use of an ILD was avoided as the use of vias had caused problems in previous work. The patterned aluminum contacts were wet eched at 50° for 2 min with agitation. The

polyimide used was Durimide 112A, a non-photosensitive film that could be etched by positive developer. The polyimide was applied with a static dispense followed by a 15 sec spread at 600 RPM. Spinning at 2000 RPM for 45 sec resulted in a 4 μm thick polyimide film with relatively good uniformity. Following a stepped softbake at 100° C and 120° C the wafers were coated with photoresist. The develop time had to be reduced to 30 sec due to significant undercutting or the resist. The resist was removed by a simple spray with acetone, followed by IPA and a DI water rinse and spin dry. The polyimide was cured in the Heraus Vacuum oven at atmospheric pressure in a $N_2$ ambient. The oven was set to 400° C though typically only reached ~350 – 370° C. The thickness of the polyimide layer was measured to decrease from 3.4 μm to 2.4 μm due to the cure. While significant this is not the 50% volumetric contraction the material is capable of.

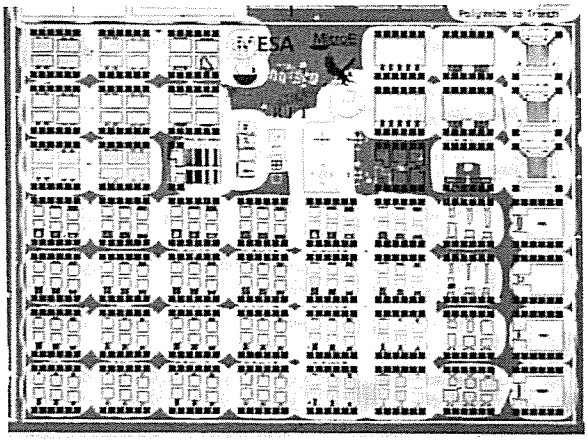

**Fig. 2** Optical image of 0.25X form factor devices at 2X on unpatterned LPCVD polysilicon after release etch. Note significant lateral encroachment.

The devices were released using the Xactix $XeF_2$ etcher. The system consisted of a $XeF_2$ source connected to an expansion chamber that allowed the material to sublimate up to its vapor pressure. The expansion chamber is isolated before being opened to a sealed vacuum chamber containing the samples. The system simply pump –purges the chamber with $XeF_2$ gas, and soaks for a set period of time and cycles.

Due to issues with the initial process runs, a revised process was proposed. A significantly thicker sacrificial silicon layer was deposited to reduce the effects of mass-transport limitations. This was also deposited as polysilicon in an LPCVD system. To further investigate effects of the relase etch devices were fabricated on bulk silicon in addition to un-patterned and patterned sacrificial layers, To prevent etching of the heater elements devices were created with aluminum heater elements. This required a slight change to the process sequence as the heater elements were exposed during the etch to form the contacts. To address this 2 μm of aluminum was deposited immediately after the structural layer. Slightly thicker contacts were used here due to concerns about connectivity over the topology from the thick silicon layer. After the contacts were patterned a thin (~2000 Å) layer of

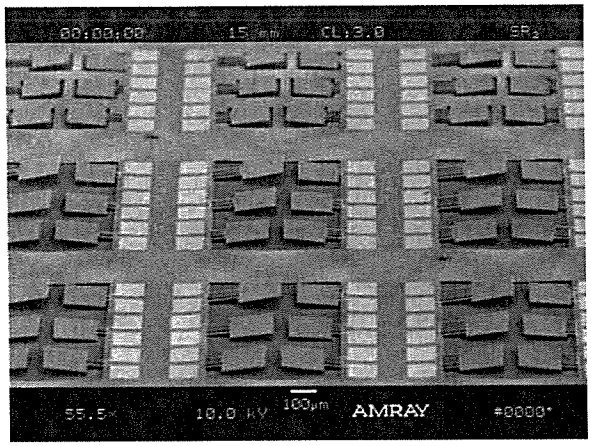


**Fig. 7** SEM image of released single anchor mirrors on unpatterned LPCVD sacrificial silicon

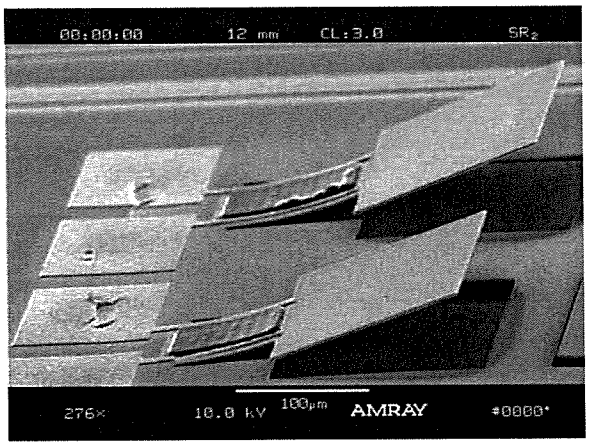


**Fig. 8** SEM close up of released single anchor mirrors on unpatterned LPCVD sacrificial silicon. Mirrors shown have anchor lengths of 150 μm and 200 μm, and a width of 50 μm.

aluminum was deposited that served not only as the heater elements but also a hard mask for the trench etch. The rest of the process followed as described above.

## V. Discussion of Results

The arcing events during the trench etch proved to one of the main challenges of fabrication. The arcing appeared to be stemming from the edge of the wafer at the location of the secondary flat. When the SOI substrate wafers were used the same arcing events were observed, however from random location. The oxide on the back of the wafers was causing a charge to build that found the most favorable location on the chuck to arc. Upon removal the system provided a very consistent isotropic etch with a rate of 30 Å/sec. Unfortunately selectivity to resist was only 2:1, however the use of aluminum as a hardmask worked well.

During the release of first lot, the lateral undercutting of devices was observed to self-limit when encroaching etch planes met, leaving a connecting ridge. Figure 3 shows an optical image enhanced by a Nomarski polarizer where the underlying ridge can be seen. This effect was observed to be independent of device area and was present in all form factors.

As it was also seen for all trench widths the effect was determined to be caused by mass transport limitations. A cross section of one of the devices is shown in Fig. 4, where the gap resulting from etched silicon can be seen to decrease towards the center of the device. A small number of devices were released by subjecting them to extremely prolonged etching cycles. These devices were analyzed with the Veeko Wyko NT1100 Optical profiler. An angle of ~10° was determined for the mirrors shown in Fig 5.

Tantalum was also found to be etched by the $XeF_2$ process, compromising the heater elements. The design allowed the sides of the ladder elements to be exposed, and the tantalum was corroded out from under the polyimide pads. The serpentine resistors all failed due to step height opens over the patterned silicon pads.

In the revised process the lateral undercutting of the release etch increased significantly. Device fabricated on unpatterned silicon fully released from only 60 cycles. An optical image is shown in Figure 6 where the sacrificial silicon can be seen to have almost completely removed.

In order to verify device release, SEM images were taken. Figure 7 shows that all single anchor mirrors fully released and stiction was not an issue. Figure 8 is a close up of the mirrors with the largest anchor aspect ratio. These exhibited the largest degree of deflection. In testing the mirrors were visually verified to move. Additional device testing is ongoing.

## VI. Conclusion

A CMOS compatible surface MEMs process using a $XeF_2$ release etch was successfully developed. Thermally actuated micromirrors were fabricated to demonstrate the process. It was determined that during the trench etch, the presence of a backside oxide on the substrates was the cause of arcing events that lead to severe etch rate variability. Lateral undercutting of devices in the $XeF_2$ release etch was observed to self-limit when encroaching etch planes met, and was independent of device area or trench width. Tantalum was also found to be etched by the $XeF_2$ process, compromising the heater elements.

In a revised process, a significantly thicker sacrificial silicon layer was deposited to reduce the effects of mass-transport limitations. To prevent etching of the heater elements devices were created with aluminum heaters, though alternate materials could be implemented with refined process rules. An optical profiler was used to determine the angle of the mirrors. Additional process refinements are still under investigation.

## Acknowledgment

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## References

1. J. Hebding, "Development and Characterization of Low Temperature Thin-Fillm MEMs Structures for Thermal Actuation Applications," Masters Thesis, RIT, Feb '07