Reclaimed Silicon Solar Cells

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Abstract—
Fully processed CMOS Si wafers were reclaimed to make solar cells, while ensuring an acceptable efficiency loss of 15%. This project successfully developed a wafer reclaim process coupled with a solar cell fabrication process. The optimum efficiency obtained was 12.4% using prime wafers and surface texturing, while comparably processed reclaimed wafers were able to achieve 10.5% efficiency.

I. Introduction

Demand for electricity is increasing at an exponential rate, our consumption of coal is harmful to the environment and solar cells seem to be a promising alternative. One key factor for future implementation of solar cells is cost per watt, reclaiming scrapped silicon wafers into solar cells may be a viable option. This project is aimed towards the use of reclaimed silicon wafers for reducing cost while ensuring acceptable efficiencies.

Fully processed CMOS Si wafers were reclaimed to make solar cells. The reclaim process removes 100μm of the top surface by grinding, this was done to ensure all deposited and diffused layers have been removed. After the front grind process, wafers were polished using chemical mechanical polishing (CMP), followed by a clean using wet processes.

II. Theory

A. Wafer Reclaim

Wafers that have undergone CMOS processing may have many deposited layers as well as diffused layers that need to be removed before subsequent processing. 100μm of the top surface ensures the removal of all deposited and diffused layers. The wafers were than polished in order to be of the same surface roughness of prime wafers, this step may be skipped in future work. Once polished, a modified RCA clean was used to ensure the removal of contaminants.

A modified SC2 is used initially to remove metal contaminates. The higher concentration of hydrochloric acid etches off residual metals that may have adhered to the substrate during the wafer grind process. The SC1 bath is used to ensure the removal of organic contaminants, the wafers are then etched in HF to remove the native oxide. Once the native oxide is removed a subsequent metal contaminant clean is utilized to further ensure the removal of metals. Between cleans is an assumed 5min DI water rinse clean undergone at room temperature. Fig. 1 shows the entire clean process.

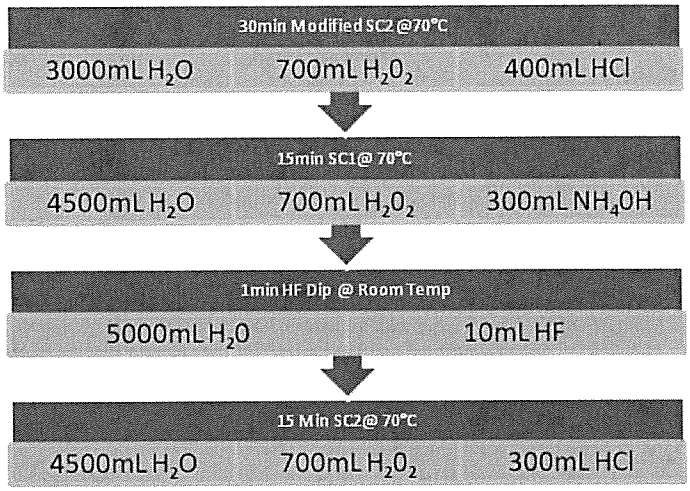

Figure 1 Wafer Cleaning Process

B. Solar Cell

Figure 2 shows a typical solar cell with an n-type emitter on a p-type wafer. An if the hv of the incoming light is greater than the bandgap of silicon, an electron hole pair is generated. A fraction of the generated electron hole pairs are collected by the depletion region and internal electric field. If the carriers are not recombined, they are collected by the metal fingers and grid.

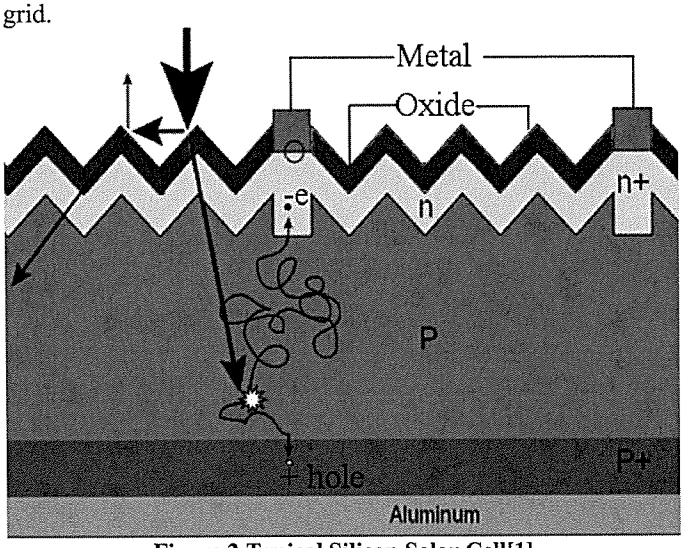

Figure 2 Typical Silicon Solar Cell[1]

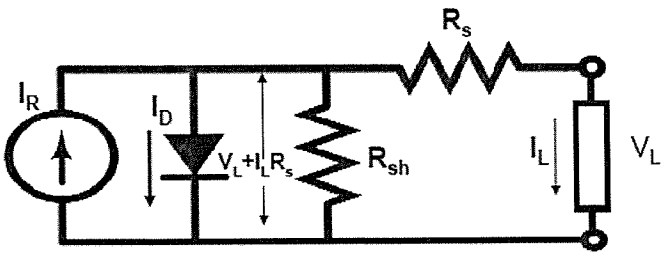

Figure 3 Solar Cell Circuit Diagram

Figure 3 shows a single diode with simulated parasitic series and shunt resistances. To obtain the maximum amount of power from the solar generated current (I_R) to the load, the series resistances should be minimized and the shunt resistance should be maximized. Two key parameters when considering solar cells are the short circuit current and the open circuit voltage, these parameters are highly dependant on series and shunt resistances as shown in equation 1 and equation 2.

$$I_{sc} = I_R - I_0\left[\exp\left(\frac{q}{nkT}(I_{sc}R_s)-1\right)\right] - \frac{I_{sc}R_s}{R_{sh}}$$

Equation 1 Solar cell short circuit current

$$V_{oc} = \frac{nkT}{q}\ln\left[\frac{I_R}{I_0}+1-\frac{V_{oc}}{R_{sh}}\right]$$

Equation 2 Solar cell open circuit voltage

III. Experiments

A. *Experiment I*

The goal of the first experiment was to fabricate working solar cells using different simulated diffusion profiles as well as oxide thicknesses. Table 1 shows all the treatment combinations

TABLE I
SOLAR CELL SIMULATED VALUES

Condition	X_j (nm)	Oxide (nm)	Integrated Dose	Average Doping
900°C for 20min	200	100	4.2E+012	2.1E+17
1000°C for 20min	421	400	4.13E+012	9.2E+16
1100°C for 20min	950	553	4.06E+012	4.3E+16

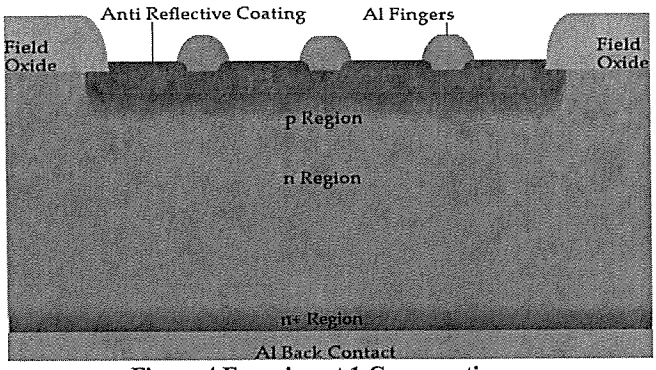

Figure 4 Experiment 1 Cross-section

Figure 4 shows the cross-section of the devices fabricated in experiment 1, the substrate chosen was an n-type wafer with a p-type emitter due to its abundance at RIT. It is ideal to use a p-type substrate with an n-type emitter for enhanced minority carrier mobility and future work can be to do so. The thick field oxide is used as an implant block for the spin on dopant used to diffuse, the n+ region is used as a back surface field to sweep holes back into the depletion region to be collected.

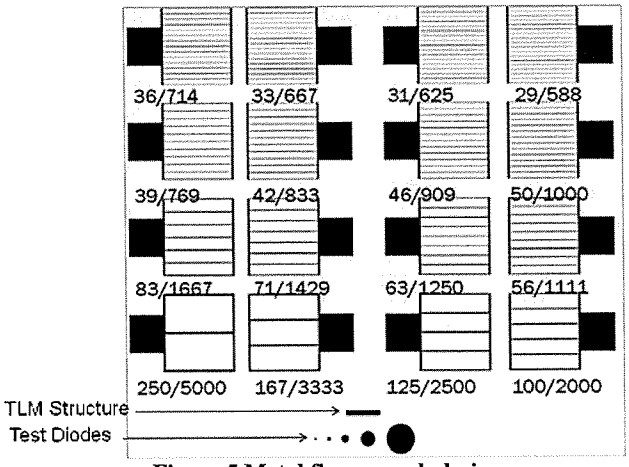

Figure 5 Metal finger mask design

The top metal finger grid design was also varied for all experiments to determine what the optimum spacing between fingers and the optimum metal thickness is. Figure 5 shows this top level metal mask, which also includes TLM structures and test diodes to be able to extract contact resistance and diode idealities. The nomenclature for the mask is line width/ spacing and all numbers are in microns.

B. *Experiment II*

Using the optimum diffusion profile found in experiment 1, fully processed CMOS wafers were reclaimed and were processed into solar cells. Using the tools and process parameters shown in figure 6 coupled with the wet processes shown in figure 1, reclaimed wafers had 100um of their top layer removed were chemical-mechanically polished and then wet cleaned.

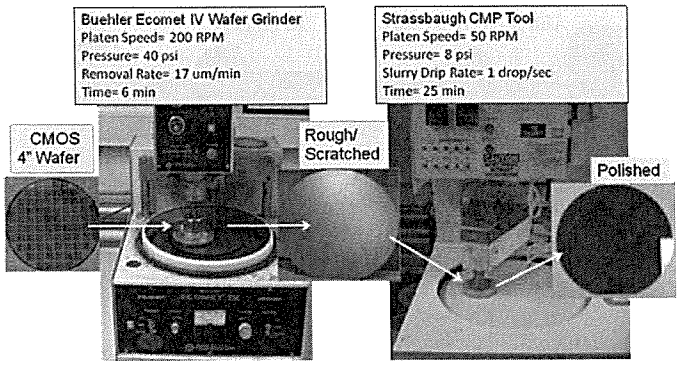

Figure 6 Wafer reclaim process

C. *Experiment III*

Experiment III's goal was to increase efficiency by increasing the surface area of the solar cell and also attempting to reduce reflection loss. This was done by surface texturing as seen in figure 7.

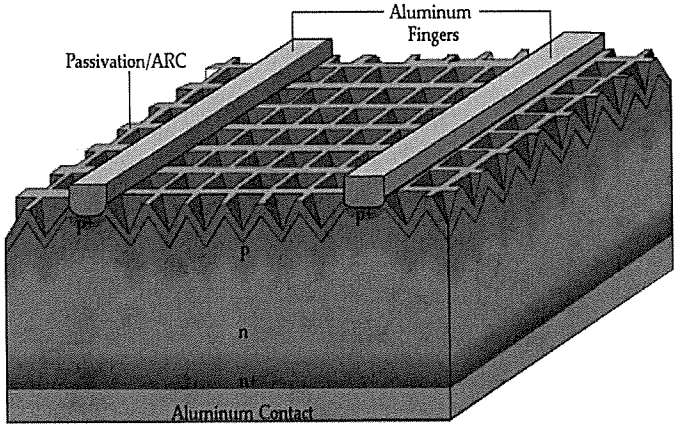

Figure 7 Cross-section of modified PERL design[1]

Inverted pyramids by KOH etching in the configuration shown in figure 7 were achieved as well as top and back surface fields for enhanced carrier collection.

IV. Results

A. *Experiment I*

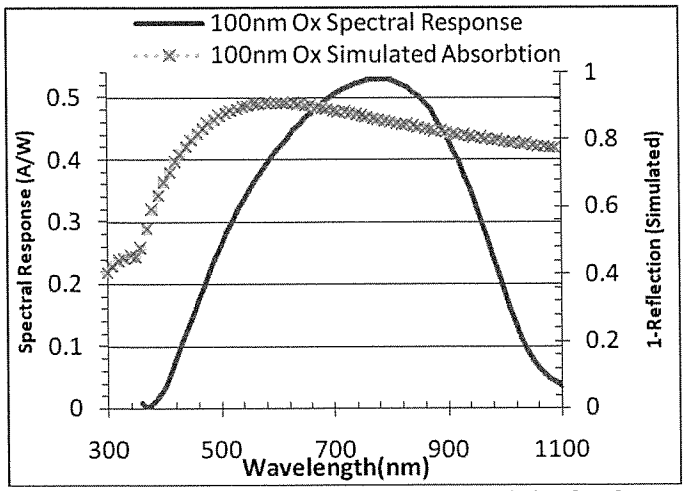

Figure 8 100nm Oxide spectral response and simulated absorption

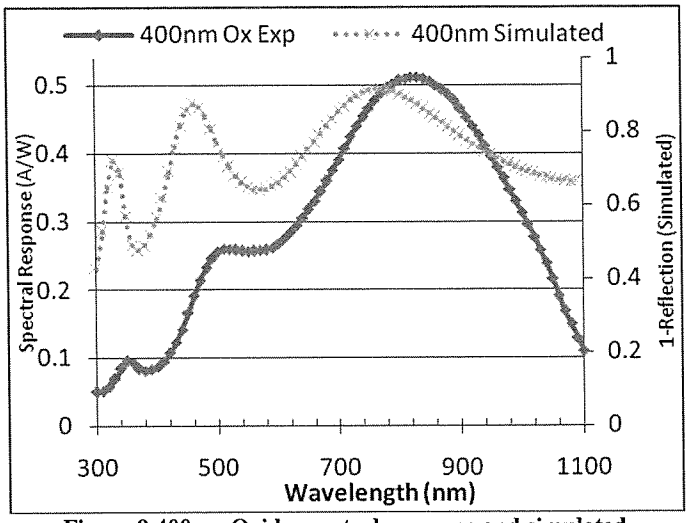

Figure 9 400nm Oxide spectral response and simulated absorption

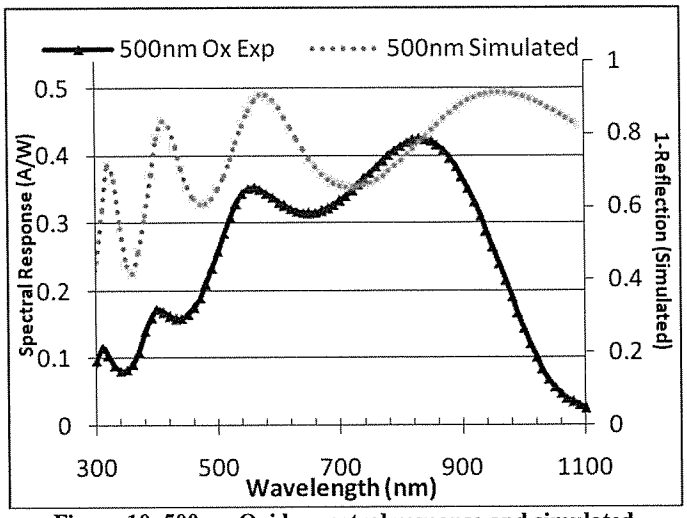

Figure 10 500nm Oxide spectral response and simulated absorption

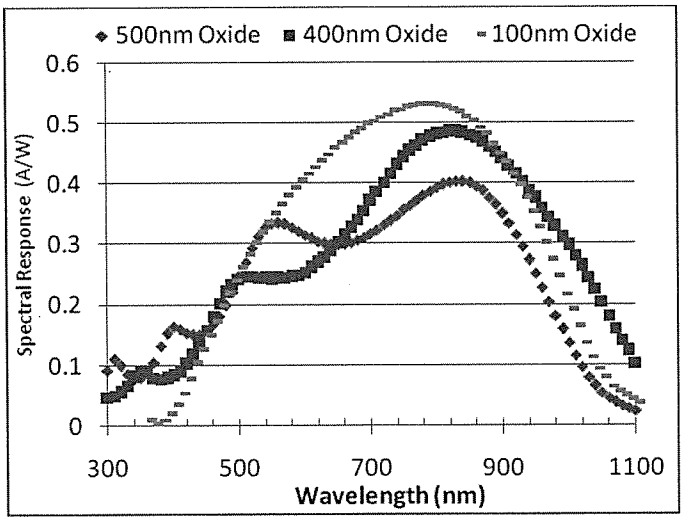

Figure 11 Experiment 1 Spectral Response

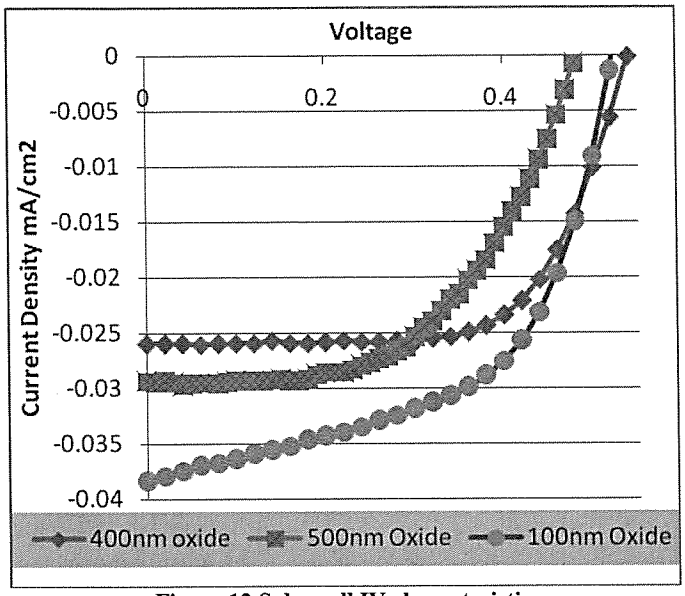

Figure 12 Solar cell IV characteristic

B. Experiment II

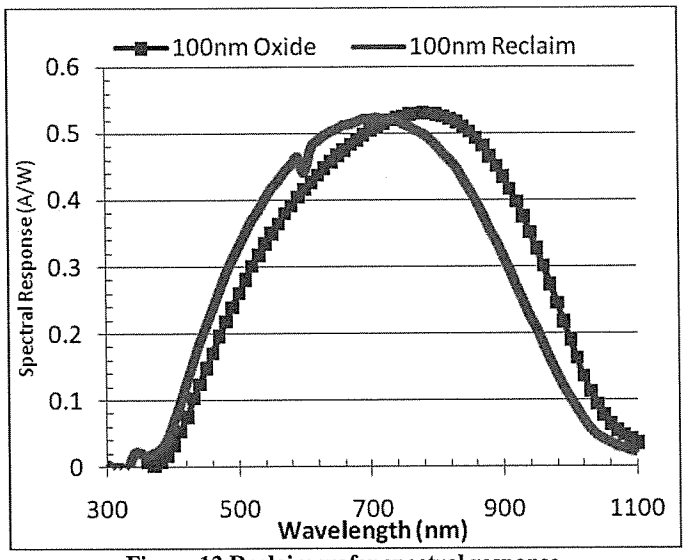

Figure 13 Reclaim wafer spectral response

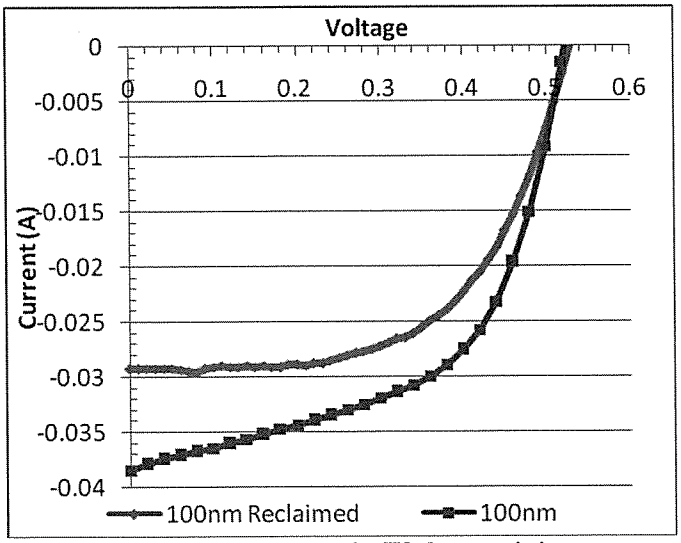

Figure 14 Reclaim wafer IV characteristic

C. Experiment III

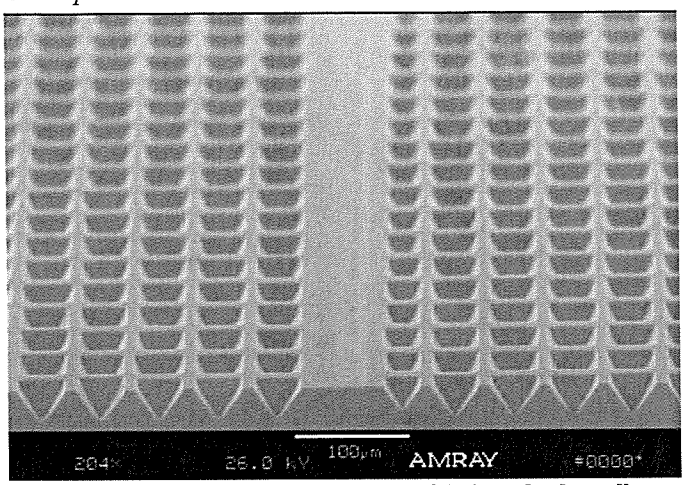

Figure 15A SEM image of textured fabricated solar cell

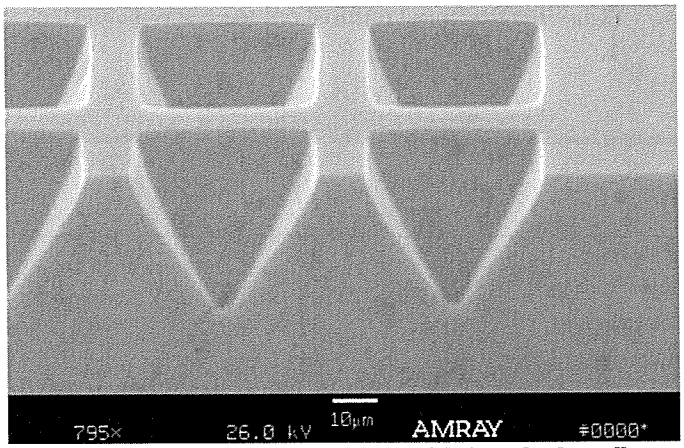

Figure 15B SEM image of textured fabricated solar cell

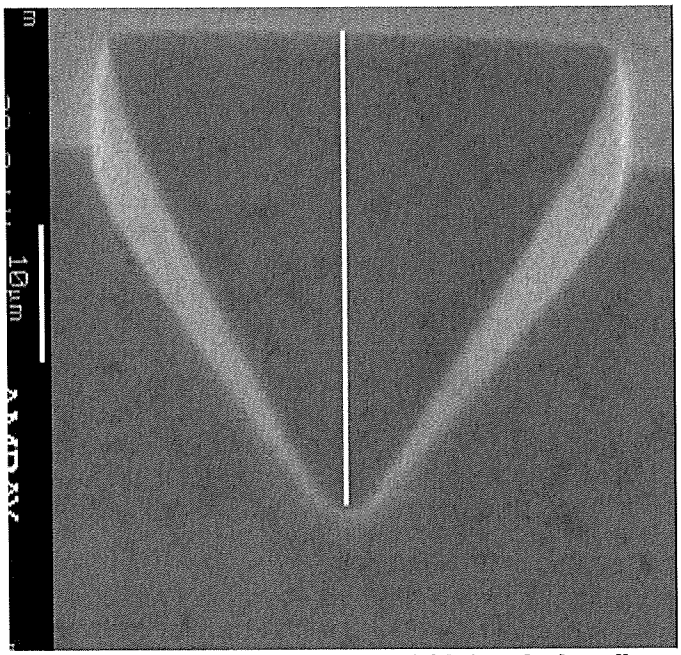

Figure 15C SEM image of textured fabricated solar cell

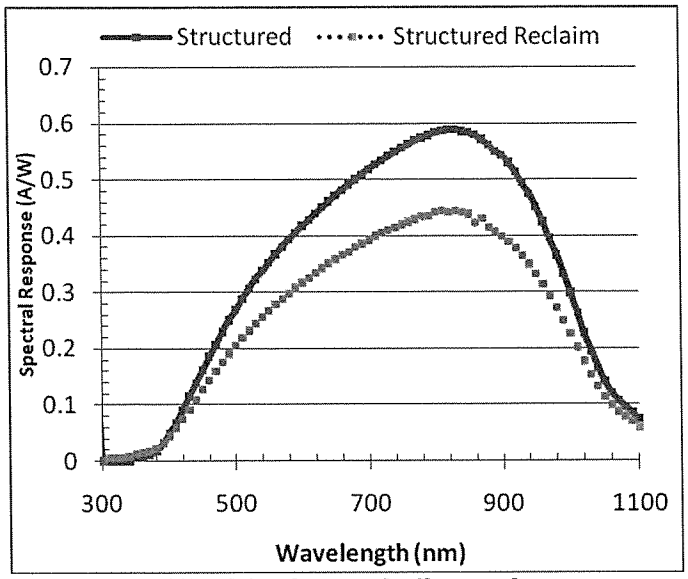

Figure 166 Reclaimed textured cell spectral response

TABLE 2
SOLAR CELL RESULTS

	Jsc (mA/cm^2)	Voc (V)	Fill Factor (%)	η (%)
500nm Oxide	29.4	.48	54	7.7
400nm Oxide	25.6	.55	66	9.2
100nm Oxide	38	.52	55	11.1
100nm Ox. Reclaim	25.9	.47	64	7.8
Surface Texturing	39.8	.38	67	12.4
Surface Text. Reclaim	29.6	.53	67	10.5

V. Discussion

Figures 8-10 show the spectral response plotted with the simulated absorption. Figure 8 shows the 100nm oxide device performance not being hindered by its reflection loss, where as the other figures 9 and 10 show significant device performance decreases at the reflection peaks or the absorption valleys. These were proof of concept measurements to accurately indicate that reflection was truly hindering the performance of the device and using an optimum oxide thickness increases device performance. This conclusion is clearly shown in figure 11 where the spectral response of all three devices are plotted together. It shows that the 100nm oxide has the best device performance, which is also reflected in figure 12's current-voltage characteristic. The 100nm device generates more current as expected from its spectral response.

Experiment II's results are shown in figures 13 and 14, where it could be shown that the reclaim wafer has a shifted spectral response and does not perform as well as the prime wafer. At 600nm the reclaim wafer has a decrease in response as shown in figure 13, this may be attributed to gettered sites in the CMOS process the reclaim wafers had undergone previously. In future work, it is possible to cleave the reclaim wafer and wet etch the gettered sites preferentially and under a scanning electron microscope it will be easy to see where the gettered sites are located. As expected the generated current for the reclaim wafers is not as high as the current generated by the prime wafers. This is can be attributed to a lower carrier lifetime, the carriers are being recombined before they are collected by the metal finger scheme.

Figure 15A-C show the fabricated textured cell's cross-section which is similar to the simulated desired cross-section shown in figure 7. The pyramid mask design was 30μmX30μm squares, but after undercutting they were fabricated at 37.5μmX37.5μm squares as shown in the scanning electron microscope pictures. This increased the surface area of the device by 50%, although the irradiance through the increased surface area is constant. Another advantage of the inverted pyramid design is its decrease in reflection as shown in figure 2. A measurement that can be taken as future work is scatterometry measurements, by shinning light incident to the sample and collecting reflected light at various angles, an experimental reflection value can be obtained by adding all of the individual angle's reflection measurement. Figure 16 shows the reclaim wafer performance as compared to a prime wafers performance, and as expected the reclaim wafer has a decrease in spectral response as shown in table 2 as well.

VI. Conclusion

The goal of developing a process to reclaim wafers into solar cells has successfully completed. An acceptable efficiency loss of 15% has been demonstrated comparing prime and reclaimed silicon as shown in table 2. This experiment has shown that using reclaimed silicon can be a viable option to meet the future electricity demands.

Acknowledgment

The author would like to acknowledge all of those who have helped along the way, including, but not limited to SMFL, NPRL and μE. If it weren't for the people around us, we would be nothing.

References

[1] N. Savage. (1999, December). Photovoltaics: Small and efficient wins the race *Laser Focus World* [Online] Available: http://www.laserfocusworld.com/ARTICLES/54408