

Integrated Thin Film Crystalline Silicon Photoactive Components

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Abstract—Single crystal silicon photoactive devices using a low-temperature thin-film transistor (TFT) compatible process were designed and manufactured on bulk silicon and silicon-on-insulator (SOI) substrates at the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT. Photodiodes and phototransistors designed with transparent indium-tin oxide (ITO) gates, along with n-type and p-type ITO Schottky test devices were manufactured and investigated. Possible applications for devices investigated here include on-display photodetectors, on-display digital logic and possible integration into touchscreen or lightpen sensitive liquid crystal TFT displays.

The photoactive devices were integrated in active pixel sensor (APS) arrangements to determine feasibility of integration into large-field SOI or Silicon on Glass (SiOG) applications. Currently most APS sensors fabricated using standard bulk silicon processes are incompatible with TFT processing due to temperature constraints; standard TFT processing does not exceed $\sim 660^\circ\text{C}$. Device sizes were varied in order to quantify sensitivity due to junction size. Elements of the APS circuit were scaled to enable the acquisition of a transient response.

Index Terms—Active pixel sensor, photodiode, silicon-on-insulator, silicon-on-Glass.

I. INTRODUCTION

CLASSICALLY, Thin-film transistors have been built using amorphous silicon on glass substrates. This has provided working devices with the lowest cost for the display industry. The performance of these TFT devices is inferior to crystalline silicon, in that carrier mobility in amorphous silicon is two orders of magnitude lower. This paper will attempt to demonstrate the advantages of crystalline silicon over amorphous silicon using TFTs, and will also provide an overview of a manufacturable process for TFTs on crystalline silicon using SOI or SiOG.

Recently, a step has been made by certain corporations (e.g. Corning, Inc.) to produce a new substrate which incorporates crystalline silicon with glass. This process, when it meets fruition may provide near-SOI quality semiconductor on a large glass substrate. This would facilitate the manufacture of

not only higher quality flat panel displays, but also allow for integration of amplifiers and digital logic on the display itself, where currently these devices are integrated off-display, linked by wirebond. Using the process outlined in this paper it is possible to obtain working CMOS logic on glass, using a TFT compatible process.

Photoactive devices will be investigated, along with silicon photodiodes, in an APS arrangement. ITO gate transistors and photodiodes were integrated on the same design. Much like standard TFTs, photoactive devices benefit greatly from a move to crystalline silicon. Photoresponse should scale with the differences in carrier mobility, providing the ability to not only have a display, but to also have a detector on the same piece of glass. However there is an inherent tradeoff in junction area if the device region is confined within a thin-film crystalline silicon layer.

II. DEVICE DESIGN

Standard TFTs and photodiodes were constructed using a molybdenum gate, self-aligned process with aluminum as the metal on both SOI and bulk.

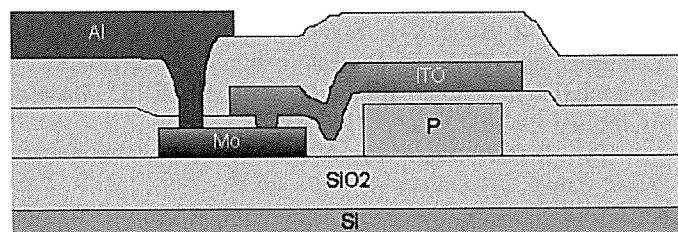


Fig. 1. Cross-sectional diagram of ITO gated phototransistor. ITO is contacted to a Mo bridge and Al is contacted to Mo. Done to prevent HF contact with ITO, the results of which are uncharacterized.

Fig. 1. shows a representative ITO gate phototransistor. The ITO gate phototransistors were constructed with a non-self-aligned process, and contacted to metal via a molybdenum bridge. This design alleviates the need for an HF contact cut through silicon dioxide down to ITO, and instead cuts down to molybdenum; the interaction between HF and Mo is better characterized than that of HF and ITO, and this was done to remove uncertainty from the process.

Other than acting as a transparent, conductive gate, the ITO layer was utilized to investigate phototransistor and possible Schottky effects due to workfunction difference when contacted directly to silicon.

Silicon photodiodes investigated were of the P-I-N variety,

Manuscript received May 20, 2008. This work was supported by the Department of Microelectronic Engineering, Rochester Institute of Technology

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with a 12-micron long junction length. Widths of the photodiodes were varied to examine photocurrent response to junction size. The lengths investigated were 116 μm , 216 μm , 280 μm , 344 μm and 408 μm .

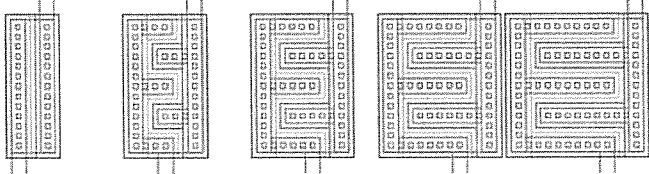


Fig. 2. Layouts of 5 photodiode sizes investigated in this paper, increasing in size from left to right, these devices have junction widths of 116, 216, 280, 344 and 408 μm .

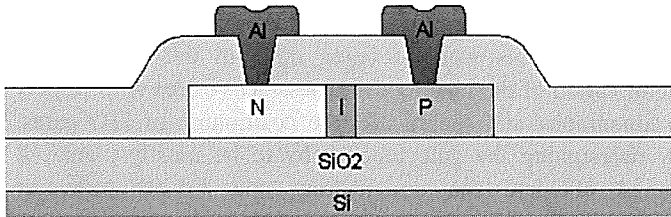


Fig. 3. Cross-sectional diagram of P-I-N photodiode. Photoactive area is centered around the intrinsic silicon (lightly doped p-body) between the two Al contacts.

Fig. 2. shows a layout design of the photodiodes and their various sizes. The interdigitated junction widths are a more important factor than the lengths or depths of the devices, as the substrate limits junction depth, while the junction length should be as short as design rules allow.

Electron-hole pairs (EHPs) are generated by photons absorbed in the junction area of the diode, and they are swept away by the built-in voltage across the junction, in the case of a photovoltaic or solar cell, or by a reverse bias across the junction, in the case of a photodiode. Once the e^- or h^+ reaches the doped region, it acts as a charge carrier, and its presence will disrupt equilibrium and the junction will generate more EHPs to re-equilibrate. The junction must be suitably short for both design rules and for carrier lifetimes – if the junction is too long, the newly generated e^- or h^+ will recombine before it reaches the doped region of the diode, and will not cause create photocurrent.

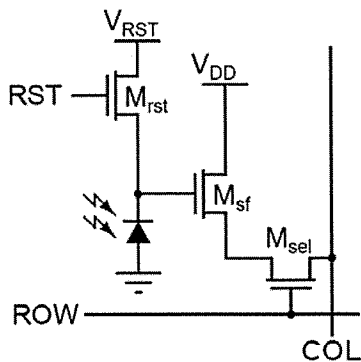


Fig.4. Schematic of active pixel sensor circuit. Photodiodes or phototransistors can take the place of the photodiode in the schematic.

Figure 4 shows the generic schematic of an active pixel

sensor circuit. The photoactive components were integrated as part of an APS circuit[2]. The APS circuit is comprised of 4 or more transistors arranged to provide clocked output for digital imaging applications. These are most commonly utilized in modern digital cameras and some forms of medical diagnostic digital imaging.

In order to utilize an APS circuit[1], proper timing and clocking must be implemented. Before the photoactive device can be used, a voltage must be set, or more correctly, a charge accumulated on the gate of M_{sf} ; this is done by turning the RST signal high, causing M_{rst} to turn on. To read out, RST goes low, turning off M_{rst} , and the charge accumulated on M_{sf} is dissipated by the photoactive component. The charge on the gate of M_{sf} will determine the conductance of the transistor, and the amount of current passing through the readout rail, or the voltage drop over M_{sf} and M_{sel} is utilized by the readout circuit. The current or voltage is read off the COL, and the ROW signal going high will cause the pixel to be read.

Due to the importance of the capacitance of the integration node M_{sf} , its sizes were varied as part of the design. In order to obtain a transient response as opposed to a high-speed clocked response from the APS, the integration node must be made very large. M_{sf} sizes were designed as 12x4, 100x100 and 320x320 micron.

Lightblock was added to prevent stray light from affecting the performance of the non-photoactive transistors in the active pixel sensor array. It is a metal layer over a passivating ILD. It is not present over photoactive devices and testpads.

III. DEVICE FABRICATION

Processing was done on 100mm bulk p-type wafers and n-type SOI wafers. Only Bulk NMOS will function without VT adjust implant. NMOS and PMOS will function on SOI.

A ten level mask set was designed for use on quad reticles (4 layers per plate) with a 5x reduction stepper. Normal TFT processing only uses six lithography levels, however this process included two non-standard layers, ITO and Lightblock metal. All lithography was done using an SVG 100mm coat and develop track, and a GCA 6700 g-line 5x reduction stepper. Exposure was found to be optimal at 1.9 seconds with a focus setting of 100. HPR 504-10 resist was used with CD-26 as a developer.

Deposition of layers was done in a myriad of tools. Low pressure Chemical vapor deposition of oxide was done in an ASM 150mm LPCVD system, using a 425C LTO recipe. Molybdenum was deposited using a CVC 601 sputter tool. ITO was also sputtered using the same tool, using the following parameters: 180W pulsed DC, 1600ns pulse width at 250KHz, sputter at 5mT with a 10-20 minute pre-sputter. A 1-hour sputter yielded approximately 2400 angstroms of ITO, or approximately 40 angstroms per minute. The resulting film was translucent and conductive, measuring 180 ohms/square.

Ion implantation was done in a Varian 350D Implanter. Four implants were done, backside 2E15 boron at 35KeV,

4E15 phosphorus at 110KeV, 3E15 fluorine pre-amorphization at 60KeV, and 4E15 boron at 35KeV.

Etching processes were done using a LAM490 silicon plasma etcher, along with a Drytek Quad which dry-etched molybdenum. A specialized wet etchant, formulated 10:10:1, water : hydrochloric acid : nitric acid was used for ITO. This etchant was noted to be extremely sensitive to temperature and etch rate repeatability was only obtainable at 17-20°C.

IV. DISCUSSION

Fabrication of devices is still being investigated. The patterned ITO gates and other ITO devices suffered undercutting during etch and are non-working.

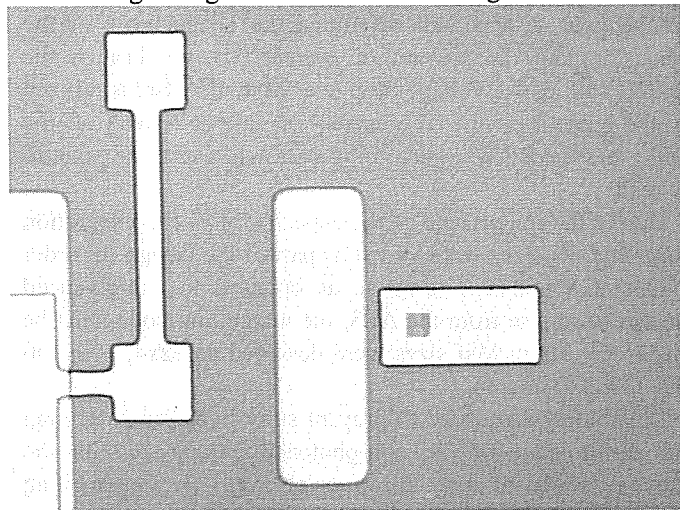


Fig.5. Optical micrograph of ITO gate device. ITO is present on the wafer, as can be seen in the ITO contact cut.

Fig.5. is an image of a representative device with ITO deposited before lithography. Directly after this step, a lithographic pattern was applied to form a gate. When that gate was wet etched, the ITO began to lift-off and undercut along major lines of topography.

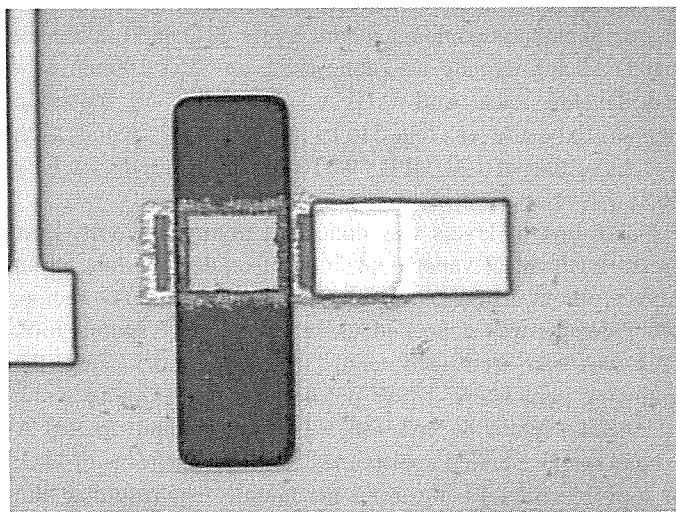


Fig.6. Optical micrograph of ITO gate device. ITO undercutting and lift-off is visible

Fig.6. shows the result of a wet etch on an ITO gate device. The speckling and rough appearance are indicative of liftoff and undercutting. Undercutting this severe will result in open-circuits and therefore lead to non-working transistors.

The silicon mesa etch done on the SOI wafers early in the process suffered a non-uniformity problem and this was not discovered until later processing. At that point it was impossible to correct the mesa etch problem, so the fabrication of devices was continued despite the non-uniformity which may short some mesas on the SOI device wafers.

V. CONTINUING INVESTIGATION

Work is being done to engineer solutions to the undercutting observed when wet-etching ITO over major topography. This work is being done in the design of a modification of the layout of the mesa/active area with respect to topography and specifically the positioning of ITO gates. By redesigning the gate topography to be mostly planar, it should alleviate the undercutting and lift-off problems observed.

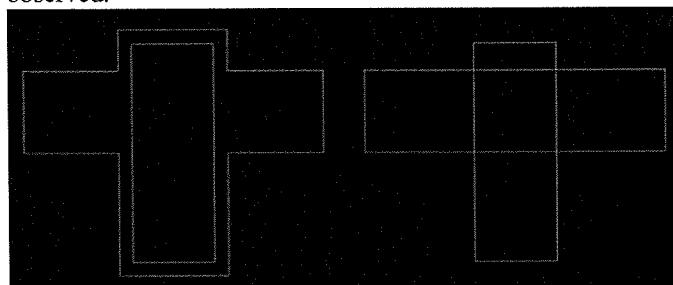


Fig.7. Diagram of proposed layout design change to combat ITO undercutting along topography.

Fig.7. shows a proposed change in the layout of the active mesa which may solve the problem of undercutting. The device on the right is the current design which is in manufacturing. The ITO (the vertical part of "T") intersects with the edges of the active (the horizontal part of the "T"). In the device on the right is the changed layout, with the ITO completely surrounded by mesa on all sides with an overlap. While not an elegant solution it is a possibility.

Another possibility is the use of a dry-etch process incorporating methane or halogens. Both of these are, however, covered under intellectual property of several organizations and also pose very real risks of contamination of the chamber, along with hazardous byproducts.

Fabrication also continues on devices which suffered the ITO problems. The photodiodes and active pixel sensor devices remain unaffected and may prove functional.

VI. CONCLUSION

A process for manufacturing crystalline silicon TFTs on SOI and glass was investigated. Setbacks due to ITO wet etch problems were encountered. Solutions for correcting the problems are being engineered and fabrication continues with electrical results forthcoming.

ACKNOWLEDGMENT

I.J.Onigman would like to thank Dr. Karl Hirschman, Dr. Sean Rommel, Ms. Patricia Meller, Mr. Christopher Shea and the staff of the Semiconductor and Microsystems Fabrication Laboratory.

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