Germanium Esaki Diodes by N-type In-Situ Doping

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Abstract—**A rapid melt growth process is performed in the formation of Esaki tunnel junctions on in-situ n-doped germanium on silicon substrates. An aluminum-silicon alloy is used as the p-dopant for the junctions as well as an ohmic contact for testing. The rapid thermal anneal (RTA), used for the incorporation of the aluminum-silicon, is characterized by varying ramp rate and peak anneal temperatures. It is found that peak anneal temperature is the dominant factor affecting the current density through the devices. The maximum current density recorded is 2098mA/cm^2 at a peak anneal temperature of 620°C.**

Index Terms—**alloy, in-situ doping, rapid thermal anneal (RTA), tunnel junction**

I. Introduction

RECENT interest has been taken in the area of germanium technologies specifically for its high current density tunneling capabilities. These properties are essential for the fabrication of low-power dissipation field-effect tunneling transistors[1] as well as combining tunnel diodes with transistors in low-power circuits.[2] The ITRS currently lists the tunnel transistor as an emerging research device to be used as an alternative to MOSFETS.[3]

To create the Esaki tunneling effect, degenerately doped abrupt p and n junctions must be formed to maximize direct interband tunneling. A rapid melt growth process has recently been demonstrated by Zhao et al. at the University of Notre Dame for the realization germanium tunnel junctions.[4] This process uses an RTA step to heat the devices above the eutectic temperature of Al-Ge. During the ramp up the aluminum and germanium react allowing aluminum donor atoms to incorporate into the germanium substrate. Upon cooling the germanium re-crystallizes forming the degenerately doped p-junction.

Aluminum has the highest solid solubility as a p-type dopant in germanium with concentrations possible to about 2x10^{20}cm^{-3}.[5] Figure 1 shows the phase diagram for Al-Ge. The eutectic temperature of Al-Ge is T_E=420°C. Peak anneal temperatures above this value should theoretically result in 51.6% weight percent germanium or greater.

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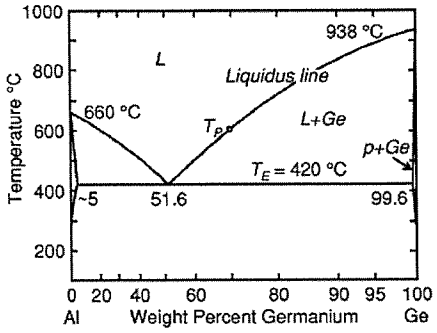

Fig. 1. Al-Ge phase diagram[6]. In the rapid melt growth process, the devices are heated above the eutectic temperature of 420C to allow for the reaction of the aluminum and germanium. This process forms the degenerately doped p-junction.

II. Approach

A. Simulations

To build the devices an n-type in-situ doped germanium on silicon substrate was used. The substrate had a known doping of 1x10^{19}cm^{-3}. Using a rapid melt growth process the maximum doping concentration theoretically should be around 1x10^{20}cm^{-3}. Band gap simulations using Silvaco Atlas show the Fermi Level on the n-side at or slightly below the conduction band edge. Based on this information it was expected that the devices would have large depletion regions and act similar to a backwards diode. Negative differential resistance (NDR) is not likely since the n-type doping concentration is not high enough.

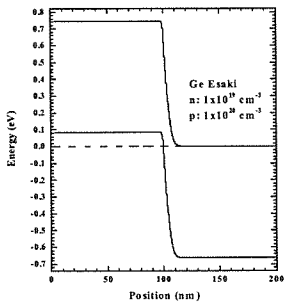

Fig. 2. Silvaco Atlas band diagram simulation of device using expected doping concentrations. Devices were expected to operate similar to a backwards diode. NDR not expected due to the lower concentration of n-type dopant atoms.

B. Process

This process was adapted from an existing process at Rochester Institute of Technology to create tunnel junctions. Fig. 3 outlines the steps in the original process and the new

process used in this study. The original process used a spin-on-glass (SOG) dopant source to dope the substrate. Since the substrates were already uniformly highly doped, this step was omitted. The substrates were patterned using contact photolithography with a LOR layer for use in a later lift-off process. The aluminum was DC sputter deposited on the patterned substrate. Substrates were then placed in a heated bath of Nanoremover PG to complete the lift-off process. The lift-off process was also a modification to the original process. The original process used a wet aluminum etch bath to pattern the aluminum, but it was found that the aluminum etch bath was attacking the germanium and an alternate method to pattern the aluminum was preferred.

Step	Old Process	New Process
1	SOG	Lithography using LOR and Resist
2	DC Sputter Aluminum Deposition	DC Sputter Aluminum Deposition
3	Lithography	Lift-off in Nanoremover PG
4	Wet aluminum etch	Alloy
5	Resist strip	
6	Alloy	

Fig. 3. Old Process vs. New Process. This table outlines the changes made to the existing process at the Rochester Institute of Technology to form tunnel junctions in germanium.

Fig. 4 shows a representative cross section of the finished device. After the RTA process a p-type doped region is formed just below the patterned aluminum.

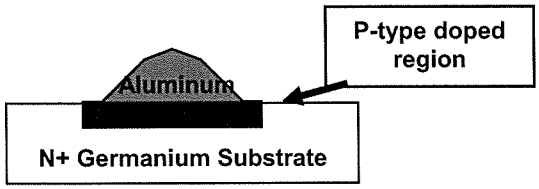

Fig. 4. Cross section of diode. This is a representative cross section of a tunnel junction after the anneal process.

III. P-Doping Experiment

Although the substrates were not doped sufficiently to cause NDR, the factors of the RTA process to form the p-junction could be isolated because of the uniform substrate doping. Both ramp rate and peak anneal temperature were varied to characterize the anneal process. Ramp rates varied from 50°C/s to 150°C/s and peak anneal temperatures ranged from 550°C to 820°C. Fig. 5 shows the current voltage characteristics from this experiment. All data shown has a ramp rate of 100°C/s since this value showed the most consistent results and showed the most prominent inflection points. The current density had an obvious response to the peak anneal temperature.

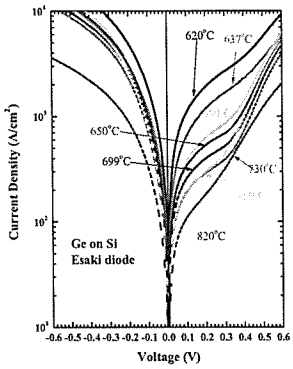

Fig. 5. Current voltage characteristics for devices using 100°C/s ramp rate at several peak anneal temperatures.

Fig. 6 shows how the current density of the devices responded to the peak anneal temperatures. There is an obvious decreasing exponential trend as the temperature increases. The hotter temperatures of the anneal process allowed the reaction between the aluminum and the germanium to take place for a longer period of time. Since the reaction takes place horizontally as well as vertically, the resulting junction had a less abrupt doping profile. This inhibited the tunneling current through the devices greatly limiting the current density at higher temperatures.

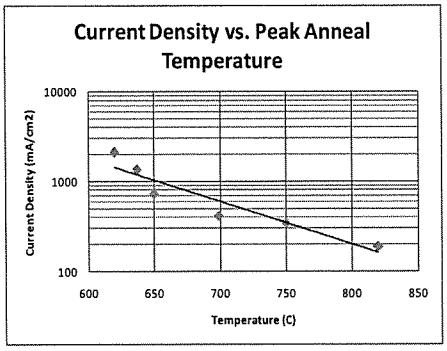

Fig. 6. Current density vs. peak anneal temperature trend. As the temperature of the anneal increased the current density decreased. Higher temperatures allowed the germanium and aluminum to react for a longer period of time. This resulted in less abrupt junctions inhibiting tunneling current through the device.

Fig. 7 shows the surface morphology of two separate samples after the anneal process. The image on the left shows a sample with a peak anneal temperature of 620°C. The reaction between the aluminum and the germanium was mostly confined to the areas right below the metal lines. The image on the right is a sample with a peak anneal temperature of 720°C. The reaction in this case has spread well beyond the metal lines and could actually be shorting out adjacent devices.

Ideality factor also showed a strong response to peak anneal temperature. Ideality factor vs. peak anneal temperature is shown in Fig. 8. At temperatures above 720°C and below 650°C there is an obvious degradation in device performance. Devices with peak anneal temperatures between these temperatures showed similar results with the 700°C anneal

temperature showing the best ideality factor at 1.39. Devices using lower peak anneal temperatures probably did not see enough of a reaction between the aluminum and germanium, while the hotter temperatures could not contain the reaction. Both of these factors could contribute to the degradation in performance.

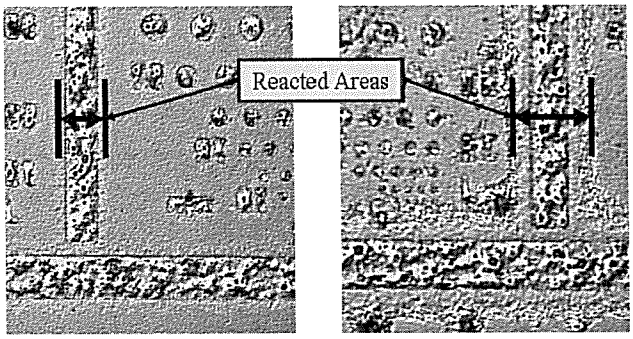

Fig. 7. Surface morphology of a sample annealed at 620°C (left) and a sample annealed at 720°C. The hotter temperatures allowed for a longer time for the reaction to take place resulting in the junction spreading well beyond the aluminum lines.

CONCLUSIONS

This study has shown that peak anneal temperature is the dominant factor affecting device performance of germanium Esaki diodes. Although dopant concentrations in the substrate were not high enough to promote enough direct tunneling to cause negative differential resistance, these same findings can be applied to other substrates to optimize tunnel junction devices. Lower peak anneal temperatures showed the highest current densities, but the ideality factor was degraded. Best device performance was seen using a peak anneal temperature between 650°C and 700°C.

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