Process Development for the Fabrication of a Double-Sided Photodiode

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Abstract—**Given a cross-section and functionality requirements for a photodiode designed for application as the focal plane array on SNAP (SuperNova Acceleration Probe), a proposed satellite in the Joint Dark Energy Mission by NASA and the DOE, a process has been developed to fabricate the device in the most efficient and reliable manner. The photodector is to be hybridized with a ROIC (Read-Out Integrated Circuit) that interprets the individual pixel signals and converts the electrical information into an image. After several versions of the process based on simulations, efficiency of sequence, and research, a test run of key process steps was completed to evaluate chosen process values and their final results, including well profile and I-V characteristics. The results from the test run were used to create a preliminary process flow for device wafer fabrication. The process was implemented in full on a small lot of device wafers with some monitor wafers, with the entire process (not including test) requiring about 100 hours. The results from this device run were used to create a new revised version of the process flow in order to attain better functionality from the device. After this device run was completed, the results were analyzed and used to update the process flow again to address deficiencies in the resulting devices and processing difficulties.**

Index Terms—**Photodetector, ROIC, Dark Current, Diode Ideality**

I. Introduction

SNAP (SuperNova Acceleration Probe) is a deep space observatory that will measure the expansion of the universe by tracking supernova as markers. This information will also help scientists understand the nature of dark matter and its role in the acceleration of the expansion of the universe. It is a part of the Joint Dark Energy Mission (JDEM), included in the Beyond Einstein program: an initiative by the scientific community to better understand the universe. The photodetector described here will act as the focal plane array for this observatory in its final revision. Fig. 1 above shows a final cross-section of the device. The bump bonding sites will be the point of communication between the detector pixels and the ROIC circuit. The backside of the wafer has a metal frame to introduce a bias across the whole wafer via a heavily doped region of silicon. Fig. 2 shows the top-down views for both the front and back of the wafer. There is a metal grid that runs between the pixels which will act as a field effect gate to decrease cross-talk between the pixels by creating a slightly N-type accumulation. The design of the device stipulated that there was to be minimal shadowing (which implies that the metal layer must be tightly controlled), the implant well junctions were to be less than a micron each (more specifically, less than 0.75μm for the n-well and less than 0.5μm for the p-well), and the pixel pitch was 15μm. The surface concentration of the wells was to be also aggressively high to make a good ohmic contact between the silicon and the aluminum: $1x10^{18}cm^{-3}$ for the N+ implant and $1x10^{19}cm^{-3}$ for the P+ implant. The goal for the dark current (the limiting factor in the resolution of the resulting image) was $0.1^{pA}/_{cm^2}$ at the operating conditions for the device (200K at a 50V reverse bias), which translates to $15^{nA}/_{cm^2}$ at the testing conditions of 300K with the same bias.

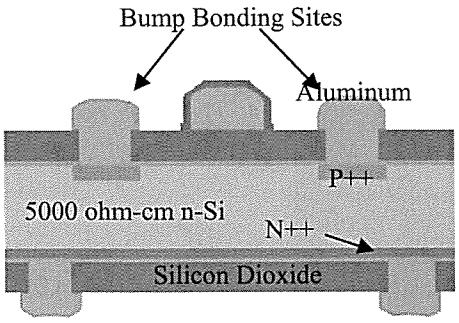

Fig. 1. Cross-Sectional View of the final device

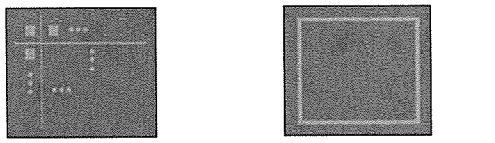

Fig. 2. Top-Down View of the final device (front and back)

II. Challenges and Solutions

A. *"Backside" Contamination*

In normal CMOS fabrication, the devices are made on only one side of the wafer, and while the backside of the wafer is exposed to contaminants and vulnerable to scratching, this is generally ignored (and perhaps encouraged to aid in gettering). For the fabrication of this device, however, the backside must be as device-ready as the front side. To make sure that both sides of the wafer remain pristine as possible, protective coatings, proximity bakes, and careful sequencing were used so that neither side the wafer was ever subjected to the contamination usually seen by a standard CMOS process wafer.

B. Limited Thermal Budget

Due to the need for shallow junctions (to decrease surface recombination velocity, a parasitic that decreases the signal to noise ratio in a photodiode), little to no diffusion of the implanted species could occur. Since this diffusion occurs at high temperature (like temperatures seen during thermal oxide growth steps), these high temperature steps were eliminated as much as possible. Since the final device requires an anti-reflective layer (silicon dioxide) 5000Å thick, the decision was made to use LTO for the majority of the film thickness, but still grow 100Å of thermal oxide for a good interface between the oxide and the silicon. These oxide growths also served to activate the implanted species since they occur after each implant step in the process flow. Rapid thermal anneals were also done after the implants to anneal out damage due to implant.

C. Front to Back Alignment

Double-sided alignment is a challenge at RIT due to the availability of tools only designed for single-sided alignment. A process needed to be found that would facilitate the alignment of the front die and the back die to within a reasonable shift. Alignment was done by first aligning the side that would not be exposed to a mask, then affixing the wafer to the mask by using water droplets to create adhesion. The wafer and mask were then flipped, and the second mask was aligned to the first mask by use of marks outside the design area and the backside of the wafer was exposed, now aligned to the front side[1].

D. Selectivity / Over-Etching

Because the implanted wells are so shallow, selectivity and over-etching became an issue. Dry etching is more anisotropic, which leads to better contact etching, but has poorer selectivity, meaning that the etching gases will not stop on the desired layer. Instead, they will continue into the silicon layer after etching the oxide layer and consume the highest doped portion (the surface) of the doped well. End point detection can be used to gauge the transition from oxide to silicon by monitoring the spectra emitted in the chamber, but slight over-etching would result in dopant loss and poorer contacts, which result in more parasitic resistance and poorer device performance. For these reasons, wet etches, though isotropic in nature, were chosen for their selectivity (ratio of more than 500:1) and therefore reliability.

III. Simulations

Once a preliminary process flow had been completed, simulations were done using Silvaco Athena to ensure that assumptions that were made incurred good results (as per the goals listed previously). The entire process was simulated save for the passive steps (such as RCA cleans) and then the final well profiles were analyzed to determine the defining characteristics. Fig. 3 shows the front and back-side well profiles (P+ and N+, respectively).

[1] http://people.rit.edu/lffeee/backside%20alignment.pdf

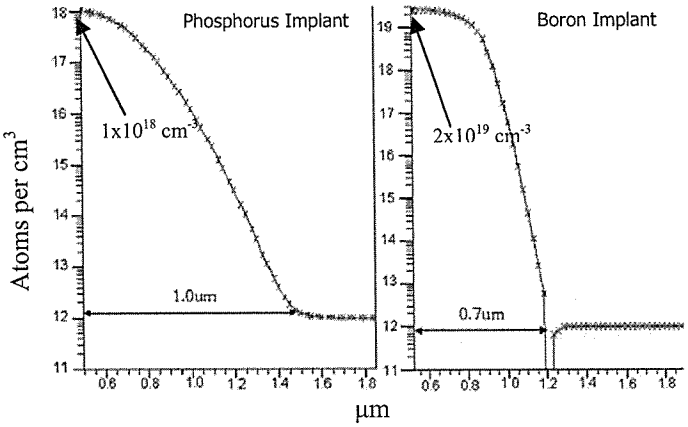

Fig. 3. Well Profiles from Silvaco Athena after Full Process Simulation

As seen in the figure, the surface concentrations are correctly obtained, but the junction depths are about 0.25µm too deep. Since all of the thermal steps had already been reduced and the P+ implant species changed from B_{11} to BF_2 (for shallower initial junction), these values were deemed acceptable and the project moved forward, knowing that the goals were aggressive to begin with. Should the simulations prove correct at the end of fabrication, more steps would be taken to decrease them.

IV. Testing Run

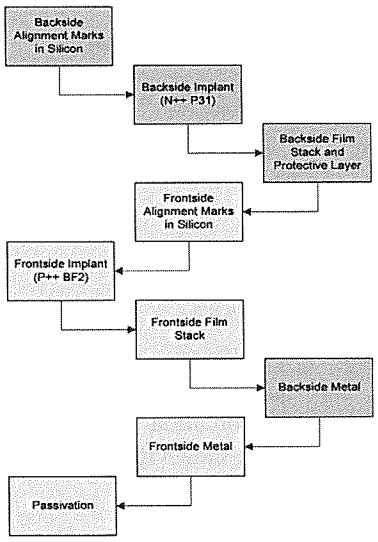

Fig. 4. Generalized Process Flow

A truncated version of the full process (which excluded photolithography steps and metal layers) was run to verify that the designed process parameters would result in the desired junction depths and sheet resistance of the implanted areas.

Blanket implants were used for ease of testing, and all of the thermal steps were included to achieve the most accurate profiles. The testing wafers were characterized using a groove and stain method to record junction depth and a four-point probe measurement was used to procure the sheet resistance of the implants. After completion of the truncated fabrication, some of the process values needed adjustment, and so changes were made to the process and then verified. These changes included phosphorus implant dose, boron implant screening oxide thickness, and deposition time for the LTO steps based on a newly calculated deposition rate. Fig. 4 to the left shows a generalized process flow for the device fabrication.

V. Device Fabrication and Results

A. Fabrication

The device run was done with three device wafers and two monitors (one for implant measurements and one to monitor metal deposition). There were 55 steps total in the last version of the process, requiring approximately 96 tool hours. During the course of fabrication, there was a problem with LTO uniformity, even though the testing run had much better quality of oxide with the same settings. This led to difficulties in etching the films, which then led to a degradation of the surface (scratches and plasma damage), which would then affect device performance.

B. Results

A series of tests were done on the implant wafer and device wafers to ascertain well profile characteristics and I-V characteristics (both reverse and forward biased). Table 1 shows the well characteristics from the implant monitor wafer. The sheet resistance and junction depth were taken as measurements, with the surface concentration derived from those two values using Irvin's Curves.

Table 1. Well Profile Characteristics (Measured)

N-Implant	
Sheet Resistance	994 $\Omega/_{\square}$
Junction Depth	0.76 um
Surface Concentration	$3x10^{18}$ cm^{-3}

P-Implant	
Sheet Resistance	1085 $\Omega/_{\square}$
Junction Depth	0.44 µm
Surface Concentration	$2x10^{19}$ cm^{-3}

Fig. 5 below shows the forward bias condition for all three of the device wafers, tested on the test die shown in Fig. 6.

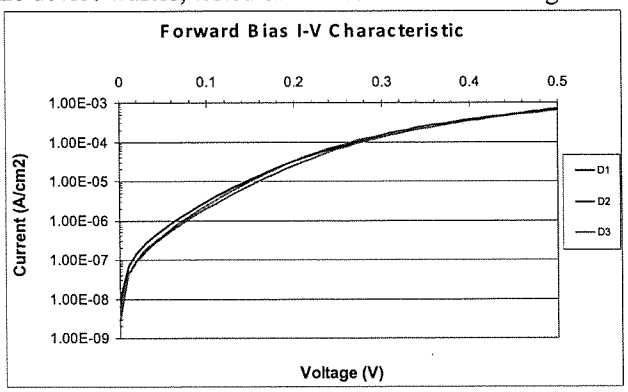

Fig. 5. Forward Bias Characteristic

The test die is larger than the actual pixel size so that hand probes could be placed with ease. From the curves in Fig. 5, the ideality factor for each device wafer's test diode can be obtained. The ideality factor refers to how closely the diode performance coincides with ideal assumptions. The number always falls between one and two and is represented as 'n' in Eq. 1

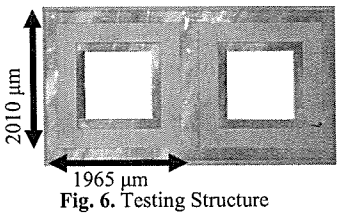

Fig. 6. Testing Structure

$$I_D = I_S(e^{(V_D/nV_T)} - 1), \qquad \text{Eq. 1}$$

where I_D is the diode current, I_S is the leakage current (or dark current for a photodiode), V_D is the voltage placed on the diode, and V_T is the turn-on or threshold voltage for the device. Table 1 to the right shows the ideality factors for all three device wafers, the average being 1.31.

Table 2. Ideality Factors

Sample	Ideality Factor (n)
D1	1.36
D2	1.26
D3	1.31

A reverse bias curve was also obtained from the device wafers and the data is reported below in the graph in Fig. 7.

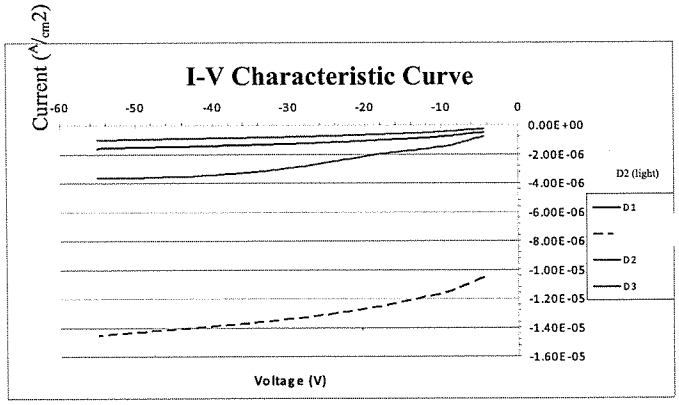

Fig. 7. I-V Characteristic Curve, Reverse Bias

The average dark current at a 50V reverse bias is on the order of $1x10^{-6}$ $A/_{cm^2}$, three orders of magnitude higher than the goal. This is likely due to insufficient anneals and the surface damage described earlier. There is one curve that represents one device wafer (D2) with the light on, showing that the diode functions as a photodetector.

Figures 8 and 9 show the top down views for the frontside and backside (in comparison with Fig. 2), respectively. It may be seen that while the wet etching worked sufficiently on the backside patterning (due to the relatively large and isolated features), the wet etch was not sufficient for the frontside due to the dense features and therefore resulted in over-etching of the oxide contact cuts (note the round shape as opposed to the on-mask square shape). The metal was also under-etched due to the dense features as well, resulting in larger than desired contact pads, encroaching on the metal grid pad.

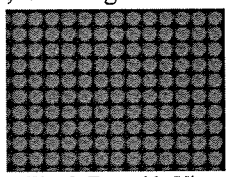

Fig. 8. Frontside View

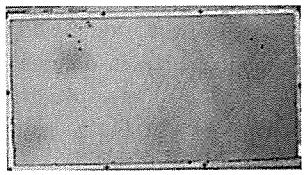

Fig. 9. Backside View

VI. Conclusions and Future Work

The process was an overall success, with the exception being the contact etching parameters. Based on results from the full process run, changes were made to increase the total tool time to 100 hours and 59 steps.

For future work, dry etches will be looked into for the contact etches. Etch rates, possible changes to the gas flows, and endpoint detection will be investigated to provide the optimum etch with minimal over-etching.

In addition to the dry etch experiments, the anneals will be optimized to decrease the damage remaining from the implant, resulting in lower dark current. Also, since the area of the test die is much larger than that of the individual pixels, the perimeter parasitics will be larger in theory. Characterization of perimeter to area ratios and the resulting dark current (for the same implants that will have the same bulk dark current) will help to eliminate the parasitics' contribution to the dark current.

Appendix

Final full process flow below: (DW = Device Wafers, IMP = implant monitor, ET = metal monitor)

Step	Process	Details	Include	Record
1	RCA Clean	RCA Wetbench	DW	-
2	Protective Oxide Growth	Bruce Furnace, Tube 1, Recipe #311	DW	Oxide Thickness
3	Coat Frontside with Photoresist	CEE Hand Coater, 120C for 60s	DW	-
4	Etch Backside Oxide	10:1 BOE, 2 minutes (586 A/min) (be sure that it pulls dry)	DW	-
5	Remove Photoresist	PRS-2000 Bench	DW	-
6	Photo 1 - Backside Alignment marks	Coat HMDS on CEE Hand Coater Bake at 90C for 30s Coat Resist on CEE Hand Coater Bake at 90C for 60s Expose on KarlSuss MA56 Bake at 140C for 90s Develop on CEE Hand Developer	DW	-
7	Etch Silicon Alignment Marks	DryTech Quad, use carrier wafers, recipe "polysilicon", 1 min	DW	-
8	Strip Photoresist	Branson Asher, 4" Normal Ash	DW	-
9	Etch Remaining Oxide	HF Wetbench, 10:1 BOE, 2 minutes (586 A/min)	DW	-
10	RCA Clean, RCA Wetbench	RCA Wetbench	DW	-
11	Backside Screening Oxide Growth	Bruce Furnace, Tube 4, Recipe #458	DW + IMP	Oxide Thickness
12	Backside Phosphorus Implant	Varian 350D Implanter, Dose = 5e14, Energy = 33keV, P31	DW + IMP	-
13	Strip Oxide, BOE Chemical Bench	HF Wetbench, 10:1 BOE, 1 minute (586 A/min)	DW + IMP	Junction Depth
14	Anneal	AG610A/B RTA, 1000C, 3 minutes	DW + IMP	-
15	RCA Clean	RCA Wetbench	DW + IMP	-
16	Backside Oxide Growth	Bruce Furnace, Tube 4, Recipe #450	DW + IMP + ET	Oxide Thickness
17	Backside LTO Deposition	LPCVD Upper Tube, 425C LTO recipe, 53 min.	DW + IMP + ET	Oxide Thickness
18	Backside Protection Silicon Nitride Growth	LPCVD Tube #2, Factory Nitride Recipe, 23 minutes	DW + IMP + ET	Nitride Thickness
19	Backside Photoresist Protective Coating	Coat Resist on CEE Hand Coater Bake at 120C for 90s	DW + IMP + ET	-
20	Dry Etch of Nitride on the frontside of the wafer	DryTech Quad, Nitride Recipe, 2.5min (stop on LTO)	DW + IMP + ET	-
21	Oxide Etch frontside oxide	HF Wetbench, 10:1 BOE, 4 min (1600 A/min, 586 A/min-Th)	DW + IMP + ET	-
22	Strip Photoresist	Branson Asher, 4" Normal Ash	DW + IMP + ET	-
23	Photo 2 - Frontside Alignment marks	Coat HMDS on CEE Hand Coater Bake at 90C for 30s Coat Resist on CEE Hand Coater Bake at 90C for 60s Expose on KarlSuss MA56 Bake at 140C for 90s Develop on CEE Hand Developer	DW	-
24	Etch Silicon alignment marks	DryTech Quad, use carrier wafer, recipe "polysilicon",1.5 min	DW	-
25	Strip Photoresist	Branson Asher, 4" Normal Ash	DW	-
26	RCA Clean	RCA Wetbench	DW + IMP	-
27	Frontside Screening Oxide Growth	Bruce Furnace, Tube 4, Recipe #456	DW + IMP	Oxide Thickness
28	Photo 3 - Frontside Well Definition	Coat HMDS on CEE Hand Coater	DW	-

		Bake at 90C for 30s Coat Resist on CEE Hand Coater Bake at 90C for 60s Expose on KarlSuss MA56 Bake at 140C for 90s Develop on CEE Hand Developer		
29	Frontside Boron Well Implant	Varian 350D Implanter, Dose = 1e15, Energy = 33keV, BF2	DW + IMP	
30	Strip Photoresist	Branson Asher, 4" Normal Ash	DW	-
31	Etch Oxide (damaged from implant) Frontside	HF Wetbench, 10:1 BOE, 2 minutes (586 A/min)	DW + IMP	Junction Depth, rs
32	Anneal	AG610A/B RTA, 1000C, 3 minutes	DW + IMP	-
33	RCA Clean, RCA Wetbench	RCA Wetbench	DW + IMP	-
34	Frontside Oxide Growth	Bruce Furnace, Tube 4, Recipe #450	DW + IMP	Oxide Thickness
35	Frontside LTO Deposition	LPCVD Upper Tube, 425C LTO recipe, 53 min.	DW + IMP	
36	Coat Frontside with Photoresist	CEE Handspinner, 120C for 60s	DW + IMP	
37	Backside Oxide Etch (remove any oxide on the nitride)	10:1 BOE Cup Etch, 5 minute (586 A/min)	DW + IMP	-
38	Strip Photoresist	Branson Asher, 4" Normal Ash	DW + IMP	
39	Strip Backside Silicon Nitride	Hot Phosphorus Bench, 45 min	DW + IMP	-
40	Coat Frontside with Photoresist	CEE Hand Coater, 120C for 60s	DW + IMP	
41	Photo 4 - Backside Contact Etch	Coat HMDS on CEE Hand Coater Bake at 90C for 30s (Proximity Bake) Coat Resist on CEE Hand Coater Bake at 90C for 60s (Proximity Bake) Expose on KarlSuss MA56 Bake at 140C for 90s (Proximity Bake) Develop on CEE Hand Developer	DW	-
42	Etch Oxide (backside contacts)	10:1 BOE Etch, 3.5 minutes (1600 A/min, 586 A/min)	DW + IMP	Junction Depths, rs
43	Strip Photoresist	PRS-2000 Bench	DW + IMP	-
44	Backside Aluminum Deposit	CVC601 Sputter, 15sccm Argon, Power = 1500W, 5mT, 930s	DW + ET	Al Thickness
45	Photo 5 - Backside Aluminum Etch	Coat HMDS on CEE Hand Coater Bake at 90C for 30s Coat Resist on CEE Hand Coater Bake at 90C for 60s Expose on KarlSuss MA56 Bake at 140C for 90s Develop on CEE Hand Developer	DW	-
46	Wet Etch of Backside Aluminum	Aluminum Etch Bench, 1 minute 20 seconds	DW + ET	-
47	Strip Photoresist	PRS-2000 Bench	DW	-
48	Backside Photoresist Protective Coating	CEE Hand Coater, 120C for 60s	DW	-
49	Photo 6 - Frontside Well Contact	Coat HMDS on CEE Hand Coater Bake at 90C for 30s (Proximity Bake) Coat Resist on CEE Hand Coater Bake at 90C for 60s (Proximity Bake) Expose on KarlSuss MA56 Bake at 140C for 90s (Proximity Bake) Develop on CEE Hand Developer	DW	-
50	Etch Oxide - Frontside Contacts	10:1 BOE, 3.5 minutes (1600 A/min, 586 A/min)	DW + IMP	-
51	Strip Photoresist	PRS-2000 Bench	DW	-
52	Frontside Aluminum Deposition	CVC601 Sputter, 15sccm Argon, Power = 1500W, 5mT, 930s	DW + ET	Al Thickness
53	Photo 7 - Frontside Contact Etch	Coat HMDS on CEE Hand Coater Bake at 90C for 30s (Proximity Bake) Coat Resist on CEE Hand Coater Bake at 90C for 60s (Proximity Bake) Expose on KarlSuss MA56	DW	-

		Bake at 140C for 90s (Proximity Bake) Develop on CEE Hand Developer		
54	Wet Etch of Frontside Aluminum	Aluminum Etch Bench, 1 minute 20 seconds	DW + ET	
55	Strip Photoresist, PRS 2000	PRS-2000 Bench	DW	-
56	Frontside Passivation Layer Deposition of LTO	LPCVD Upper Tube, 425C LTO recipe, 4 min.	DW + ET	Oxide Thickness
57	Photo 8 - Passivation Layer Trim	Coat HMDS on CEE Hand Coater Coat Resist on CEE Hand Coater Bake at 90C for 60s Expose on KarlSuss MA56 Bake at 120C for 60s Develop on CEE Hand Developer	DW	-
58	Etch Passivation Layer, BOE Chemical Bench	"Pad Etch", 15 minutes (38 A/min)	DW + ET	-
59	Strip Photoresist, PRS 2000	PRS-2000 Bench	DW	-

End

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