Fabrication of an Esaki Tunneling Diode by Proximity Rapid thermal diffusion

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Abstract—**Tunnel diodes need degenerately doped junction to optimum performance. They are fabricated using the Molecular Beam Epitaxial method. This method yields good degenerately doped junctions. However it is not clear whether the process can be used with 300 mm wafer technology due to the demand for a high thermal budget. Proximity Rapid Thermal Diffusion (PRTD) uses the RTP tool for its thermal processing. The amount of time used for the processing is in seconds which yields to a low thermal budget. Moreover RTP tools are a common place in the industry and hence comparatively, PRTD is easy to integrate into the wafer fabrication process. Tunneling diodes are fabricated using the proximity diffusion technique where a dopant is diffused from a source wafer to a device wafer in a RTP chamber. The resulting devices yielded PVCR of 2.1 and a current density of 160 mA/cm^2 at 300K. The performance of this device is better than the device which was fabricated before at 850 ^{0}C. This paper discusses the process flow and the results of the fabricated devices.**

Index Term - Tunneling, Tunnel diode, Peak to valley current ratio(PVCR), Spin on Glass(SOG), Proximity Rapid thermal diffusion (PRTD)

I. INTRODUCTION

Tunneling diodes employ the quantum mechanical effects of tunneling for their operation. They offer lower leakage current and faster switching speeds compared to normal diodes.

The proximity rapid thermal diffusion process is a method by which dopants are transferred from a source wafer to a device wafer at a certain temperature and ambient. The dopant, in the form of spin on glass is spun on the wafer and cured. This is placed facing the source wafer separated by a spacer usually at a distance of 300 um. Due to the heat the dopant gets transferred from the source wafer to the device wafer. The process is carried out in a Rapid thermal anneal chamber.

The rapid thermal anneal process is used commonly in the industry today. After the ion implantation process, wafers are usually undergo rapid thermal anneal to anneal the damaged lattices in the silicon structure.

Tunneling diodes are usually fabricated by Molecular beam epitaxy. This process is very efficient in providing the degenerately doped profile of the tunneling diode. But this process is not feasible with 300mm wafer technology and is vey cost consuming. PRTD, on the other hand is very cost efficient, using only the RTA chamber and requires low thermal budget.

But however the PRTD is influenced by a number of factors such as heating rate, cooling rate, ambient flow rate and source preparation to name a few. There is also no technique which allows to measure the amount of dopants transferred during the process.

II. THEORY

A. *Tunnel Diode*

Tunnel diodes are diodes which have a negative resistance region in the forward bias mode and have very high switching speed in the GHz range. The diode works on the principle of Quantum mechanical principle of tunneling. If the doping characteristic of a diode is very high, a thin depletion region results in the flowing of the majority carriers through the thin depletion region, even if the potential barrier across is greater than the kinetic energy of the particle.

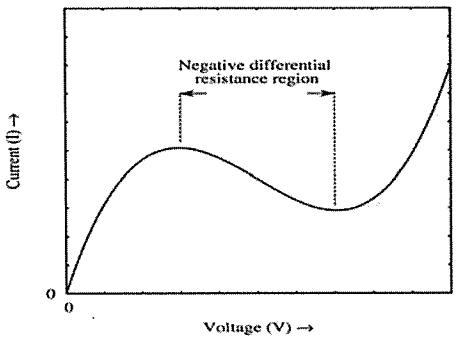

Figure 1: Tunnel diode I-V curve

Figure 1 shows the I-V characteristics of a tunnel diode. As the voltage increases, the current increases as is usual with a normal p-n junction diode. But after a point, as the voltage increases, the current starts to decrease. After a point, as the voltage increases, the current again starts to increase. The region where the current decreases as the voltage increases is called the negative differential resistance region of the tunnel diode. This is a characteristic unique to tunnel diodes.

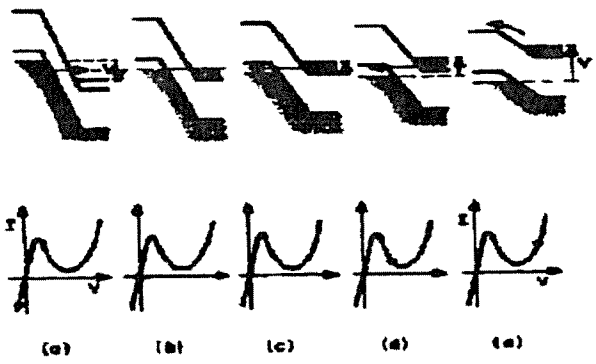

Figure 2: Band diagram under various biasing conditions

The tunnel diode is degenerately doped so that abrupt junctions are created. An ideal junction for a tunnel diode is 10nm. Figure 2 shows the band diagram under various biasing conditions of the tunnel diode. Fig 2.2(a) shows the diode under negative potential or reverse bias. In this condition, the electrons from the occupied stated from the p-side tunnel to the n-side giving a negative current. Under zero biased condition, no tunneling take place and as a result no current is present. This is shown in fig 2.2 (b). Fig 2.2(c) shows the diode under small forward bias. In this condition, the electrons from the n-side conduction band tunnel into unoccupied sites of the p-side valence band. As the conduction and valence band uncross, the tunneling decreases leading to a decrease in current as shown in fig 2.2 (d). As the applied potential exceeds the built in potential, normal diffusion current of the diode takes over and the current increases once more.

B. Proximity Diffusion

Proximity diffusion is carried out in a rapid thermal anneal chamber. Proximity diffusion is similar to the CVD process but unlike CVD, the dopants are obtained from a source wafer rather than gasses flown into the chamber. The tungsten halogen lamps emit the ultraviolet radiation which is readily absorbed by the silicon wafer. As a result the silicon wafer heats up. This heating causes the diffusion of the dopants from the source wafer and absorption of the dopants in the device wafer.

This diffusion technique relies heavily on the preparation of the silicon on glass sample. The diffusion properties of the SOG are affected by the thickness, cure time and cure temperature. The SOG is spun on the source wafer and cured at a certain temperature.

Studies have shown that optimum diffusion occurs with thicker SOG layers and hence it is cured at 200C. There are two methods to measure the temperature inside the chamber. The two methods are by attaching a thermocouple to the back of the silicon wafer of by a pyrometer. A thermocouple is ensures accurate readings at a cost and thermal budget while a pyrometer is cheap but does not ensure accurate reading.

III. PROCEDURE

The Esaki diodes were fabricated on a Six inch wafer which already had a high n-doping of the 1E19 cm^{-3} and 1 milliohm resistivity. One six inch p-type wafer was used as a source wafer. Phosphorsiclica was used as an n-type dopant source and Borofilm was used as a p-type dopant source.

At first the source wafer was prepared. The Source wafer was cleaned. At first the Phosphorsilica was coated on the wafer. The coating was done at 3000 rpm for 40 seconds on the manual coater. The wafer was then cured for 20 minutes inside the Blue M oven at 200C. During this time, the device wafer was cleaned with HF to remove any surface oxide.

The RTA needed to be optimized to make sure the temperature was achieved as fast as possible and at the same time it didn't overshoot a lot. After the source wafer was taken out of the oven it was cleaved into 4 pieces. One piece of the source wafer is placed facing down on the device wafer separated by three spacers at each corner.

The RTA process was run at the desired temperature for 1 second. Following the RTA run, the source wafer was removed and the just the device wafer was run for the drive in process for 90 seconds. Following this, another source was prepared with the Borofilm dopant source. The bottle was warmed and the wafer was coated with the solution at 3000 rpm for 40 seconds, following by the curing process at 200C for 20 minutes. The device wafer was again dipped in HF for 30 seconds to remove any native oxide. The source was broken into 4 pieces and one piece was placed facing down on the device wafer, separated by spacers. The process was run for 1 sec at the desired temperature.

After the diffusion was carried out in the RTA, the wafers were cleaned with HF (50:1) in the wet bench and prepared for aluminum deposition. The CVC Evaporator was the tool used for the deposition of aluminum. Tungsten baskets were loaded with aluminum and placed inside the chamber. The wafers were placed inside the chamber and the pump down for vacuum was initiated. The pressure was allowed to go to 2.4E-7 torrs. Following this the filament was heated to melt the aluminum. 2000 Angstroms of aluminum was deposited.

The aluminum deposition was followed by photolithography. The Karl Suss 6" mask aligner was used for the photolithography step. HPR 504 wafer was coated on the wafer at 3000 rpm for 45 seconds. The wafer went through pre bake at 90C for 60 seconds. Exposure dose of 115 mj/cm^2 was required. The exposure was run for 16 seconds followed by post exposure bake at 115 c for 60 seconds. The photoresist was then developed with CD-26 developer followed by a bake at 120C for 120 seconds.

The wafer was placed in the Al etch bath to remove the aluminum from exposed areas. The photoresist was stripped

of and then placed in the dry tech quad to etch into the silicon to isolate each device.

The recipe used for etch contained 4 cc flow of SF6 and 16cc flow of CHF3. The pressure was 100mT and the power was 100w. The recipe was run for 65 seconds.

Following table shows the process splits used.

Wafer #	Phosphorous diffusion	Phosphorous Drive	Boron Diffusion
1	850 C , 1 Sec	850 C, 90 Sec	850 C, 1 Sec
2	900 C, 1Sec	900 C, 90 Sec	900 C, 1 Sec
3	950 C, 1 Sec	950 C, 90 Sec	950 C, 1 Sec

Table 1: Process splits used

IV. Results and Analysis

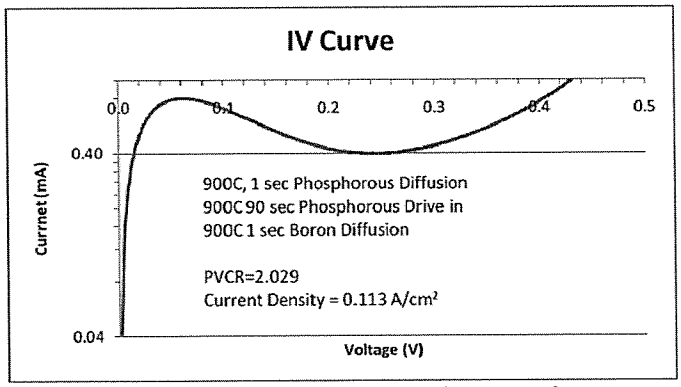

Figure 3: 30umx30um Esaki Diode with a PVCR of 2.029

Fig. 3 shows the characteristic I-V curve of am Esaki Diode with a PVCR of 2.029. The current density of this diode was 0.113 A/cm^2. The peak voltage of this device is 0.06 volts.

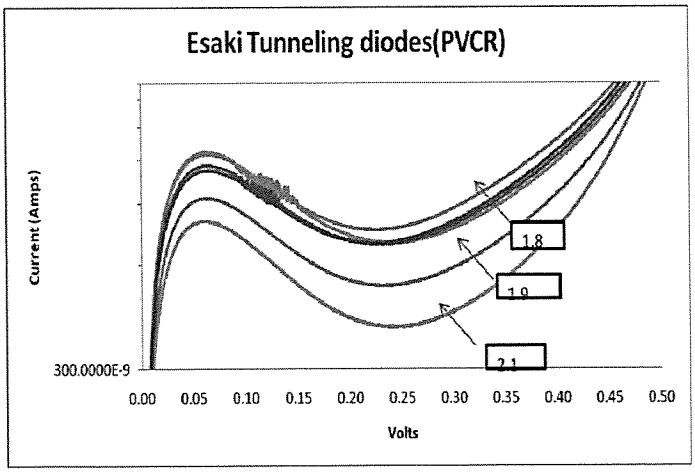

Figure 4: Comparison of the PVCRs of different devices

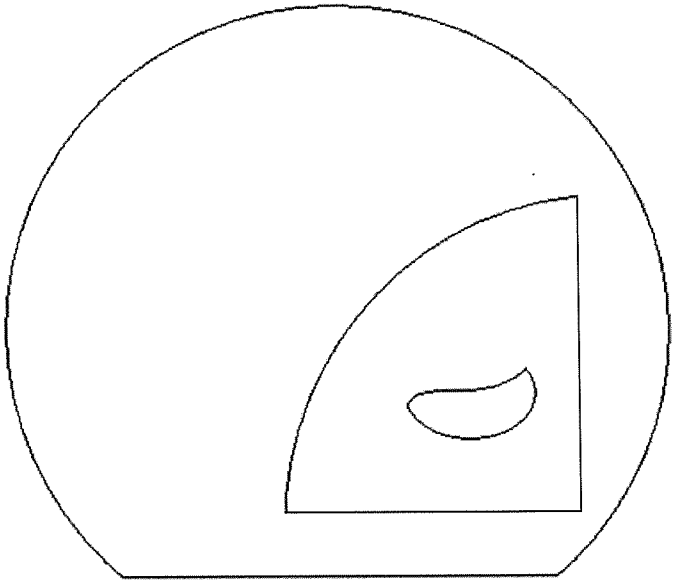

Figure 5: The figure shows the device wafer, the placement of the source wafer and the area where the working device wafers were found.

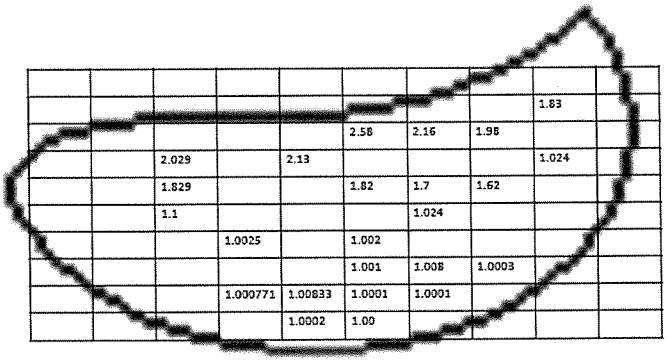

Figure 6: The map shows the PVCR of the different devices measured.

Figure 4 shows the PVCR of the different devices measured. It is seen that as the PVCR decreases, the current density decreases.

Figure 5 shows the area where the working Esaki tunneling diodes were found. The area where the quarter source wafer placed is also shown.

Figure 6 shows the measurement of the Esaki Tunneling diodes. The metal adhesion in the area above it was not good and hence the metal came out. But it is seen that as the dies move farther away from the top, the PVCR decreases exponentially.

The variation in the PVCR of the diodes is attributed to the gas flow inside the chamber. Due to the gas flow some of the dopants, while diffusing from the source wafer to the device wafer got carried away in the ambient and got deposited elsewhere. To understand the effect of the ambient inside the chamber, few dopant studies were carried out.

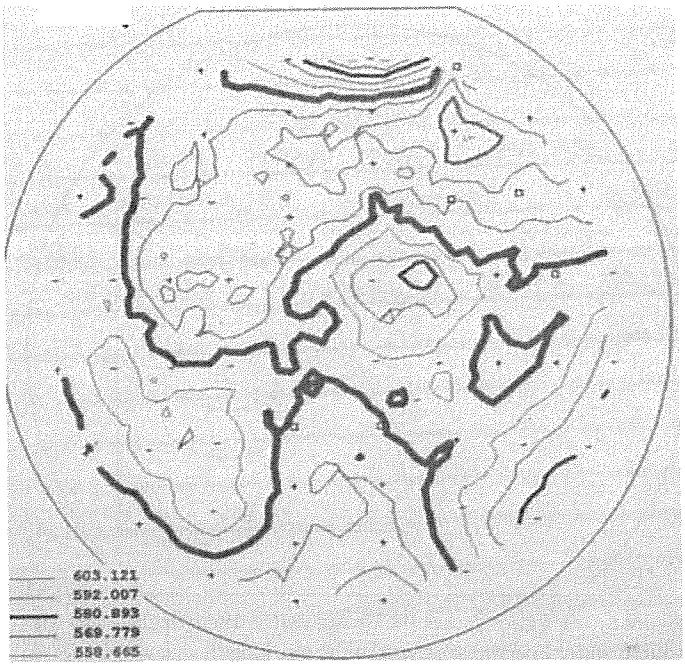

Figure 7: 6 inch wafer before the 900c Boron Proximity diffusion

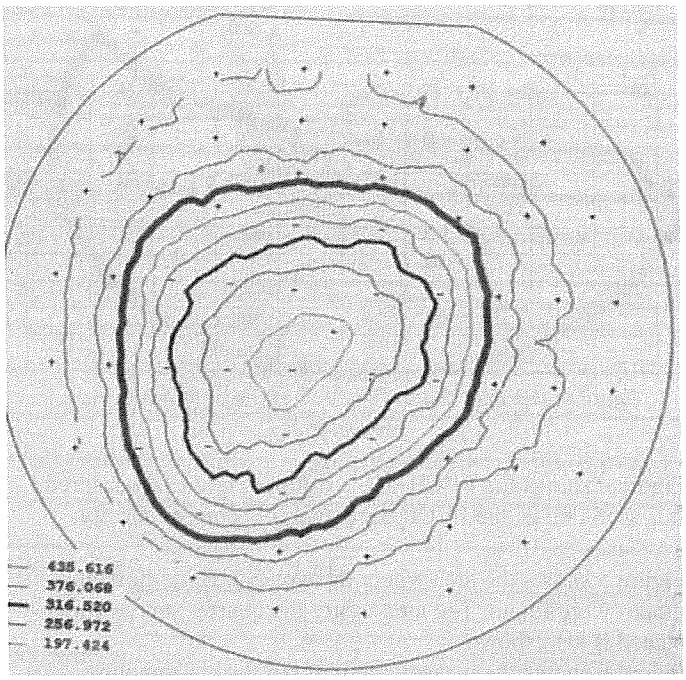

Figure 8: 6 inch wafer after the 900c Boron Proximity diffusion

Figure 7 and 8 show a p-type 6-inch wafer which went through a Boron proximity diffusion. It is seen that after the proximity diffusion some dopants diffused from the source wafer to the device wafer. But it is seen that the diffusion was not uniform as the resistivity is no the same all around. It is seen that most of the diffusion took place around the center of the source wafer area as the resistivity there is the highest. But overall some diffusion took place.

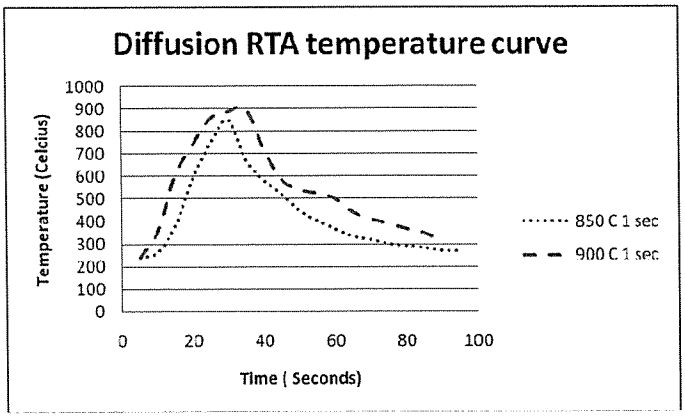

Figure 9: RTA diffusion temperature curve

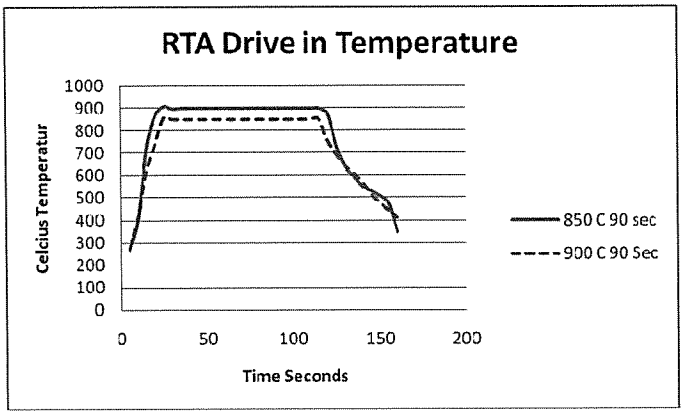

Figure 10: RTA drive in temperature curve

Figure 9 and figure 10 show the RTA drive in and diffusion temperature profile. It is very important to get the temperature high as fast as possible and cool them as fast as possible. The figures show that the ramp rate of the temperatures to be good but it takes a long time for them to cool down. Also this level of repeatability was attained after a number of trials before a real run. A thermocouple was used to measure the temperature of the wafer inside the chamber. But the thermocouple gives inaccurate readings below 300 C.

V. Conclusion

The goal of the project was to fabricate Esaki tunneling diode and to understand the tolerances involved in fabricating such a device using PRTD. Working devices with PVCR greater than 2.0 were created at 900C temperature. However the current density was small, about 160 mA/cm^2. Esaki diodes created three years ago had lower PVCR but greater current density of about 3 A/cm^2. From this project it was revealed that the process tolerances for fabrication Esaki diodes using PVTR is very small. The map of the measured dies proves this very point. There are devices with PVCR concentrated in a small region, but as the dies go away from them, the PVCR reduces exponentially.

VI. References

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