

# Fabrication of Metal-High-κ Capacitors on Germanium (May 2008)

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**Abstract**—The objective of this study is to gain understanding of MOS devices built on germanium. Ge PMOS transistors were simulated using Silvaco. MOS capacitors have been fabricated using hafnium oxide, a high-κ dielectric, and molybdenum, a metal gate. The capacitance-voltage (CV) characteristics of the devices were obtained and studied. During the deposition of hafnium oxide on germanium substrate, the surface integrity plays a significant role. Two different surface treatments for the Ge substrates were implemented: one with NH<sub>3</sub> immersion at 650°C for one minute, the other with a deionized (DI) water rinse for one minute. In doing so, one can examine how nitrogen passivation prior to the dielectric deposition impacts device performance compared to a standard rinse with DI water.

**Index Terms**—Carrier mobility, crystallinity, drive current, germanium, nitrogen passivation

## I. INTRODUCTION

The use of silicon (Si) in the semiconductor industry will soon reach a physical barrier due to drive current saturation in scaled Si metal-oxide-semiconductor field-effect transistors (MOSFETs). To address this challenge, the International Technology Roadmap for Semiconductors (ITRS) suggests replacing the strained silicon MOSFET channel with an alternate material offering higher quasi-ballistic carrier velocity and mobility than strained silicon [1]. By using germanium (Ge), a semiconductor with higher carrier mobility for both holes and electrons as well as greater source injection velocity, these scaling bottlenecks can be overcome and allow for the continual advancement of device technology approaching 16 nm and beyond. In this situation, Ge substrates can provide maximum drain saturation current while providing sufficient electrostatic control so that short-channel effects can be suppressed [2]. Through the processing of MOS capacitors on Ge and Si, one can see how substrate material impacts overall device performance and how Ge devices are advantageous in terms of greater voltage output and faster device speed. This work will lead to Ge device research and education at RIT and in turn for the continuation of device scaling and ease forward progress for the semiconductor industry as a whole.

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## II. THEORY

### A. Material Differences

The use of Ge is a logical upgrade from Si in that it is another Group IV element, meaning it has the same number of valence electrons as silicon and thus will have some of the same physical and chemical behaviors as silicon. While the two elements are comparable to a certain extent, there exist vast differences as seen in Table I below:

TABLE I  
MATERIAL DIFFERENCES BETWEEN GROUP IV ELEMENTS

Properties	Symbol	Ge	Si	Units
Bandgap at 300 K	$E_g$	0.66	1.12	eV
Breakdown E-field	$E_{BD}$	$\sim 10^5$	$\sim 3 \times 10^5$	V/cm
Drift mobility (electron)	$\mu_e$	3900	1500	cm <sup>2</sup> /V-s
Drift mobility (hole)	$\mu_h$	1900	450	cm <sup>2</sup> /V-s
Effective mass (electron long.)	$m_{le}^*$	1.64	0.98	—
Effective mass (electron trans.)	$m_{te}^*$	0.082	0.19	—
Effective mass (heavy hole)	$m_{lh}^*$	0.044	0.16	—
Effective mass (light hole)	$m_{lh}^*$	0.28	0.49	—
Intrinsic carrier concentration	$n_i$	$2.4 \times 10^{13}$	$1.45 \times 10^{10}$	cm <sup>-3</sup>
Melting point	—	937	1415	°C
Thermal conductivity at 300 K	$k_{th}$	0.6	1.5	W/cm-°C
Abundance in Earth's crust	—	$1.5 \times 10^{-6}$	27.7	%

There are numerous benefits to using Ge in the channel region of transistors, as enumerated below:

- Lower effective masses for longitudinal electrons, heavy holes, and light holes are primarily responsible for higher drift mobility values
- A smaller bandgap at room temperature is more compliant with supply voltage scaling as specified by ITRS
- The lower melting point of Ge reflects a possibility to fabricate MOSFETs with much lower thermal budget processes than are currently being utilized in industry

While Ge has many valuable properties, it also has certain characteristics that are disadvantageous when compared to Si—these are detailed below:

- The breakdown of electric-field in Ge is much lower which could be a concern for deeply scaled or high voltage Ge devices
- Higher carrier concentration and lower thermal conductivity values could be problematic with regard to

heat dissipation in integrated circuits that are already heavily tasked

- While Si is the second-most abundant element in the Earth's crust, Ge makes up only 1.5 parts per million and is thus a much more expensive material

### B. Material Cost Analysis

As was previously mentioned, the discrepancy in abundance of Ge in comparison to Si leads to an extreme cost differential between the two elements. While hyperpure silicon (i.e., of greater than 99.99% purity) costs somewhere between \$0.25 and \$0.40 per gram, the cost of Ge of equivalent purity is about \$3 per gram. Because of this increase, alternative methods have been explored to reduce transistor critical dimensions.

One such method is double patterning, a class of photolithography methods designed to enhance feature density. This technique has proven to be challenging, however, for several reasons. Most importantly, tool throughput is reduced when double patterning is employed because the same pattern requires multiple passes to be fully printed. Another glaring problem is that the yield of a double patterning process can be expected to be lower because the overall yield then becomes the product of the overlay yield, first mask yield, and second mask yield together.

Another option that has been explored is extreme ultraviolet lithography (EUVL), which uses a 13.5 nm wavelength as the irradiation source. The problem with this lithography technology, however, is that it is not fully developed for production; because of this, it cannot compete with 193 nm immersion lithography, an established process for industry. Intel, the largest semiconductor company in the world, has set the tone for the semiconductor industry by stating that they will not be using EUVL in their upcoming 22 nm production line due to its inadequacy at this time; instead, they will continue working with immersion lithography.

### C. Oxides on Germanium

Use of silicon dioxide ( $\text{SiO}_2$ ) has been common practice in the semiconductor industry for its dielectric properties. Recently, however, the negative effects of shrinking critical dimensions have been noticeably increasing. Below the 2 nm threshold for oxide thickness, one can begin to see drastic increases in tunneling effects which in turn leads to higher amounts of leakage currents. This effect can then lead to such issues as excessive power consumption in devices and reduced device reliability [7]. For this reason, new materials have been explored to allow for improved performance without the need for such small dielectric layers. These compounds, known as high- $\kappa$  materials, allow for increased gate capacitance without having leakage problems seen with older products.

These materials are especially important when using a germanium substrate as the native oxide formed on germanium ( $\text{GeO}$ ) is very volatile and easily desorbed, thus making it very difficult to control the dielectric/germanium interface. This instability also leads to a large amount of interface states which will hinder device performance [7]. For this reason, high- $\kappa$  dielectrics are essential for use on

germanium substrates as they will stabilize both interfaces of dielectric films and metals with germanium. Their addition to MOS devices should provide excellent device control and aid in the desired enhancement.

### D. Simulations

Fig. 1 illustrates through simulation how the use of Ge in the channel region of a transistor impacts device performance. By modeling a PMOS transistor with SiGe in the channel region, one can alter the percentage of Ge present in order to show how drive current changes:

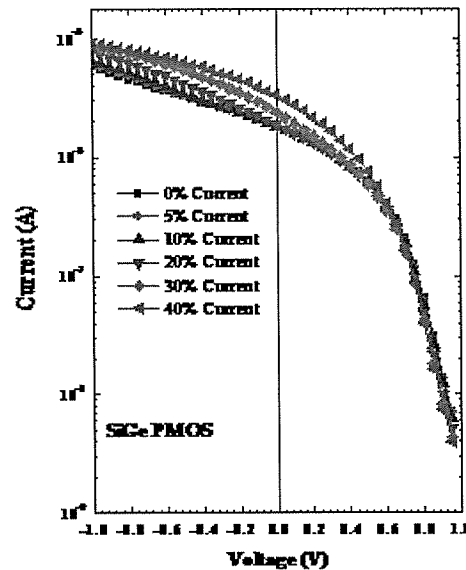


Fig. 1.  $I_{\text{drain}}$  v.  $V_{\text{gate}}$  curves of simulated data for increasing amounts of Ge in channel region.

The figure above shows a distinct increase in drive current as the concentration of Ge is augmented, thus demonstrating how Ge can greatly enhance electrical properties when used in place of Si.

## III. PROCEDURE

As was previously mentioned, two different surface treatments for the Ge substrates were implemented. The first involved  $\text{NH}_3$  immersion at 650°C for one minute in an LPCVD system prior to oxidation—this preparation should create an amorphous oxide layer. The second treatment, consisting of a one minute deionized (DI) water rinse, should instead lead to the formation of a crystalline dielectric. Following their respective surface treatments, the Ge samples were loaded into the deposition tool and underwent a 15 minute reactive sputter of hafnium oxide and a 30 minute sputter of molybdenum before being patterned and tested. The full process flow can be found below in Fig. 2:

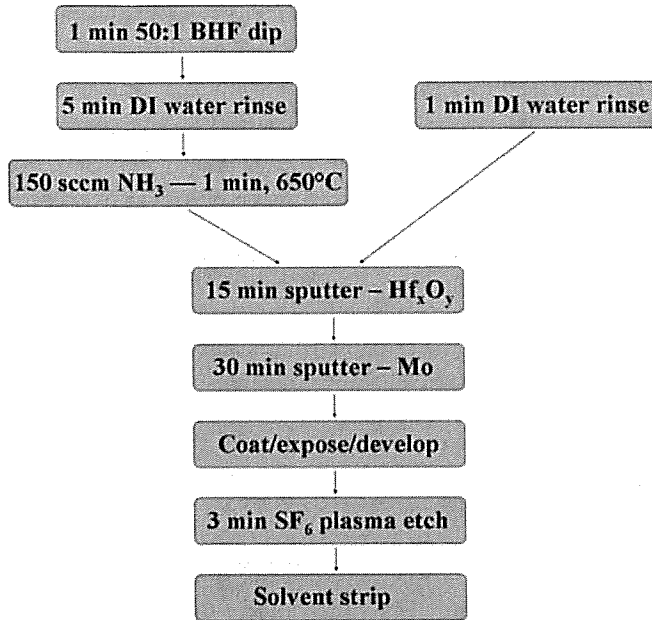


Fig. 2. Process flow describing the two surface treatments utilized on Ge.

#### IV. RESULTS

##### A. Atomic Force Microscopy (AFM) Results

In order to characterize the planarity of the hafnium oxide sputtered onto the Ge surfaces, AFM was utilized. Fig. 3 below shows the results obtained following the deposition – (a) represents the DI water treatment results and (b) shows the nitrogen passivation results. As can be seen from the figures, the DI water treatment had greater surface uniformity with a maximum variation of 5 nm. The nitrogen passivation, on the other hand, led to more variance in surface roughness with a maximum variation of 200 nm. This deviation suggests an undesirable non-planar interfacial layer that could negatively impact the device behavior [4]:

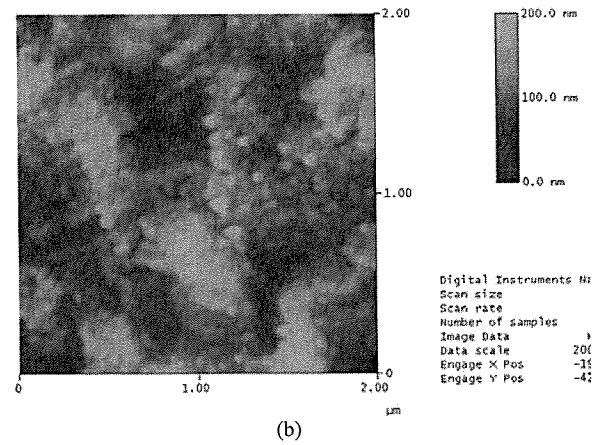
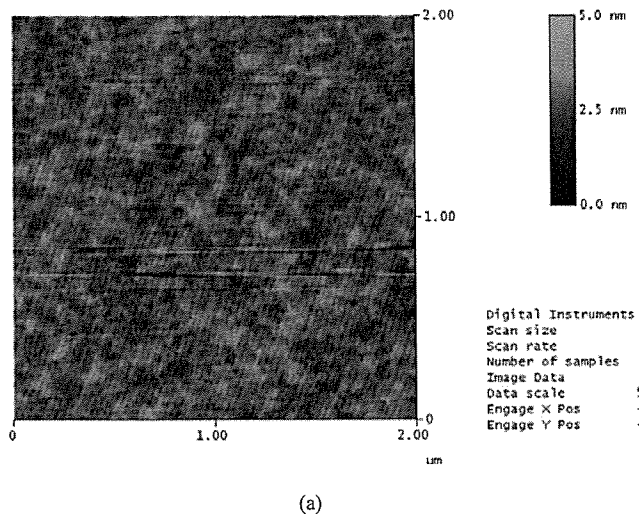
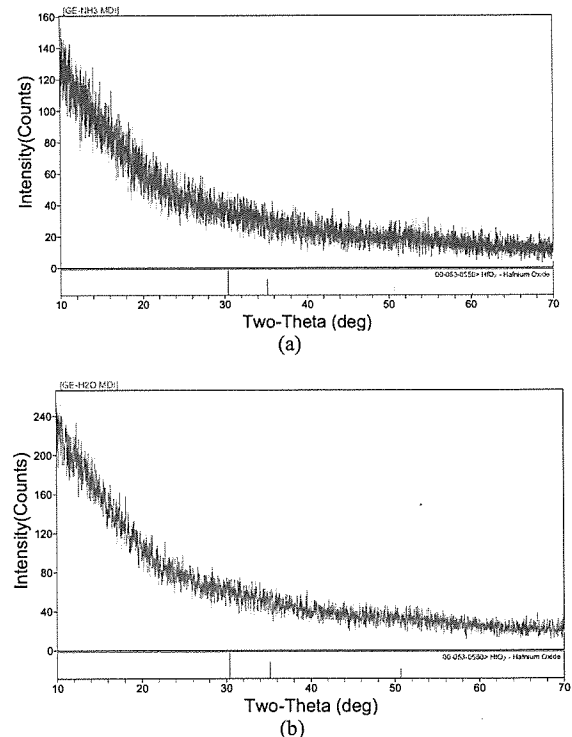


Fig. 3. AFM results showing surface roughness of Ge samples with DI water surface treatment (a) and nitrogen passivation (b) prior to oxidation.

##### B. X-Ray Diffraction (XRD) Results

X-ray diffraction, the second surface analysis performed, was used to characterize the crystallographic structure of the hafnium oxide layer. Fig. 4 shows the results obtained following the deposition – (a) represents the DI water treatment results and (b) shows the nitrogen passivation results. Following testing, the hafnium oxide was reported to exist in three polymorphic phases: tetragonal, cubic and orthorhombic phase. Unlike the predicted outcome, however, the DI water surface treatment did not lead to a crystalline dielectric film. Instead, the method resulted in similar properties to the amorphous layer created with a nitrogen surface passivation as indicated by the lack of peaks throughout the curves below:

Fig. 4. XRD results showing amorphous state of the high- $\kappa$  dielectric layer on Ge samples with DI water surface treatment (a) and nitrogen passivation (b) prior to oxidation.

### C. Capacitance-Voltage (CV) Results

Following analysis of the hafnium oxide surface, the CV characteristics of the Ge samples were examined through the use of mercury probing. As can be seen from Fig. 5 below, the Ge devices did not perform as expected when first tested:

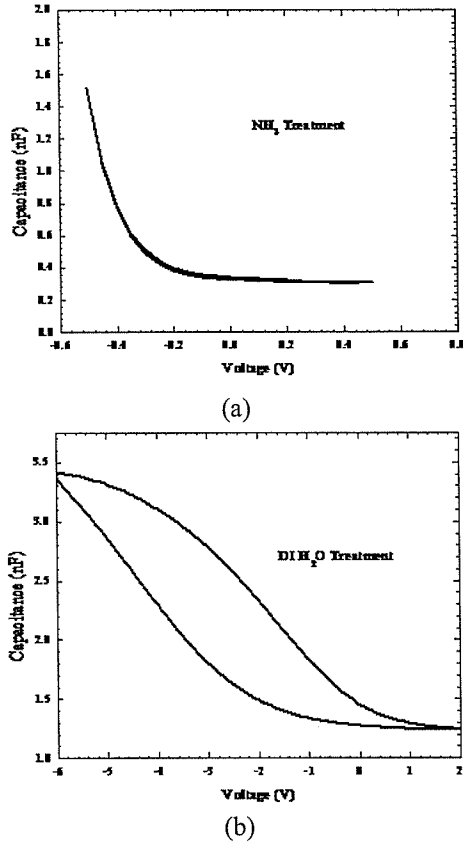


Fig. 5. C-V characteristics for Ge samples with nitrogen passivation (a) and DI water surface treatment (b) obtained using Hg-probing methods.

The nitrogen-prepared Ge sample (Fig. 5a) had issues forming a strong contact—this was likely due to an inadequate oxide layer and possible interference from the passivation layer. The DI water-prepared Ge sample (Fig. 5b) exhibited very large hysteresis—this may be attributed to presence of a large amount of interface traps. Because the test device reached accumulation, an effective oxide thickness (EOT) value could be extracted by using (1), as shown below:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox} A}{t_{ox}} \Rightarrow t_{ox} = \frac{\epsilon_0 \epsilon_{ox} A}{C_{ox}} \quad (1)$$

$$EOT = \frac{\epsilon_0 \epsilon_{SiO_2} A_{Hg}}{C_{HfO}} = \frac{(3.9)(8.854 \times 10^{-14} \frac{F}{cm})(0.0053 cm^2)}{3.5 nF}$$

$$= 5.23 nm$$

As can be seen from the equation above, the effective thickness was extracted to be 5.23 nm in comparison to the 17.7 nm of hafnium oxide deposited. This shows how the high-κ dielectric serves as a better film in that thinner layers

can be deposited without having to worry about leakage current that plagues silicon dioxide.

### D. Further Processing

Upon further processing of the devices, various issues were encountered, in particular with etching. The wet etch chemistry used did not properly remove the molybdenum and so, upon stripping photoresist, the capacitor patterns no longer remained. Following this, the wafers had another layer of molybdenum deposited and were patterned once again. For the second test, a plasma etch was used to remove metal. Upon testing of the completed capacitors, however, the capacitance values obtained were constant. These results suggest oxide was no longer present on the wafers, possibly due to the high power used in the metal deposition step which destroyed the hafnium oxide to the point where it was an ineffective dielectric.

### V. CONCLUSION

Upon completing experimentation, much was learned regarding MOS devices on Ge and how surface treatments affect performance. It was found that Ge surface treatments prior to oxidation do not impact the crystallographic structure of the oxide layer as expected and that nitrogen passivation increases surface roughness, thus causing greater variation across wafer surface. With this in mind, however, more extensive testing is needed to understand how each processing step affects Ge performance. In particular, future work should be completed with regard to hafnium oxide deposition on Ge and what thermal treatment steps are needed to optimize Ge device performance as a whole.

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