

Deep Submicron Pattern Formation for Selective Epitaxial Growth of III-V Semiconductors

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In the world of optoelectronics a common barrier has been integrating logic and device circuits on a single substrate, as it was generally only possible to optimize the device for the logic, or the optoelectronic device at hand. However, a new approach that uses metal organic chemical vapor deposition (MOCVD) enables the growth of III-V semiconductors on silicon substrates. The fact that III-V semiconductors can now be integrated within the current silicon CMOS processes may allow new possibilities. An approach to investigate the feasibility of this process has been investigated. The enabler to integrate III-V is an innovative approach called aspect ratio trapping (ART) developed by Amberwave. This method involves the use of oxide trenches to trap defects in a buffer region during crystal growth (Figure 1). The growth process is a selective growth that only occurs on silicon and this process. ART on III-V's only works well with a ratio greater than 2:1 for oxide thickness to patterned oxide opening. The objective of this project is to develop a process to build these structures at RIT, perform a growth in Amberwave's reactor, and then characterize the film. In the future, RIT may also become involved in the Chemical mechanical planarization (CMP) process for these structures.

A mask was designed with four different pitches to characterize different density of features (fig. 5). Text labels were also added on the mask so that one could optically determine the pitch and in addition the reticle had labels that describe the relative field position to be used for CMP characterization. In order to be able to pattern the submicron features with a positive tone resist, a bottom antireflective coating (BARC) donated by Brewer Science was used to increase the process window in which a useable image was present. The thickness of this layer was tuned specifically to minimize the substrate reflection. By optimizing film thickness parameters and setting the focus near the bottom of the resist, this yielded much greater process latitude. After this the patterns were etched using the P5000's magnetically enhanced etch chamber, the etched features were imaged a new Zeiss SEM at University of Rochester and the 3:1 etched features yielded acceptable profiles (fig. 10).

In order to prepare patterned wafers here at RIT, the level of contamination in the process and toolset at RIT must to be characterized. The main concern is to not contaminate the growth chamber that Amberwave will be using to perform the growth of the semiconductor materials. A method of metals analysis called vapor phase decomposition-inductively-coupled plasma mass spectrometry (VPD ICP MS) was utilized as a surface contamination metric. After sending the samples to ChemTrace, it was determined that an RCA would dramatically reduce the surface contaminants present on the wafer to acceptable levels for the MOCVD reactor (fig. 6).

Interesting future projects include building and characterizing a GaAs laser. Another appealing project involves building silicon drive transistors connecting them to GaAs tunneling or memory devices. It was shown that the pattern transfer portion is indeed possible at RIT and this project has set the stage for future projects regarding aspect ratio trapping.

Index Terms—Aspect Ratio Trapping, Gallium Arsenide epitaxy, VPD ICP MS

I. INTRODUCTION

THIS project investigates the task and process steps involved in patterning and characterization of submicron high aspect ratio structures at the Rochester Institute of Technology. ART (aspect ratio trapping) is a selective growth process developed by Amberwave Systems. Shown in fig. 1 there are two different samples of GaAs epitaxially grown on silicon. The first sample does not contain any oxide side walls to act as a trapping site. Observe on in fig. 1 b. the images shows single crystalline silicon with no defects at the device surface.

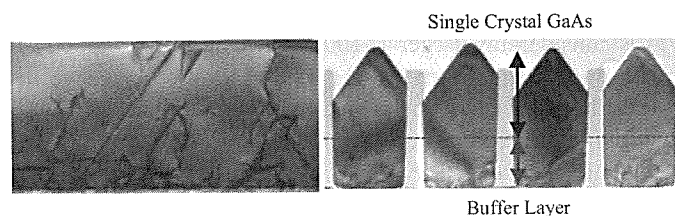


Fig. 1 a. Bulk GaAs on silicon with surface defects b. ART GaAs

Currently Amberwave does all of their patterning with a company that performs interference beam lithography. This is a rather expensive process, and it is desirable to build a process at RIT to be able to pattern these kinds of structures. Their current process also lacks additional items that were added to the current reticle design to make characterization less complicated. Motivation to work with ART samples it is a very efficient way to integrate III-V's on silicon substrates. This process also would work well to make optoelectronic/photonic devices on silicon substrates and high mobility MOSFET channels.

The goals for this project were to pattern high density oxide openings for Amberwave's structures. Amberwave has determined that they would like to characterize growth on two different profiles. The profile on the left (fig. 2 a) is a high aspect ratio 2:1 RIE (reactive ion etched) oxide sample. The profile on the right (fig. 2 b) is a similar sample, but it has an additional Etch performed to give it a V shaped profile on the bottom. Another key aspect of this project

is to design a reticle that can be patterned with the equipment here at RIT. Finally, the appropriate process conditions were determined which included the following: minimum feature size, transferring this pattern via an etch, and characterizing the contamination levels in our lab. Finally the final profiles were evaluated.

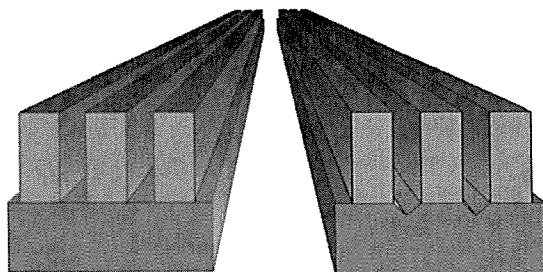


Fig. 2 a. RIE etched Sample b. RIE KOH etched sample.

II. THEORY

2.1 VPD ICP MS Concepts

The VPD ICP MS process involved several steps. First the wafer was placed in an ultra clean wet etch chamber. This chamber was highly saturated with hydrofluoric acid vapor. The oxide then reacts with the HF vapors. A drop of ultra pure acid etchant was added to the surface of the wafer and the surface contaminants were then incorporated into this liquid. This liquid was then collected and the ICP- MS analysis was then performed. A Perkin-Elmer Sciex ELAN 6100 DRC ICP-MS was used in the ICP MS analysis. It was calibrated with the three different NIST standards for the thirty metals under examination. The thirty elements were Al, As, B, Ba, Be, Bi, Ca, Cd, Co, Cr, Cu, Ga, Ge, Fe, In, K, Li, Mg, Mn, Mo, Na, Nb, Ni, Pb, Sb, Sn, Sr, Ta, Tl, Ti, V, W, Zn and Zr. The detection limit was generally on the order of 10^7 or 10^9 atoms/cm² depending on the size of the wafer and trace element being tested. The accuracy of this method was based on the level of the signal above the detection limit. Generally when the signal was greater than one order of magnitude above the detection limit, the data had an accuracy of +/- 15%, but when it was lower than this threshold value it had an accuracy of +/- 30%.

$$\text{Surface Conc} = \frac{(C_s - C_b) \times V \times D \times N_A \times 10^{-12}}{AW \times S}$$

Equ. 1 Surface concentration data

Equation 1 can be explained as the method of how the amount of material in the liquid sample is converted into atoms/cm² on the wafer surface. C_s was the concentration of the sample material of interest in the solution and C_b was the concentration of the baseline sample. V is the volume of the etchant solution in mL and D is the density of this solution in g/cm³. N_A was Avogadro's number to convert for the number of moles of the sample. AW was the atomic weight of the trace metal of interest and finally S represented the analysis surface area.

The Perkin Elmer Sciex ELAN offers many advantages in comparison to many of the other ICP MS systems available. It used several novel design features that enable it to have very good sensitivity to elemental species that before were very difficult to analyze. One of the main problems with many past ICP MS systems was that there are polyatomic interferences species that are the same atomic weight as the analyte species at hand. The Perkin Elmer system used a dynamic reaction cell (DRC) that chemically scrubbed the interfering species from the ion beam by using a reaction gas that

did not interfere with the plasma chemistry and also does not change the signal of the analyte ion. Shown below (fig. 3) is the typical setup for the DRC system. This system, along with several other features, have been shown to drop the background noise by a factor of 1,000,000 in comparison collision based systems. A common interference is an argon oxygen plasma species which has an atomic weight of 56, which is the same atomic weight of the most common isotope of iron. By using this chemical scrubbing technique it almost completely eliminates all of the background noise resulting in very low and efficient detection limits. This method of metals analysis was also much more sensitive than SIMS, TXRF or similar methods.

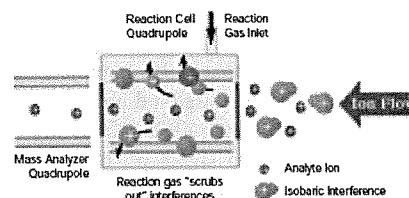


Fig. 3 ICP system basic layout [2]

2.2 LITHOGRAPHY SIMULATIONS

The first part of the project involved determining what the minimum pitch to pattern here at RIT. Prolith was used to perform lithography simulations. Generally for imaging to occur a NILS value of 3 or greater was determined to be desirable, so this was what determined the minimum half-pitch. The minimum half pitch used was 400 nm to allow for some room in the process window. This ended up being a K1 of .58 which is fairly aggressive for full field imaging .

$$\frac{P}{2} = \frac{k_1 \lambda}{NA}$$

Equ. 2 Resolution minimum half pitch equation.

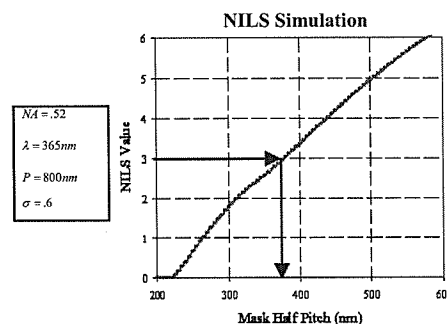


Fig. 4 NILS simulation

In order to achieve the desired pitch on a wafer with a thermally grown oxide wafer, an additional step had to be taken to increase the process window. An I-line BARC was chosen to perform this task. Brewer Science's ARC I-CON 16 was generously donated to RIT by Brewer Science. This BARC was chosen because it was not developable in CD-26. This BARC had to be etched, so it should end up with a much more anisotropic profile giving a much better process window rather than an isotropic wet developable BARC. A BARC or bottom antireflective coating increases the process window by minimizing the substrate reflection. Shown here are three profiles. It can be seen that the second sample with the oxide has 3 interfaces, more that allow interference to occur which can cause standing waves to form during the exposure process. Standing waves are generally undesirable and decrease the process window. By tuning

the thickness of the BARC layer the optical path length can be set correctly so destructive interference occurs at the photoresist-BARC interface and thus reflection is minimized at this surface and consequently standing waves are minimized.

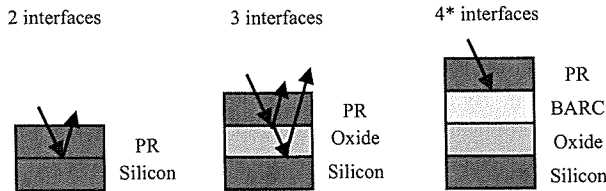


Fig. 5 Substrate reflections with various films

III. DESIGN

The first part of the design phase of this project was to push the lithography to the limits of the toolset and process capability at RIT. The limiting factors on the Cannon FPA-2000i I-line stepper were a numerical aperture of .52 and a sigma of .6. Based on the NILS simulation a reticle was designed to incorporate the most dense features capable here at RIT.

The lithography constraints were that patterning must occur on 6 inch wafers, because there would be more useful die on 6 in wafers and also this size will work well with the geometry of their reactor. The field size was also limited by bulk device and optical characterizing. RIT in the future may be involved with the CMP of some of these post growth structures. Fig. 1 shows the results of performing a growth and the CMP of these samples is not trivial, due to dishing in the oxide spacer sidewalls, hence the reason for the four different pitches chosen. Finally these features must be transferred to the underlying oxide and maintain a high aspect ratio: greater than 2:1. This means that in order for the current process to be acceptable the structure will need at least a micron of oxide to be able to obtain these high aspect ratio features based on the 400 and 500 nm limitation in the lithography process. Figure 5 shows the arrangement of the new reticle with contacts in the KERF regions.

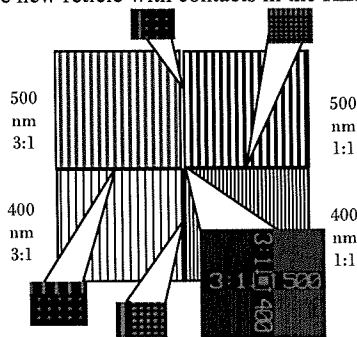


Fig. 5 RIT ART mask design

IV. CHALLENGES ENCOUNTERED

The first main concern was to determine the metal levels in our laboratory. A method of characterizing this process was to perform a vapor phase decomposition inductively coupled plasma material spectrometry (VPD ICP MS) analytical test to determine the metal levels running through our process flow. This must be completed so that Amberwave's reactor does not become contaminated.

Another Main issue during the process development was the writing of a reticle. These current features written were some of the smallest and certainly the most dense patterns written at RIT. The main problem in getting the reticle to write was that the time out feature on the tool was set too long so the mask writer would write

for 10 minutes and then perform another baseline registration. This time was too long and the tool would simply drift too long during this time and it would not be able to continue writing due to reregistration errors. This problem was simply fixed by setting this time to a much shorter more reasonable value such as 2 minutes between reregistration.

Some initial tests were performed and it was determined that the process window was very small when patterning on oxide. An initial FE had shown that a bare silicon wafer had a minimum resolvable feature of 350 nm. However once this patterning was done on a wafer that had a thermal oxide grown on it, the minimum feature size was 550 nm, because the CD swing was much greater with this additional interface.

Initially the OLN-620i resist was thinned down to a ratio of 2:1 by adding a 50:50 mixture by volume of resist to PGMIA solvent. This new lower viscosity resist had a new spin speed range of 400-500 nm. However it was determined after an etch screening this would not protect sufficiently during the etch process. In order for a usable image to occur in the normal viscosity resist a bottom anti reflective coating or BARC was used to improve the process window. Brewer Science's ARC-ICON was chosen to be the best choice for advanced I-line processing. Another challenge that this involves is the fact that with a positive tone resist and a darkfield reticle this process involved imaged spaces rather than lines and due to the energy distribution this also caused a decreased exposure latitude. In the future there may be more process latitude to work with a clear field reticle and a negative resist.

Another problem that occurred was the variation in oxide thickness that resulted in pattern fallout at the edge of the wafer. Even though the variation from center to edge was only about 1.5% when these non-idealities compounded with an additional 1.5% thickness variation in BARC thickness and resist thickness, it causes significant difference in optical path length that increases substrate reflection to a non optimal location on the swing curve. Future work could improve upon the oxide thickness variation, and more importantly improve spin coating with a designed experiment. Some of the important input factors may be ramp rates and really controlling how the photoresist and BARC flow and remove solvents across the wafer.

Initially the oxide etch was performed in the Drytec Quad RIE system and it was determined that this tool was not optimum for etching 6 inch wafers due to the electrode design. A much better tool for 6 inch wafers, the P5000 was utilized in the etch process. However it was determined after trial and error in this tool that the wafers could not have oxide on both the front and back side, otherwise arcing would occur and could potentially ruin the process kit. The reason that this arcing occurs is based on the fact that the tool

V. PROCESS PARAMETERS

The first step in preparing a device wafer was to grow the thermal oxide. Bruce tube 1 was used to grow the wet thermal oxide. This oxide was chosen to be wet thermal oxide, rather than a dry thermal due to time constants and the fact that growing oxide on the order of 1 micron was expensive and takes a relatively long time and can use significant chemical. Also an thermal oxide much thicker than 1 micron causes such a great amount of stress that it induces oxidation induced stacking faults which may not be annealed out. This oxide could be deposited, but one of the constraints was that this must be a thermal oxide due to its higher interface quality. A deposited TEOS may be interesting to investigate for backend devices with a lower

allowance for a thermal budget. The SMFL 10000 angstrom recipe was used. An oxide thickness of 950 nm was measured. Next a blanket resist coat was performed so that the front side of the wafer could be protected. A ten minute HF etch was then performed in the 5.2:1 BOE etch would remove all of the oxide off of the backside of the wafer so that arcing would not be a problem in the P5000 etch chamber.

A Prolith simulation was performed to determine where the minimum substrate reflection is for the BARC. The thickness that yielded excellent results was around 100 nm BARC thickness. This thickness was limited by the speed of spinning 6 inch wafers. Ideally it would have been easier for the BARC to be coated around 150 nm, and the originally targeted oxide thickness would allow for this, but due to the offset in the oxide thickness. The spin speed curve was used for from Brewer Science's datasheet. This curve was verified by measuring the thickness with both the profilometer and nanospec at three different spin speeds so that an optically measured thickness and a profilometry measurement was obtained.

The BARC was coated using the appropriate spin speed. A spin speed of 4000 RPMs was used to obtain a BARC thickness of 110 nm. A single stage 180 degree bake was used to crosslink the BARC. No prime was used for both the resist step and the BARC coating. The resist was then coated by using the standard coat recipe with a spin speed of 3250 RPMs. A post apply bake (PAB) of 90 degrees Celsius was used. Two separate stepper jobs were ran. The first job (RIT_ART) was programmed to run with reticle carrier 12 and used the recently designed RIT ART reticle. An optimum exposure of 130 mJ/cm² was used. A best focus of 1 μ m was found to be focusing to the bottom of the resist stack. The resist thickness was verified to be 1050 nm. The second exposure RIT_ART2, was done just to form open areas in which bulk film could be grown directly on silicon without spacers. This region was also very beneficial to measure film thickness and to watch during the etch process because there was no optical end point set up on the P5000 etch tool. The post exposure bake (PEB) was kept at the default 110 degrees centigrade. A single stage puddle develop was used. A two stage puddle develop was also experimented with, but it did not yield any better results. Finally the hard bake was lowered from 132 degrees to 125 degrees to ensure that the resist did not reflow.

The final etch process used on the P500 was composed of three steps: a stabilize step which the gas flows, 40 Gauss electric Field turned on for 20 seconds, followed by the etch step which turned on the RF power to 500 W, and finally the gases were turned off and the chamber was pumped down. The gases used were 100 SCCM of CHF₃, 50 SCCM of CF₄, and 10 SCCM of O₂. A hard ash was then done to remove all of the organics from the wafer surface. After this was completed a 2 minute KOH etch was performed to give the v-groove profiles. Finally an RCA clean was completed to remove any surface contaminants.

VI. DISCUSSION OF RESULTS

While characterizing the lithography some screening ran some screening runs through the process flow to determine if the SMFL fab was in fact clean enough to run samples through an outside companies reactor. Due to cost only several samples were sent to a sample called Mentrion Chemtrace. Several wafers were ran through a blanket version of our process flow and the analysis method used was VPD ICP MS. This analysis method must be done on wafers without topography. Notice the results of the top ten contaminants on the right. The first wafer was the bare starting substrate. This sample was run to get a baseline for our starting material and to

determine that our starting material was not the source of the surface contaminants. The second sample was one that ran through the complete pattern transfer process. Finally the last sample was exactly the same as the second one with the exception that it had an RCA clean after wards. It can be seen that generally speaking the cleaned wafer came out much lower than the process flow run, and in some cases even lower than the starting substrate. Notice the high levels of Al this is probably due to the fact that a lot of the etch chamber is made of aluminum. Also many of the other metals are components of stainless steel. A further investigation needs to be done to confirm where these contaminants have come from. These metal levels are at acceptable levels to perform a growth in an outside reactor.

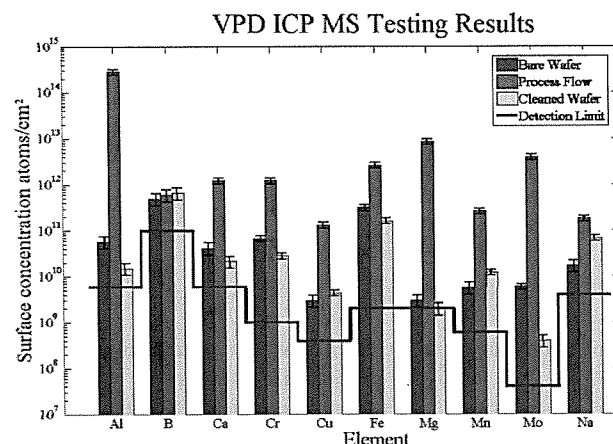


Fig. 6 VPD ICP MS test results

Figure 7 shows the lithography results. During the initial run prior to hard bake optimizing no 400 nm features were present. By optimizing focus and lowering the PEB yielded better profiles. Also notice were within 10% of their targeted widths. This was determined to be sufficient and in order to obtain a tighter distribution of CD's results a mask bias needs to be utilized to hit the proper exposure for these different density features.

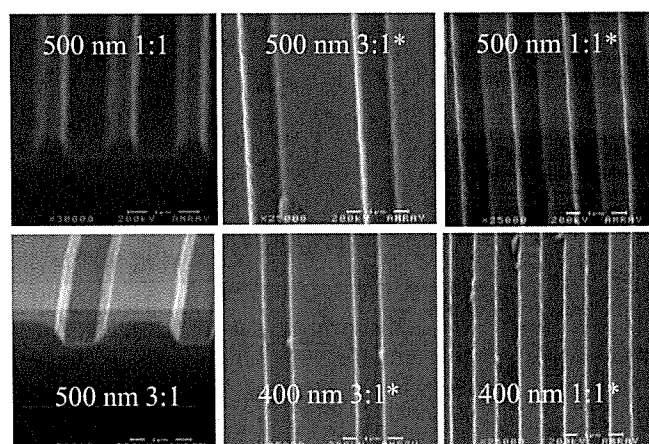


Fig. 7 RIT ART mask design

Figure 8 shows another substrate reflectivity simulation performed in Prolith. Oxide thickness is shown on the y axis and BARC thickness on the bottom axis. Initially recycled wafers were used to perform some of the lithography screening runs. This occurred with about 990 nm of oxide during the initial run. At this oxide thickness a BARC thickness of about 155 nm minimized the substrate

reflection. Figure 8 illustrates the idea that the process latitude and allowable film thickness variation is quite good in this region. However when the device wafers were grown the oxide thickness came out a bit thinner than the previous run. This now put the swing and reflectivity in a non optimal location can be seen by the 2 in fig. 8. These wafers were reworked with an adjusted spin speed on the BARC to give another thickness and my small features again appeared when the other minimum was used. This is a good verification that PROLITH can be used to accurately predict the process at RIT.

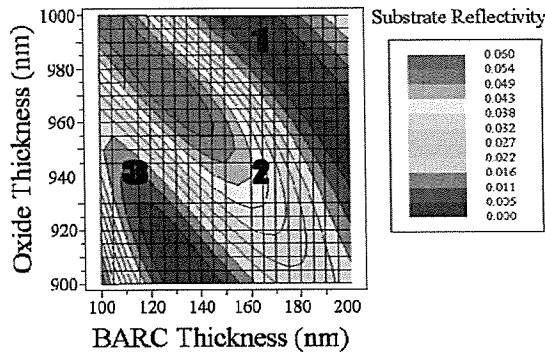


Fig. 8 Substrate Reflectivity vs. film thickness

In the etch process the selectivity was characterized while etching the BARC and after the BARC had been etched. Initially the selectivity was about 1.2:1 while etching the BARC because some of the photoresist was etching as well due to the oxygen in the etch chemistry. The BARC needed oxygen to etch well. The oxide then had an selectivity of about 2:1. Notice in fig. 9 there was remaining resist and this allows for an over etch to account for etch non-uniformities.

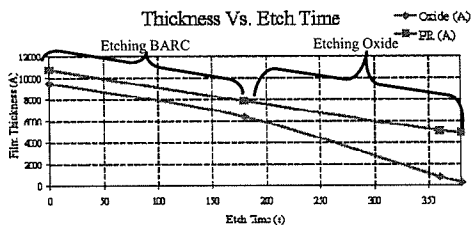


Fig. 9 Etch Rate of oxide and photoresist

It can be seen that the etched profiles turned out well for the 3:1 features however a slight over etch has occurred. The 1:1 features showed some scalloping, or summing issue that was most likely caused by the dramatic overetch. It is interesting to see that this image shows the aspect ratio dependence of the etch.

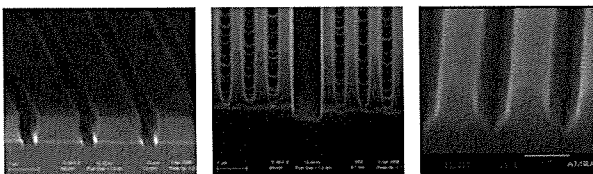


Fig. 10 a 3:1 500 nm spaces, 1:1 400 nm lines, 1:1 500 nm v-grooves

Finally a KOH etch was done to generate the additional samples that Amberwave had wanted to characterize. One of the main

concerns was that all of the etch material was not cleared out, and the fact that V grooves formed is a good indication that this occurred.

VII. CONCLUSION

It has been shown that high aspect ratio patterning here at RIT was indeed possible, but the process window was very slim. Many of the challenges presented involved working with an outside company, and several delays occurred during the project that was not planned for in the project timeline. An interesting side project involved running several screening experiments to determine the metal contamination levels in our the SMFL laboratory. Metal contamination levels are low enough after a RCA clean to send material out and several samples are ready to send to Amberwave. Future work to continue this project includes improving the current process. One method of patterning significantly smaller features would be to make a chromeless phase shift reticle. Once these structures are generated it would be possible to build a GaAs laser. Other device related projects could work on integrating silicon devices with other III-V's such as high mobility MOSFET channels. It was seen that ART is a key enabler to integrating III-V semiconductor materials into the current silicon infrastructure.

ACKNOWLEDGMENTS

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He had worked for the Office of Naval Research in Washington DC in the Summer of 2005, doing research on carbon nanotubes for field emitters. Then his work led him to Richmond, VA and he worked for Infineon Technologies as a lithography process engineer. Intel technologies was the next stop on his road map in the winter of 2007 again working as a lithography process engineer.

Mr. Fourspring has been a student member of IEEE at the Rochester Institute of Technology, in the past helping out with their design conference. Also he is a member of MESA (Microelectronic Engineering Student Association) which contributes to many projects at the SMFL (Semiconductors and Microsystems Fabrication Laboratory).