

Developing an Empirical Model for Tunable Porosity in Porous Nanocrystalline Silicon Membranes

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Abstract—In this study, a new process for the fabrication of porous nanocrystalline silicon (pnc-Si) membranes is proposed, and the early stages in the development of an empirical, stress-based model for tunable porosity are revealed.

Pnc-Si membranes that were fabricated by the proposed process showed substantial improvements in membrane morphology, i.e., porosity and pore uniformity across the wafer. These improvements were assumed to be related to stress, as suggested by the addition of materials that differ in Young's Modulus and in coefficients of thermal expansion. In order to explore this assumption, stress measurements were conducted via stylus trace on a Tencor P2 Profilometer. Extensive average stress (dynes/cm²) measurements were performed by varying thermal and RF Magnetron sputtered SiO₂ thickness on bare, 400 μ m thick, <100> orientation, double-sided polished silicon wafers.

It was found that the stress-profile differences between the standard and proposed processes were significant as the change in the wafer bow (due to film stress), across the wafer (relative to the bare substrate), were plotted for varied oxide thickness during the three major stages of pnc-Si development. The resulting plots were 2nd order polynomials (best-fit RMS \cong .970-.999), which agree with the form given by Stoney's equation for macro stress acting in a coating deposited on a thick substrate. These differences have been consistent in multiple experiments and are currently being evaluated for their role in membrane porosity.

Index Terms— porosity, porous nanocrystalline silicon (pnc-Si) membranes, profilometer.

I. INTRODUCTION

This study is based on a new type of porous silicon material in the form of an ultrathin nanoporous membrane, first reported in the journal *Nature*¹. Termed porous nanocrystalline silicon (pnc-Si), this material is fabricated through solid-phase crystallization of a sputter deposited amorphous silicon (a-Si) film on a silicon wafer substrate.

Pores in the size range of 5 nm to 100 nm form during a brief annealing step and pass completely through the original 5 nm

to 25 nm thick amorphous film. Following photolithographic and etching processes, freely suspended porous membranes are made that offer unprecedented efficiency in nanoscale separation processes and are sufficiently thin for transmission electron microscopy (TEM) applications.

II. OBJECTIVE

The standard process in the fabrication of pnc-Si membranes is shown below (Fig. 1):

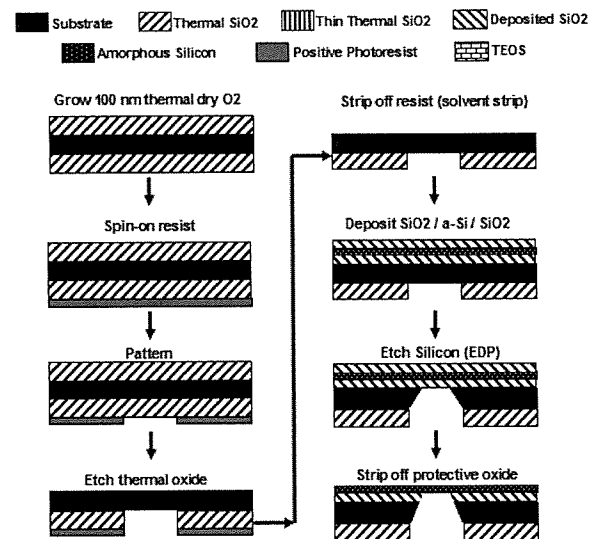


Fig. 1. Standard process for the fabrication of pnc-Si membranes.

While the current process in the fabrication of pnc-Si membranes has proven to be relatively simple and reliable, two main processing issues have hindered yield. Firstly, during the oxide pattern etch step, the front-side silicon surface is exposed before a critical three-film deposition phase. Consequently, the hydrophobic silicon surface demands aggressive treatment for contamination and surface damage to maintain yield. This involves multiple, time-consuming processing steps. Secondly, recent experiments have shown that the current process tends to form pores in radial gradients across the wafer. The large variance in porosity is such that virtually no pores form in locations near

the center of the wafer, but maintain reasonable densities in positions along the wafer edge (Fig. 2):

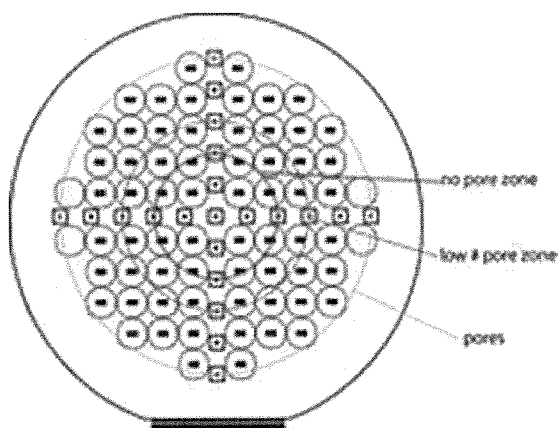


Fig. 2. Three regimes of pore formation across the wafer for pnc-Si membranes fabricated with the standard process.

The non-uniformity in porosity was verified by analysis of TEM samples across several wafers fabricated by the standard process in Fig. 1. The TEM images in Fig. 3 (below) show the porosity difference that was observed in samples positioned in the center and edges of the wafer:

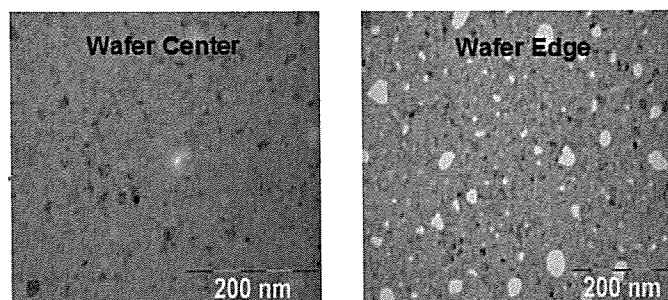


Fig. 3. TEM micrographs of two pnc-Si membrane samples taken from center and edge positions on the same wafer. This non-uniformity in porosity has been frequently observed for membranes fabricated with the standard process in Fig. 1.

This non-uniformity in porosity has hindered yield and has impeded efforts in developing a model for predictable porosity in pnc-Si membranes.

III. EXPERIMENT

A. Proposed Process

In this study, a new process is presented that offers improvements to the traditional pnc-Si process deficiencies as described above (Fig. 4):

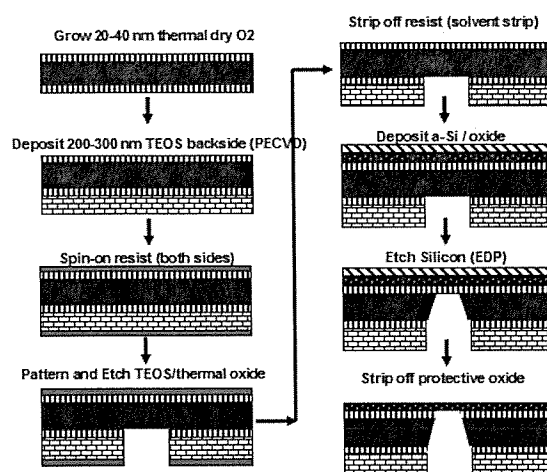


Fig. 4. Proposed process for the fabrication of pnc-Si membranes resulted in improved porosity and pore uniformity across the wafer.

The main feature of this newly developed process is the replacement of the RF magnetron sputtered SiO_2 (underneath the membrane) with a thin (20nm-40nm) thermally grown oxide that protects the silicon front surface during the entire process. Tetra-ethyl-ortho-silicate (TEOS) is also deposited on the backside of the wafer (PECVD), after the initial thermal oxide growth, in order to provide a robust pattern that can withstand the ethylenediamine pyrocatechol (EDP) etch of silicon in subsequent processing.

B. Process Improvements

Consequently, the addition of back-side TEOS and thermally-grown SiO_2 has resulted in substantial improvements in membrane morphology, i.e., porosity and pore uniformity across the wafer. The difference in porosity can be observed from two TEM micrographs that were generated from two different processes (Fig.1 & Fig. 4), taken from the same position on the wafer (Fig. 5 & Fig. 6):

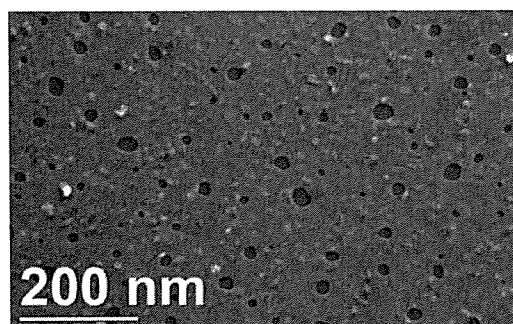


Fig. 5. TEM image of a pnc-Si membrane (magnified 150kX) for membranes fabricated with the standard process in Fig. 1. The resulting porosity is low (0.33%-2.7%) and non-uniform across the wafer.



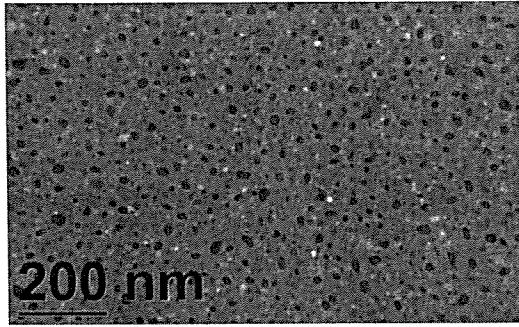


Fig. 6. TEM image of a pnc-Si membrane (magnified 150kX), for membranes fabricated with the proposed process in Fig. 4, demonstrating a much higher porosity (4.2%-12.4%) than traditional membranes yield (Fig. 5).

Further analysis of membrane porosity was conducted using a Matlab image simulator to generate statistical porosity data for TEM micrographs to provide quantitative results. The results show that the standard pnc-Si process produces membranes with porosity ranging from 0.33%-2.7%, while the proposed process achieves porosity in the range of 4.2%-12.4%.

To show that pore uniformity across the wafer had been achieved using the proposed process, refer to Fig. 7 where TEM micrographs of the membrane at the center and edge of the wafer are shown (Fig. 7):

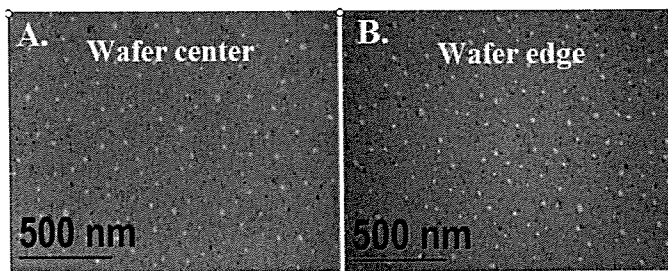


Fig. 7. TEM micrographs of two pnc-Si membrane samples taken from center and edge positions on the same wafer. The improved uniformity in porosity has been frequently observed for membranes fabricated with the proposed process in Fig. 4.

These TEM images can be compared directly to the images in Fig. 3. After several samples had been fabricated and compared, it became evident that, for membranes fabricated with the proposed process, porosity had been maintained across the wafer. The improvements in porosity and in pore uniformity across the wafer with this process was assumed to be stress-related, as suggested by the addition of materials that differ in Young's Modulus and in coefficients of thermal expansion.

C. Stress Characterization

In order to explore this assumption, stress measurements were conducted via stylus trace on a Tencor P2 Profilometer. Extensive average stress (dynes/cm²) measurements were performed by varying thermal and RF Magnetron sputtered SiO₂ thickness on bare, 400 μ m thick, <100> orientation, double-sided polished silicon wafers. These results were then compared to reliable experimental average stress values (as determined by C.H. Bjorkman *et al.*²) to assure confidence in the accuracy of the profilometer.

To obtain results for analysis, the change in the wafer bow (due to film stress), across the wafer (relative to the bare substrate), were plotted for varied oxide thickness during the three major stages of pnc-Si development. The resulting plot is shown below for membranes fabricated with the standard process (Fig. 8):

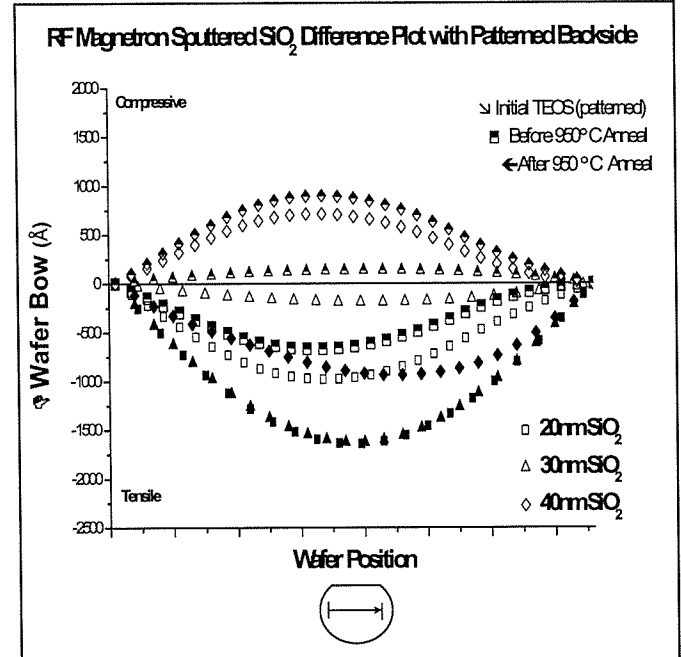


Fig. 8. Stress-profile across the wafer for deposited SiO₂ layer beneath the membrane. Measurements were conducted for i) initial oxide on bare silicon, ii) three-layer stack (SiO₂/a-Si/SiO₂) before anneal iii) three-layer stack after anneal.

All of the RF magnetron sputtered SiO₂ stress-difference curves that were generated in this experiment exhibit a translational shift in relative minima/maxima from the initial SiO₂ deposition (on bare Si) to the three film layer stack (SiO₂/a-Si/SiO₂). The translational shift is given in its general form as:

$$f(x) \Rightarrow f(x \pm \beta)$$

where β describes the shift in terms of wafer position.

The same stress measurements were conducted for a bottom thermal SiO₂ layer that is introduced with the proposed process:

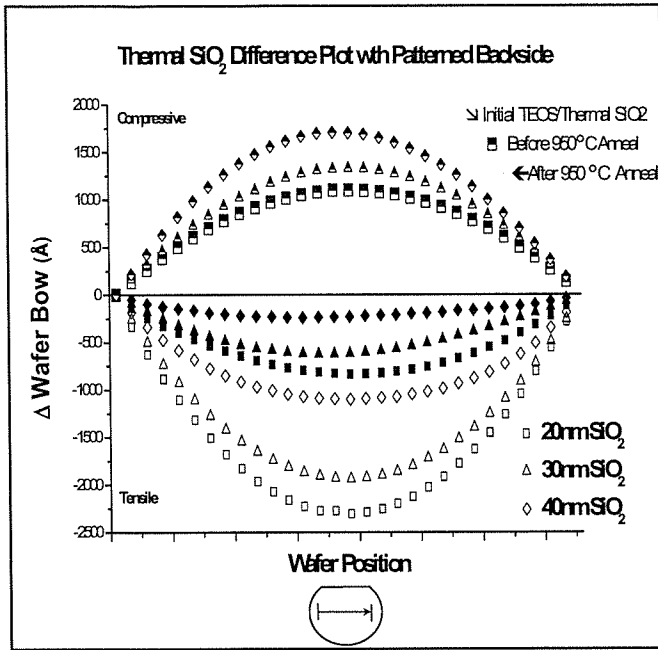


Fig. 9. Stress-profile difference across the wafer for thin (20nm-40nm) thermal SiO₂ layers beneath the membrane. When compared to Fig. 8 for deposited SiO₂, there are some significant differences that warrant a deeper, more detailed investigation.

IV. ANALYSIS

Unlike the RF Magnetron sputtered SiO₂ difference plot in Fig. 8, the thermal SiO₂ difference plot in Fig. 9 exhibits little to no translational shift when stress is measured i.) after the initial thermal oxide deposition (on bare Si) and ii.) following the deposition of the three layer stack (SiO₂/a-Si/SiO₂). The change in relative maxima for curves representing the stack before and after the 950°C anneal is also considerably larger (~1000 X change in wafer bow) than the change observed in Fig. 8 (250-400 X change in wafer bow). In fact, when using thermal SiO₂ beneath the a-Si, each curve shifts into the tensile domain (negative Y-axis) after the anneal. Analysis of the difference plot in Fig. 8 shows that the change in maxima for the same curves is extremely small and only shifts into the tensile domain when a thinner oxide is used (20nm - 30nm).

After several difference plots were generated with different materials of varying thickness, it was determined that the change in relative maxima before and after the 950°C anneal may be directly related to porosity. It was also determined that the change in translational shift (β), may directly represent the area of the wafer that prevents pore formation, which explains why the uniformity is maintained in the thermal SiO₂ case. (The difference plots have been enhanced to detail the fore-mentioned differences and can be found in the APPENDIX).

V. CONCLUSION

This study has shown that the proposed process not only succeeded in reducing process steps and controlling pore uniformity, but has also revealed the necessity for stress-based pnc-Si experiments. To address this, the initial stages in the development of an empirical model for pnc-Si stress-based measurements were conducted. This development is profound since a model characterizing the effects of stress modulation on pnc-si membrane pore formation has never been reported.

REFERENCES

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APPENDIX

